APPROXIMATION OF WIRING DELAY IN MOSFET LSI

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Abstract—Two approximation methods for wiring delay in MOS LSI are studied. One is analytical and the other is a lumped circuit approximation. The basic model for wiring is a distributed *CR* line with a drive MOSFET at one end and a capacitive load at the other end. Simple approximated formulas for the delay and the step response of this model are obtained.

Approximation of a distributed *CR* line by lumped *R*'s and *C*'s combination, which is very useful when incorporated in circuit simulation programs, is also investigated. The widely used *L* ladder circuit model is found to be a poor approximation, while π and *T* ladder circuit models give satisfactory results. The simplest circuits that approximate the interconnection line within a given tolerant error are tabulated under various drive and load conditions.

List of Symbols

c	Capacitance of wiring per unit length
r	Resistance of wiring per unit length
L	Length of wiring
C	Total capacitance of wiring ($=c \cdot L$)
R	Total resistance of wiring ($=r \cdot L$).
c_t	Load capacitance, including MOS transistor gate capacitance to be driven
r_t	Equivalent resistance of drive MOS transistor
C_T	$= c_t/C$
R_T	$= r_t/R$
x	The coordinate from driven point to load
t	Time
t'	Normalized time ($= t/CR$)
s	Laplace transformed variable for t
s'	Laplace transformed variable for t'
σ	$= -s'$
v	Voltage
V	Laplace transformed voltage
i	Current
I	Laplace transformed current
v_{cc}	Supply voltage
REMP	Relative error of minimum pole
subindex D	Distributed CT line
subindex L	L ladder circuit
subindex π	π ladder circuit
subindex T	T ladder circuit, except for C_T and R_T.

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I. Introduction

In MOSFET LSI, a wiring delay becomes an important factor in determining total delay of a system. Particularly, the delay induced by word lines, bit lines, clock lines, and bus

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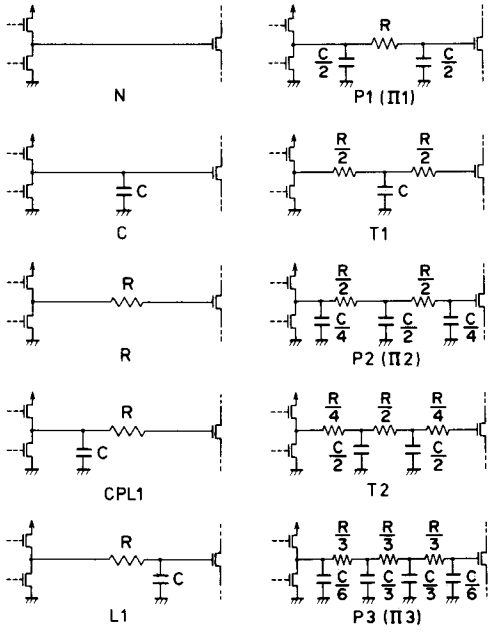

Fig. 1. Various lumped circuits used to approximate a wiring. N: no additional circuits; C: only one capacitor; R: only one resistor; $CPL1$: C preceding L circuit; $L1$: one-step L circuit; $P1$: one-step π circuit; $T1$: one-step T circuit; $P2$: two-step π ladder circuit; $T2$: two-step T ladder circuit; $P3$: three-step π ladder circuit.

lines in memory or logic LSI are essential to operation speed of a chip. These interconnection lines are considered as distributed *CR* lines. In order to evaluate the *CR* line delay, the first step is to estimate the capacitance and the resistance of the line [1]-[3] and the second step is to calculate the response of the line. The distributed *CR* lines are to be described by partial differential equations, and extensive studies have been made to solve the differential equations. A good review of this field is given by Kumar [4].

At the initial stage of designing MOS LSI's however, it is convenient to have some simple formulas which express the approximated behavior of the distributed *CR* line. One of the objects of this paper is to give simple formulas for the delay and the step response of the interconnection lines under various external circuit conditions. Some analytical work has been done by Penfield *et al.* [5] to give the upper and lower bounds of the *CR* line delay. In this paper, much stress is put on simplifying the formulas for a step response and a delay time of distributed *CR* lines without too much degradation of the accuracy. The resultant formulas are suitable for roughly estimating a partial delay of a system, such as a word line delay.

At the middle and final stage of an MOS LSI design, in order to evaluate a total system performance, interconnection lines are usually substituted by equivalent lumped circuits (see Fig. 1 for various equivalent lumped circuits). Then, they are simulated by CAD circuit programs such as SPICE, ASTAP, and SCEPTRE. This method is widely used, but the accuracy of this approximation was not clear. The second object of this paper is an assessment of the method. A comparison between the transfer function of a distributed *CR* line and that of the lumped circuit models is made to shed light on this accuracy problem. As a result, the usually adopted L ladder circuit model is found to be a poor approximation. The relative error of the delay amounts to as much as 30 percent, even when three ladder steps are concatenated. On the other hand, π or T ladder circuit models can simulate the distributed *CR* line very well. In this case, the relative error of the delay is less than 3 percent even in the worst case if three ladder steps are connected. When a tolerant error and an external circuit condition are given, there is a simplest lumped circuit that approximates the wiring delay within the tolerance. This circuit is useful in reducing computational cost, so it is tabulated in Section IV-B.

Two examples of the application of the above-mentioned approximation are presented in Section V. One is for a word line in an n-channel LSI memory of the next generation, and the other is for CMOS design. Conclusions are summarized in Section VI.

II. Basic Model for Wiring

The basic model considered in this paper is a distributed *CR* line whose one end (point 1) is driven by MOSFET's and the other end (point 2) is connected to the gates of MOSFET's as shown in Fig. 2(a). Most of the wiring in an MOS LSI can be reduced to this form. Then, the drive transistor is replaced by an equivalent resistance r_t and the load transistor by a capacitance c_t as is shown in Fig. 2(b), in order to make the problem tractable. This replacement by r_t is not exact, but it is the simplest way of taking the drive conditions into account. The value of r_t is between 1/(maximum drain conductance) and 1/(minimum drain conductance). However, the good choice of r_t turns out to be the former in this paper. Detailed discussions on r_t are given in Sections IV and V. $r_t/R \ll 1$ corresponds to a constant voltage drive and $r_t/R \gg 1$ to a constant current drive.

Charging-up of the line is explained in Fig. 2(b). The same discussion can be used for the discharging case, due to a linearity of this equivalent circuit. Conclusions about delay time and the accuracy of lumped models are essentially unchanged. Although discussions are mainly concentrated on the voltage response of the endpoint of the line (point 2 in Fig. 2), some calculations are carried out on the current and voltage waveform of an arbitrary position of the line for $c_t = r_t = 0$ in Appendix A. This endpoint is important because it shows the slowest response and decides the system speed. The transfer function $T_D(s')$ from point 0 to point 2 is written as

$$T_D(s') = \frac{1}{(1 + s'C_TR_T)\cos\sqrt{-s'} - (R_T + C_T)\sqrt{-s'}\sin\sqrt{-s'}}. \tag{1}$$

Detailed derivation of this equation is given in Appendix B. As is seen from (1), it is not the absolute values of C, R, c_t, and r_t, but the ratios c_t/C and r_t/R that determine a voltage response of the line. It is interesting to note that C_T and R_T are symmetrical in (1), and this indicates that the drive and load conditions are of equal importance.

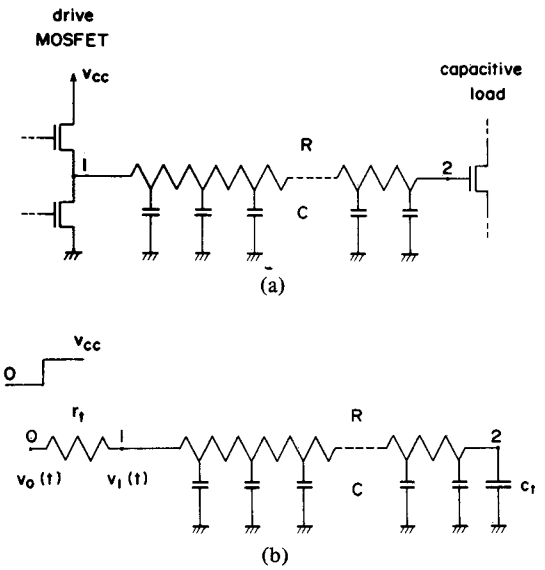

Fig. 2. (a) Basic model for wiring in MOS LSI. (b) Equivalent circuit of the basic model. The drive MOSFET is replaced by an equivalent resistance r_t and the load MOSFET by a capacitance.

III. Analytical Approximation

A. One Exponential Function Approximation

When a step voltage is applied at the gate of a drive transistor, the response of point 2, $V_2(s')$, is written as

$$V_2(s') = \frac{v_{cc}}{s'} T_D(s'). \tag{2}$$

Denoting the absolute values of the poles of (2), $0, \sigma_1, \sigma_2, \cdots, \sigma_k, \cdots$, in an increasing order, the response in time domain $v_2(t')$ can be expanded in multiexponential form as follows, by using Heaviside's expansion theorem:

$$\frac{v_2(t')}{v_{cc}} = 1 + \sum_{k=1}^{\infty} C_k e^{-\sigma_k t'} \tag{3}$$

where

$$C_k = (-1)^k \cdot \frac{2\sqrt{(1+R_T^2\sigma_k)(1+C_T^2\sigma_k)}}{\sqrt{\sigma_k}\,\{(1+R_T^2\sigma_k)(1+C_T^2\sigma_k) + (R_T+C_T)(1+R_TC_T\sigma_k)\}_{\sigma=\sigma_k}}. \tag{4}$$

Sigmas are the solutions of the following equation:

$$\tan\sqrt{\sigma_k} = \frac{1 - R_TC_T\sigma_k}{(R_T+C_T)\sqrt{\sigma_k}}. \tag{5}$$

It is shown by inspection of (5) that

$$(k-\tfrac{3}{2})\pi < \sqrt{\sigma_k} < (k-\tfrac{1}{2})\pi. \tag{6}$$

However, (5) can be solved exactly only when $C_T = R_T = 0$ as is given in Appendix A. In other cases, the solution must be numerical.

In the multiexponential expansion of the step response, (3), the third term is found to be less than 10^{-9} at the time when $v_2(t')$ is equal to $0.9v_{cc}$ even if C_T and R_T vary from zero to infinity. This means that the terms higher than the third can be neglected if a global waveform is of interest. That is, the following equation is an excellent approximation:

$$\frac{v_2(t')}{v_{cc}} = 1 + C_1 \cdot e^{-\sigma_1 t'}. \tag{7}$$

Fig. 3 shows a comparison between the exact voltage response and the approximated response by (7). Numerically calculated σ_1 and C_1 are plotted in Fig. 4, respectively, for various C_T and R_T.

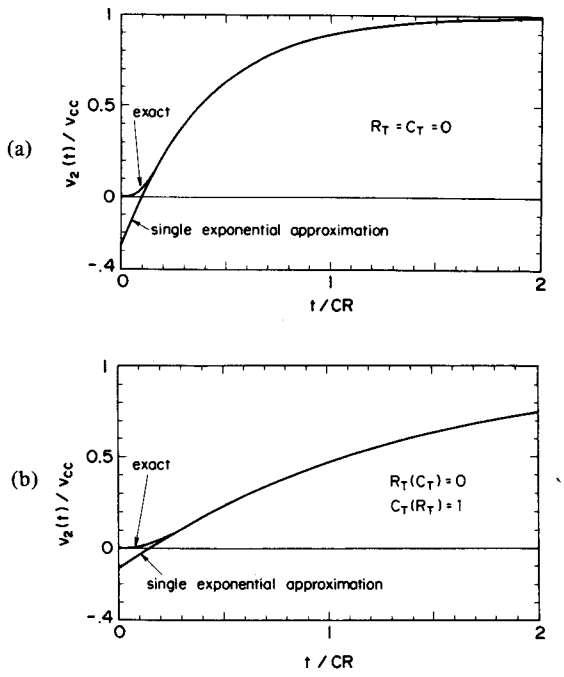

Fig. 3. One exponential function approximation for a step response of an interconnection line. Exact waveform is also shown as a reference. (a) $R_T = C_T = 0$. (b) $R_T = 0$, $C_T = 1$ or $R_T = 1$, $C_T = 0$. Approximation is excellent at $v = 0.9v_{cc}$.

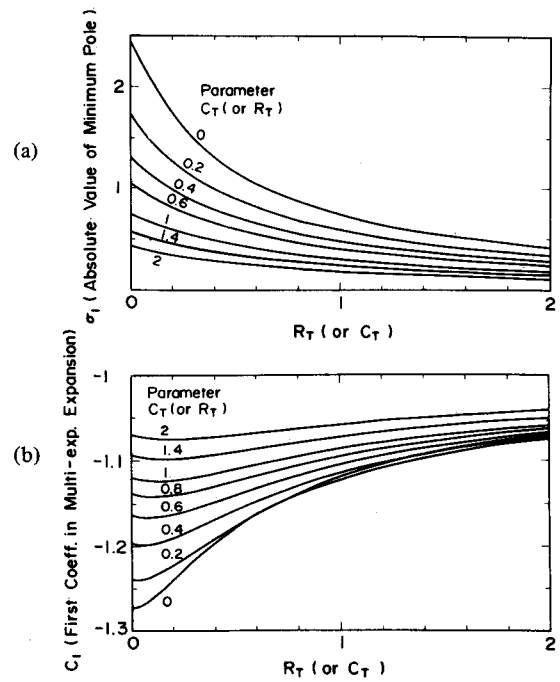

Fig. 4. (a) Minimum pole (σ_1) of transfer function of distributed CR line for various C_T and R_T. (b) First coefficient (C_1) in multiexponential expansion of step response of a distributed CR line.

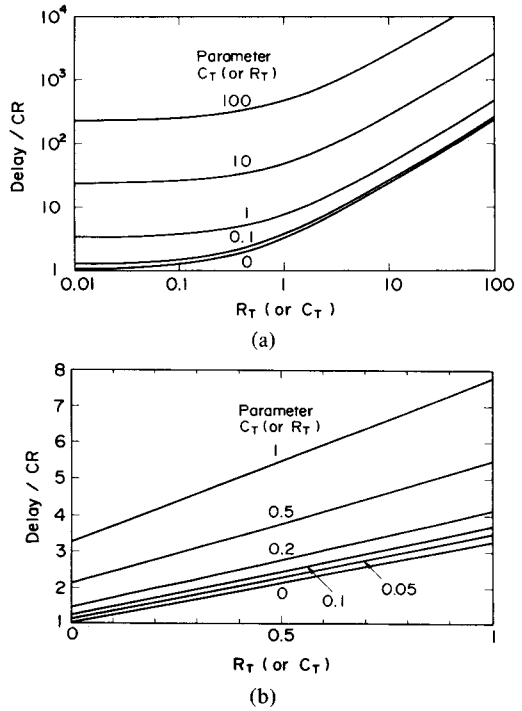

Fig. 5. Delay ($t_{0.9}$) of a distributed CR line. (a) In log scale. (b) In linear scale. When x-axis is chosen for R_T, parameter is C_T. When x-axis is chosen for C_T, parameter is R_T.

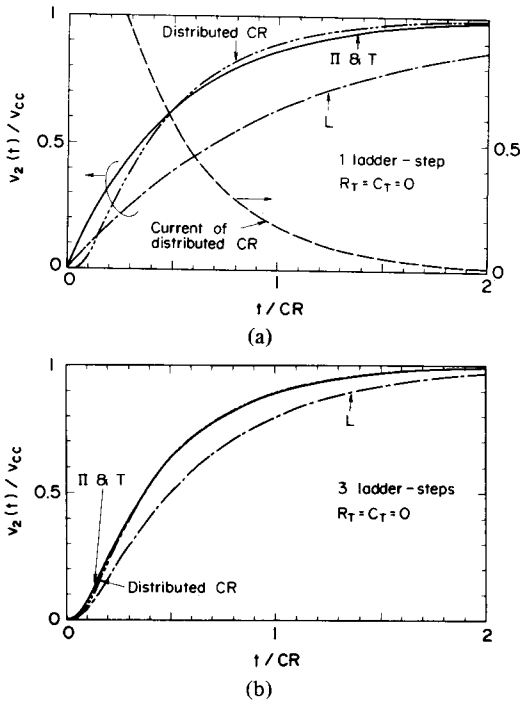

Fig. 6. Step responses of L, π, and T ladder circuits and distributed CR line for $C_T = R_T = 0$. (a) Number of ladder steps = 1. Current is also shown. (b) Number of ladder steps = 3. π and T ladder circuits approximate a distributed CR line much better than the L ladder circuit does. Although only waveforms for charging-up case are shown, those for discharge are easily seen if the chart is put upside down because of the linearity of the circuits.

B. Delay Time

We define $t_{0.9}$ as a time delay to a step voltage at the drive point 0 to the time when the node 2 in Fig. 2(b) reaches $0.9v_{cc}$. Since the accuracy of (7) is excellent, normalized delay $t'_{0.9}(=t_{0.9}/CR)$ is calculated as follows:

$$t'_{0.9} = \frac{1}{\sigma_1} \ln |10C_1|. \tag{8}$$

Fig. 5 shows calculated results of $t_{0.9}$. When R_T and C_T are large, the delay time is proportional to R_T or C_T, as seen from Fig. 5(a). In this region, the delay is limited by the drive capability of a MOSFET or the capacitance of the load. On the other hand, when both of R_T and C_T are small, the delay is almost constant, limited by the line itself.

Fig. 5(b) shows a nearly linear dependence of $t'_{0.9}$ on both C_T and R_T, so that it is suspected that $t'_{0.9}$ can be approximated by $a + bC_T + bR_T + cC_TR_T$ where a, b, and c are constants. In fact, setting these constants so as to minimize the relative error in the range $C_T, R_T < 1$, the delay is found to be expressed in a very simple form as

$$t_{0.9}/CR = 1.02 + 2.21(C_TR_T + C_T + R_T). \tag{9}$$

The relative error of this formula is within 1.1 percent when both C_T and R_T are less than unity, and is less than 4 percent for any C_T and R_T.

IV. Lumped Circuit Model

The previous section deals with an analytical approximation which is useful in the initial stage of LSI design, but is not compatible with circuit simulators. Lumped models which are suited for CAD programs are treated in this section.

A. L and T Ladder Models

Some of the examples of π, T, and L ladder circuit models are shown in Fig. 1. The names are derived from the shape of their unit blocks. These circuits are chosen here because parameters of the circuit elements are easily obtained and the circuits coincide with a distributed CR line when the number of ladder steps goes to infinity. Rajput proposed a nonuniform ladder circuit to approximate a distributed CR line [6]. The use of the circuit must be restricted because it does not reproduce the correct response when the line is driven bidirectionally. Moreover, it is difficult to improve the approximation easily.

Initially, discussions are confined to the case of $c_t = r_t = 0$. Transfer functions of L, π, and T ladders are obtained in Appendix B as

$$T_L(s') = \frac{1}{\cos(n\zeta) - \frac{1}{2n}\sqrt{-s'}\sin(n\zeta) \Big/ \sqrt{1 + \frac{s'}{4n^2}}} \tag{10}$$

$$T_\pi(s') = T_T(s') = \frac{1}{\cos(n\zeta)} \tag{11}$$

where

$$\tan\zeta = \sqrt{-\frac{s'}{n^2}\left(1 + \frac{s'}{4n^2}\right)} \Big/ \left(1 + \frac{s'}{2n^2}\right). \tag{12}$$

Step responses of these circuits for $n = 1$ and 3 are shown in Fig. 6 with responses of a distributed CR line as a reference. These responses can be calculated through Heaviside's expansion theorem, similarly to (3), if σ_k's and C_k's are obtained. σ_k's are expressed as

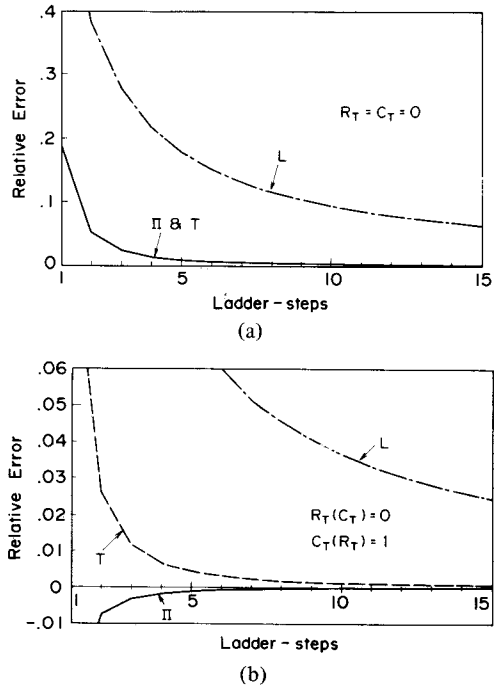

Fig. 7. Relative error of minimum pole (REMP) of L, π, and T ladder circuits. (a) $C_T = R_T = 0$. (b) $R_T = 0$, $C_T = 1$ or $R_T = 1$, $C_T = 0$. REMP is almost equal to relative error of a delay as seen from Figs. 6, 8, and this figure. Accuracy of the model increases as the number of ladder steps n increases, but it saturates at about 3 or 4.

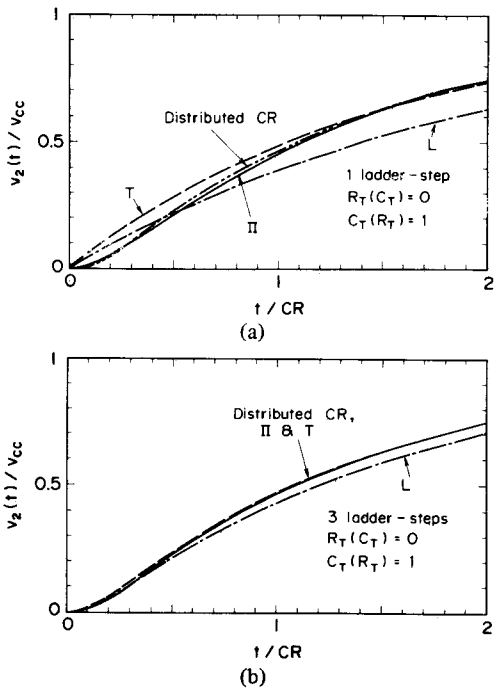

Fig. 8. Step responses of L, π, and T ladder circuits and a distributed CR line for finite C_T or R_T, namely C_T $(R_T) = 0$, R_T $(C_T) = 1$. (a) Number of ladder steps = 1. (b) Number of ladder steps = 3. π and T ladder circuits approximate a distributed CR line much better than the L ladder circuit does.

$$\sigma_k = 4\left[n \sin\left(\frac{2k-1}{4n}\pi\right)\right]^2 \qquad (k = 1, 2, \cdots). \tag{13}$$

As for the L ladder circuits, Newton's method is applied to search the poles of (10). C_k is calculated numerically by the following formula:

$$C_k = \lim_{\epsilon \to 0} \frac{T(s')}{s'} \cdot (s' + \sigma_k + \epsilon) \tag{14}$$

where $T(s')$ is one of $T_L(s')$, $T_\pi(s')$, and $T_T(s')$.

Now, an index of the error of the lumped circuit models should be settled to discuss the approximation error quantitatively. A relative error of a minimum pole (REMP) is chosen for this index in this paper. Concretely,

$$\text{REMP} = \frac{(\sigma_1 \text{ of a lumped circuit})}{(\sigma_1 \text{ of a distributed } CR \text{ line})} - 1. \tag{15}$$

In the present instances, σ_1 is quite separated from σ_2, so that it is considered as a time constant of the ladder circuit. Since the delay is proportional to the inverse of a time constant, the REMP is almost equal to the relative error of the delay $(t_{0.9})$ and this situation is assured in Figs. 6-8. Because the REMP is relatively easy to calculate, it is suitable for estimating an accuracy of a model when voltage time response is of interest.

The dependency of the REMP on n is shown in Fig. 7(a). As seen from Figs. 6 and 7(a), the widely used L ladder model is a poor approximation. The REMP amounts to as much as 30 percent, even when three ladder steps are connected. On the other hand, π and T ladder models are satisfactory. It should be noted that the accuracy of the models is improved as n increases, but it saturates at about three or four ladder steps.

TABLE I
REMP OF THREE-STEP π LADDER MODEL ($P3$)

C_T \ R_T	0	0.01	0.1	1	2
0	2.3	2.1	1.2	-.3	-.3
0.01	2.3	2.1	1.2	-.3	-.3
0.1	2.2	2.1	1.3	-.2	-.2
1	1.2	1.1	.9	.1	.0
2	.7	.7	.6	.1	.0

1: Errors are in percent. 2: Negative (positive) value corresponds to under- (over-) estimation of the delay.

When C_T or R_T has a finite value, the response becomes slower and the approximation becomes better, as shown in Figs. 7(b) and 8 and Tables I and II. These results are calculated using (B8)-(B13) in Appendix B. This improvement is naturally understood because the load capacitance and the resistance at the input can be replaced by exact models and the effects of these external circuit elements become eminent as C_T and R_T increase.

For finite C_T and R_T, too, the L ladder model is much worse than π and T models. Although π and T models have one more circuit element than the L ladder, the improvement obtained by this addition is worth the cost.

The REMP of C preceding L circuit (see $CPL1$ in Fig. 1) is also calculated. The result is that this $CPL1$ is much worse than the normal L circuit ($L1$) and should not be used in any case.

B. Recommended Circuit

It is pointed out in the previous section that the REMP of either the three-step π or T ladder circuit is less than 3 percent,

TABLE II
REMP OF THREE-STEP T LADDER MODEL ($T3$)

C_T \ R_T	0	0.01	0.1	1	2
0	2.3	2.3	2.2	1.2	.7
0.01	2.1	2.1	2.1	1.1	.7
0.1	1.2	1.2	1.3	.9	.6
1	-.3	-.3	-.2	.1	.1
2	-.3	-.3	-.2	.0	.0

1: Errors are in percent. 2: Negative (positive) value corresponds to under- (over-) estimation of the delay.

TABLE III
RECOMMENDED LUMPED CIRCUIT TO SIMULATE DISTRIBUTED CR LINE WHEN 10 PERCENT ERROR IS ADMITTED

C_T \ R_T	0	.01	.1	.2	.5	1	2	5	10	20	50	100
0	P2	P2	P2	P1	P1	P1	P1	C	C	C	C	C
.01	P2	P2	P2	P1	P1	P1	P1	C	C	C	C	C
.1	P2	P2	P2	P1	P1	P1	P1	C	C	C	C	C
.2	T1	T1	T1	P1	P1	P1	P1	C	C	C	C	C
.5	T1	T1	T1	P1	P1	P1	P1	C	C	C	C	C
1	P1	P1	P1	P1	P1	P1	P1	L1	C	C	C	C
2	P1	P1	P1	P1	P1	P1	L1	L1	C	C	C	C
5	R	R	R	R	R	L1	L1	L1	C	C	C	C
10	R	R	R	R	R	R	R	R	C	C	C	C
20	R	R	R	R	R	R	R	R	C	C	N	N
50	R	R	R	R	R	R	R	R	C	N	N	N
100	R	R	R	R	R	R	R	R	C	N	N	N

Circuit types are abbreviated according to Fig. 1.

TABLE IV
RECOMMENDED LUMPED CIRCUIT TO SIMULATE DISTRIBUTED CR LINE WHEN 3 PERCENT ERROR IS ADMITTED

C_T \ R_T	0	.01	.1	.2	.5	1	2	5	10	20	50	100
0	P3	P3	P2	P2	P1	P1	P1	P1	P1	C	C	C
.01	P3	P3	P2	P2	P1	P1	P1	P1	P1	C	C	C
.1	T2	T2	P2	P2	P1	P1	P1	P1	P1	C	C	C
.2	T2	T2	P2	P2	P1	P1	P1	P1	P1	C	C	C
.5	T1	T1	T1	T1	P1	P1	P1	P1	P1	C	C	C
1	T1	T1	T1	T1	P1	P1	P1	P1	P1	C	C	C
2	T1	T1	T1	T1	P1	P1	P1	P1	L1	L1	C	C
5	P1	P1	P1	P1	P1	P1	P1	L1	L1	L1	C	C
10	P1	P1	P1	P1	P1	P1	L1	L1	L1	L1	C	C
20	R	R	R	R	R	R	L1	L1	L1	L1	C	C
50	R	R	R	R	R	R	R	R	R	R	C	N
100	R	R	R	R	R	R	R	R	R	R	N	N

Circuit types are abbreviated according to Fig. 1.

but it is not practical to employ this circuit for all of the wiring in an LSI design. In order to reduce computation cost, the simplest lumped circuit that approximates the wiring within a tolerant error is recommended. Since the simplest circuit depends on C_T and R_T, they are tabulated in Tables III and IV for the tolerant error of 10 percent and 3 percent, respectively. The value of the equivalent resistance r_t is between 1/(maximum drain conductance) and 1/(minimum drain conductance). Since the approximation gets better as r_t/R increases, the safer choice is (1/maximum drain conductance). In these tables, a π ladder circuit is chosen when both π and T ladders are candidates. This is because the computational time of the circuit simulator programs strongly depends on the number of nodes included in the circuit and the T ladder always has one more node than the π ladder. It is to be emphasized that these recommended circuits are not confined

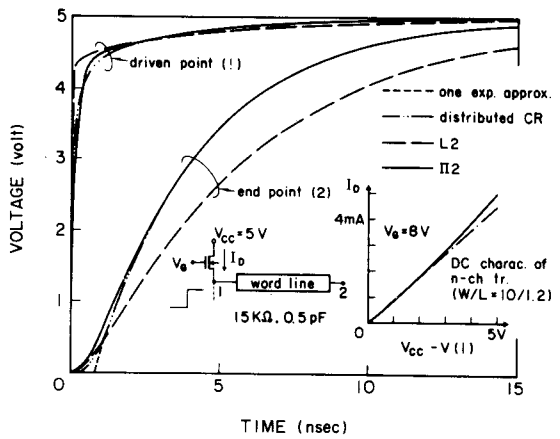

Fig. 9. Step response of a word line in n-channel dynamic memories together with dc characteristics of drive MOSFET. Approximation by $P2$ is excellent, while $L2$ cannot reproduce the correct response. The line denoted by one exp. approx. is calculated by simple formula (7). Dash-dot line in the figure represents dc characteristics of r_t whose value is chosen to fit $t_{0.9}$ to the correct response.

only to the step voltage input case because the REMP does not depend on the input waveform.

As seen from Table IV, a wiring can be replaced by only one capacitance if r_t/R is greater than 50. This condition is met in ordinary aluminum wires for MOS LSI, and thus the validity of widely used one capacitance approximation is appropriate.

V. APPLICATIONS TO WORD LINE DELAY ANALYSIS

Figs. 9 and 10 are two examples of the word line delay analysis. Simulation is carried out by SPICE, assuming LSI memory design of next generation. Fig. 9 is for a word line in an n-channel memory where the gate of the word line drive MOSFET is bootstrapped as in a dynamic LSI memory design. Fig. 10 is for CMOS memory where word lines are driven by a p-channel MOSFET. I_D versus V_{DS} plots of the drive MOSFET's are also shown in these figures. The transistor model is MOS3 of SPICE and includes the short channel effect, the back-gate bias effect, and mobility saturation, whose parameters are fitted to real devices.

Dash-dot lines in the figures show the characteristics of the equivalent resistance r_t, the value of which is chosen to fit the calculated word line delay $t_{0.9}$ by (9) with the simulation. For an n-channel drive MOSFET the drain current I_D depends on V_{DS} nearly linearly, so that it is easy to obtain the value of r_t.

For a p-channel drive MOSFET, r_t is near the value of 1/(maximum drain conductance). This is because the drive MOSFET is operated in a triode region most of the time, as seen from the voltage response of point 1 in Fig. 10. r_t should be chosen as 1/(average drain conductance of triode region). However, it is difficult to calculate this value exactly. An easier choice is 1/(maximum drain conductance), which is not bad according to the reasoning below. For the usual polysilicon word lines where the CR time constant of the word line limits the response speed the contribution of the term $2.21r_tC$ to $t_{0.9}$ is about 10-20 percent. In this case, 30 percent estimation error of r_t corresponds to 3-6 percent error of the total delay induced by the word line.

Broken lines in Figs. 9 and 10 show the calculated waveform

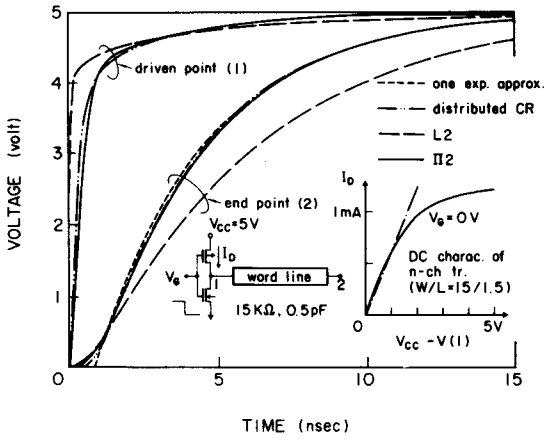

Fig. 10. Step response of a word line in CMOS memories together with dc characteristics of drive MOSFET. Discharging of a word line by an n-channel MOSFET is similar to this figure if the figure is read upside down.

by using the simple formula (7). They fit the simulated curves well.

Although only charging-up of word lines is discussed here, discharging of the line by an n-channel MOSFET is similar to the case of Fig. 10.

VI. Summary

An analytical approximation and a lumped circuit approximation for wiring delays in MOS LSI are studied. As a result, the following points are made.

1) The usually adopted L ladder circuit model is a poor approximation for a distributed CR line. The relative error of the delay is as much as 30 percent, even if three ladder steps are connected. On the other hand, the accuracy of π and T ladder models is satisfactory. Here, the relative error is less than 3 percent if $P3$ or $T3$ models are employed.

2) An approximation with ladder circuit models becomes better as c_t and r_t increase. For conventional word lines where $r_t \sim 0.1$, $P2$ is enough to achieve 3 percent error. The most difficult situation for approximation occurs when the distributed CR line is without any capacitive load and driven directly by a step voltage, namely $c_t = r_t = 0$. In any case, c_t and r_t play an important role in determining the wiring delay. The ladder circuit model coincides with a distributed CR line as a four-port linear network when infinite steps are connected. However, the simplest circuit that can simulate the distributed CR line within a given error should be employed in practical use. For this point of view, the recommended circuits are tabulated in Tables III and IV under various drive and load conditions.

3) If r_t/R is greater than 50, a distributed CR line can be approximated with only one capacitance within 3 percent error. This assures the validity of widely used one-capacitance approximation since the condition $r_t/R > 100$ is usually met in aluminum wiring.

4) The minimum pole of the transfer function dominates a global shape of voltage response of a distributed CR line. Consequently, one exponential term is sufficient to reproduce the step response [see (7)]. The wiring delay $t_{0.9}$ can

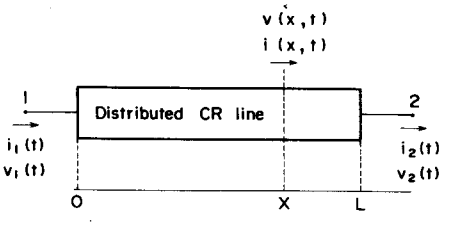

Fig. 11. Dividing the distributed CR line into two parts.

be calculated as

$$t_{0.9} = 1.02CR + 2.21(c_t r_t + c_t R + r_t C).$$

The relative error of this simple formula is less than 1.1 percent for C_T, $R_T < 1$ and 4 percent for the entire range of parameters. These formulas will provide useful tools in estimating the behavior of word lines in MOS LSI.

Appendix A
Current and Voltage Response for Step Voltage Excitation in the Case of $C_T = R_T = 0$

Exact time-domain solutions at the end of a distributed CR line with short, open, and characteristic impedance temination is presented by Peirson [7]. Here, the time-domain solution for an arbitrary position of the line is given only for completion. First, a distributed CR line is divided into two parts at x, as is shown in Fig. 11. Under the condition that $I_2(s') = 0$ ($C_T = 0$), the following equation holds (see Appendix B):

$$V_0(s) = \cosh(\sqrt{sCR})\, V_2(s), \tag{A1}$$

$$V(x,s) = \cosh\sqrt{sCR\left(1-\frac{x}{L}\right)^2}\cdot V_2(s). \tag{A2}$$

Assuming that point 1 is excited by step voltage from zero to v_{cc}, that is,

$$V_0(s) = \frac{v_{cc}}{s}, \tag{A3}$$

the following expression for $V(x,s)$ is obtained by (A1-A3):

$$V(x,s) = \frac{v_{cc}}{s}\cdot\frac{\cosh\left\{\sqrt{sCR}\left(1-\frac{x}{L}\right)\right\}}{\cosh\sqrt{sCR}}. \tag{A4}$$

The inverse Laplace transformation of (A4) yields [8]

$$\frac{v(x,t)}{v_{cc}} = 1 + \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^k}{k-\frac{1}{2}}\cos\left[\left(k-\frac{1}{2}\right)\pi\left(1-\frac{x}{L}\right)\right] \cdot e^{-(k-1/2)^2\pi^2(t/CR)}. \tag{A5}$$

The current $i(x,t)$ is calculated as

$$i(x,t)\Big/\left(\frac{v_{cc}}{R}\right) = 2\sum_{k=1}^{\infty}(-1)^{k-1}\sin\left[\left(k-\frac{1}{2}\right)\pi\left(1-\frac{x}{L}\right)\right] \cdot e^{-(k-1/2)^2\pi^2(t/CR)}. \tag{A6}$$

This can be obtained by differentiating (A5), and by using

$$\frac{\partial v(x,t)}{\partial x} = -r\cdot i(x,t). \tag{A7}$$

Appendix B
Derivation of Transfer Functions

Transfer functions of π, T, L ladder circuits and a distributed CR line are derived in this order. The fundamental matrix F_1 for a unit block of an n-step π and T ladder circuit is expressed as [9]

$$F_1 = \begin{bmatrix} \cosh(g) & Z_0 \sinh(g) \\ Z_0^{-1} \sinh(g) & \cosh(g) \end{bmatrix} \tag{B1}$$

where

$$\tanh(g) = \sqrt{\frac{s'}{n^2}\left(1+\frac{s'}{4n^2}\right)} \Big/ \left(1+\frac{s'}{2n^2}\right), \tag{B2}$$

$$Z_0 = \frac{1}{C\sqrt{s'}\sqrt{1+\frac{s'}{4n^2}}}, \quad \text{(for } \pi \text{ ladder)} \tag{B3}$$

$$= \frac{1}{C\sqrt{s'}}\sqrt{1+\frac{s'}{4n^2}} \quad \text{(for } T \text{ ladder).} \tag{B4}$$

Since the total ladder circuit is created by concatenating the unit block n times, the fundamental matrix F_n for total the π and T ladder circuit is

$$F_n = (F_1)^n = \begin{bmatrix} \cosh(ng) & Z_0 \sinh(ng) \\ Z_0^{-1} \sinh(ng) & \cosh(ng) \end{bmatrix}. \tag{B5}$$

When resistance r_t and capacitance c_t are added to the ladder circuits as shown in Fig. 12, the following equations hold:

$$\begin{bmatrix} V_0(s') \\ I_0(s') \end{bmatrix} = \begin{bmatrix} 1 & r_t \\ 0 & 1 \end{bmatrix} F_n \begin{bmatrix} V_2(s') \\ I_2(s') \end{bmatrix}, \tag{B6}$$

$$I_2(s') = s' c_t V_2(s'). \tag{B7}$$

Then, the transfer function $T(s')$ from point 0 to point 2 in Fig. 12 is written as

$$T(s') = \frac{V_2(s')}{V_0(s')} = \frac{1}{(1+s'C_TR_T)\cos(n\zeta) - \left(\frac{R_T}{\varphi}+C_T\varphi\right)\sqrt{-s'}\sin(n\zeta)} \tag{B8}$$

where

$$\tan\zeta = \sqrt{-\frac{s'}{n^2}\left(1+\frac{s'}{4n^2}\right)} \Big/ \left(1+\frac{s'}{2n^2}\right), \tag{B9}$$

$$\varphi = 1 \Big/ \sqrt{1+\frac{s'}{4n^2}}, \quad \text{(for } \pi \text{ ladder)} \tag{B10}$$

$$= \sqrt{1+\frac{s'}{4n^2}} \quad \text{(for } T \text{ ladder).} \tag{B11}$$

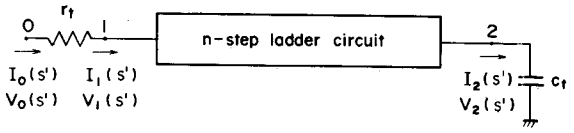

Fig. 12. Capacitance c_t and resistance r_t are connected to either the L, π, or T ladder circuit.

It is difficult to obtain the counterpart of (B8) for the L ladder circuit. However, when $c_t = 0$, a transfer function of the L ladder circuit happens to be equal to that of the T ladder circuit with a resistance $R/2n$ added at the input. Substituting R_T by $R_T + \frac{1}{2}n$ and setting C_T zero in (B8) leads to

$$T_L(s') = \frac{1}{\cos(n\zeta) - \frac{1}{\varphi_L}\left(R_T+\frac{1}{2n}\right)\sqrt{-s'}\sin(n\zeta)} \tag{B12}$$

where

$$\varphi_L = \sqrt{1+\frac{s'}{4n^2}}. \tag{B13}$$

For a one-step L circuit, the transfer function is easily obtained as

$$T_{L1}(s') = \frac{1}{s'+(1+C_T)(1+R_T)}. \tag{B14}$$

It is obvious that π, T, and L ladder circuits coincide with a distributed CR line if infinite blocks are connected. This can be readily confirmed by starting from the partial differential equations which describe the line and Laplace transforming them. n tending to infinity in (B2) and (B3), we have

$$\lim_{n\to\infty} ng = \sqrt{s'} \tag{B15}$$

$$Z_0 = \frac{1}{C\sqrt{s'}}. \tag{B16}$$

Equation (1) is obtained, substituting the relation (B15) for (B8).

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