[See page 340 for Figure 1.]

SESSION XV: STATIC RAMs

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THPM 15.1: A 46ns 256K CMOS RAM

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DEMANDS FOR HIGH DENSITY, high speed and low power dissipation are increasing with recent static RAMs. Actually, as storage capacity on a chip increases, reduction in delay time and power consumption within the core area, i.e., word line, bit line and sensing circuit delays, becomes vitally important to meet the requirements. This paper will describe an asynchronous, 256Kb CMOS static RAM, which utilizes a double word line technique[1,2], automatic power down function, and internally clocked circuitry.

The chip microphotograph and the typical characteristics are shown in Figure 1 and Table 1. The row decoder is placed on the left side of the memory arrays. The cell size is 11 x 13.5μm, and the chip measures 6.68 x 8.86mm, which fits into a standard 28pin DIP. The RAM offers typically 46ns access time, 10mW operating power, and 30μW standby power.

For achieving high packing density and improved performance with this sub-micron channel length VLSI memory chip, a P-well-based double polysilicon CMOS technology has been developed[3], which includes a narrow field isolation, and LDD-type transistors for 5V operation. A 1.2μm ground rule was employed for highest density regions. Table 2 lists the design rules and device parameters, in comparison with the preceding generation device[4]. Double level Al structure is characterized by a unique low temperature interlayer formation and planarization technique, combined with a hillock suppressed metal layer deposition.

The block diagram of the RAM is shown in Figure 2. Address transition detector circuits are employed to generate internal clocks, such as chip activating pulses and an automatic power down pulse. The chip activating pulses are used to equalize bit lines and data lines, and also to activate word line drivers and sense amplifiers. The automatic power down pulse is generated after the read out operation. The pulse deselects word line drivers and sense amplifiers, so that no dc current flows other than standby current. Therefore, the active power is drastically reduced at low operating frequencies, as shown in Figure 3.

To reduce both the word line delay and the active power dissipation, a double word line structure is introduced. Row lines consist of aluminum main word lines which select one of 512 rows, and polysilicon section word lines which activate one of 16 sections. The section word line is activated by the main word line and a column select signal. Since only 32 memory cells connected to one section word line are accessed in a cycle, column current flows only in a selected section. In addition, an RC time delay of each section word line is reduced to 1/256 compared with conventional arrangements. Therefore, the total word line delay is reduced to 8.5ns from 30ns as is the case of conventional 4 block word line configurations. The circuit design is realized by utilizing double aluminum structure.

A schematic diagram of a memory cell and peripheral circuits is illustrated in Figure 4. A two-stage current mirror type CMOS sense amplifier is used to achieve high-speed read operation. The first stage amplifies a small signal from one of the four bit line pairs. The second stage amplifies the first stage output signal to a large swing level.

The bit lines and the first sense amplifier output are equalized by the chip activating pulse before the read operation.

To improve fabrication yield, a redundancy circuit is employed without any speed degradation.

The oscillograph of the address input and data output signal waveforms at Vdd=5V with 100pF load capacitance is shown in Figure 5, which indicates a 46ns address access time.

Acknowledgments

The authors wish to thank Y. Nishi and Y. Uchida for their continuous support and encouragement, and H. Kaneko and K. Sato for their great efforts in processing and evaluations.

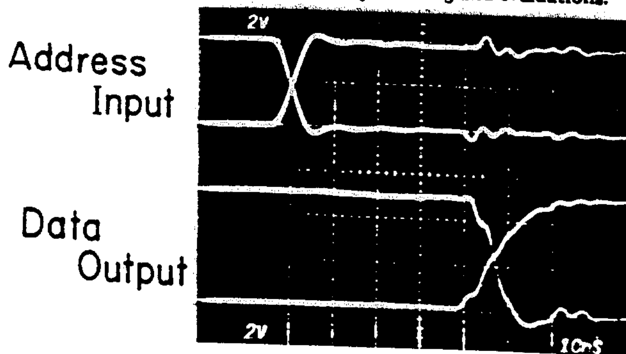

FIGURE 5—Oscillograph of address input and data output waveforms.

[Right]
FIGURE 2—Block diagram of the 256Kb CMOS RAM.

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[1]Sakurai, T., et. al., "Methods for Analyzing a Word Line Delay and Their Applications". *The Community of Solid-State Devices of IECE of Japan*, SSD82-72, p. 15-21; Oct., 1982.

[2]Yoshimoto, M., et. al., "A 64Kb Full CMOS RAM with Divided Word Line Structure", ISSCC DIGEST OF TECHNICAL PAPERS, p. 58-59; Feb., 1983.

[3]Matsunaga, J., et. al., "1.2μm Process Design for CMOS VLSI's", *Electrochem, Soc. Meeting*, San Francisco, Extended Abstracts 83-1, p. 566; May, 1983.

[4]Konishi, S., et. al., "A 64Kb CMOS RAM", ISSCC DIGEST OF TECHNICAL PAPERS, p. 258-259; Feb., 1982.

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PARAMETERS	64K-CMOS RAM	256K-CMOS RAM
PROCESS	DOUBLE-LEVEL POLY-Si SINGLE-LEVEL Al	DOUBLE-LEVEL POLY-Si DOUBLE-LEVEL Al
GATE LENGTH (NMOS)	2.0 μm	1.2 μm
(PMOS)	2.2 μm	1.5 μm
GATE OXIDE THICKNESS	450Å	250Å
JUNCTION DEPTH (N^+)	0.25μm	0.20μm
(P^+)	0.5 μm	0.35μm
POLY-Si (WIDTH/SPACING)	2μm/2μm	1.2μm/1.2μm
1st Al (WIDTH/SPACING)	2μm/2μm	1.2μm/1.6μm
1st CONTACT HOLE	2μm×2μm	1.2μm×1.2μm
2nd Al (WIDTH SPACING)	—	2.0μm/2.0μm
2nd CONTACT HOLE	—	2.0μm×2.0μm

TABLE 2

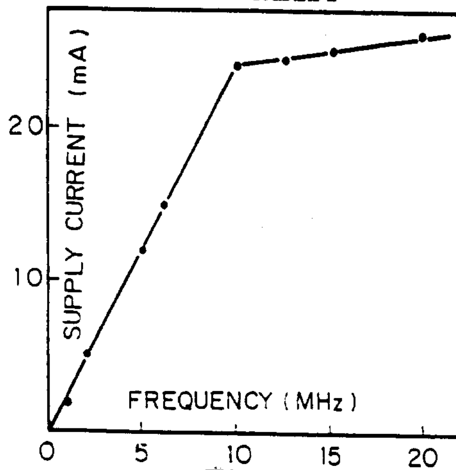
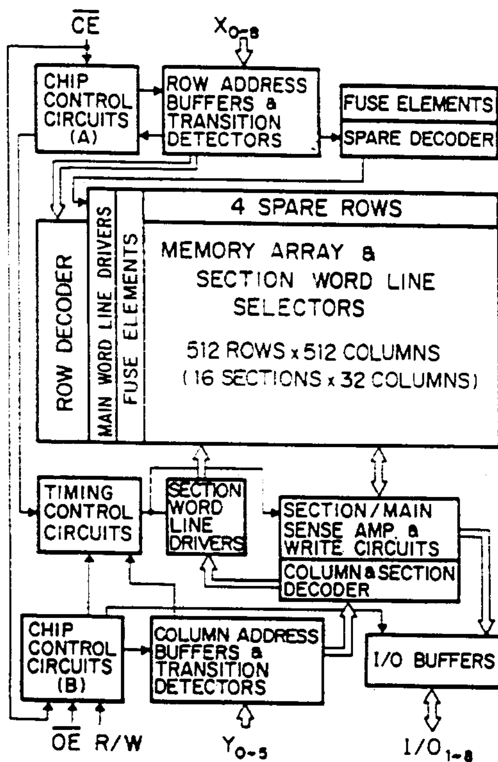


FIGURE 3



OPERATION	FULLY ASYNCHRONOUS (ADDRESS ACTIVATED CLOCKED OPERATION) AUTO POWER DOWN FUNCTION
ORGANIZATION	32K WORDS x 8BIT
REDUNDANCY	4 SPARE ROWS
CHIP SIZE	6.68 x 8.86 mm
CELL SIZE	11 x 13.5μm
I/O INTERFACE	TTL COMPATIBLE
ADDRESS ACCESS TIME	46 ns
ACTIVE POWER	10 mW (1MHz)
STANDBY POWER	30 μW
PACKAGE	STANDARD 28PIN DIP

TABLE 1—Typical characteristics of the 256Kb CMOS RAM.

[Left/Top]

TABLE 2—Design rules and device parameters of the 256Kb CMOS RAM.

[Left]

FIGURE 3—Supply current versus operating frequencies.

[Below]

FIGURE 4—Schematic of memory cell and peripheral circuits.