# A LOW POWER 46 ns 256 kbit CMOS STATIC RAM WITIH DYNAMIC DOUBLE WORD LINE

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# A Low Power 46 ns 256 kbit CMOS Static RAM with Dynamic Double Word Line

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*Abstract*—**A fast and low power 32K×8 bit CMOS static RAM with high-resistive polyload 4-transistor cell is developed utilizing a dynamic double word line (DDWL) scheme, a combination of automatic power down (APD) circuitry, and double word line (DWL) structure. The DDWL, together with bit line and sense line equilibration reduces the core area delay time and operating power to about 1/2 and 1/15 that of a conventional device, respectively. A newly developed fault-tolerant circuitry improves fabrication yield without degrading the access time. As for a fabrication process, an advanced 1.2 μm p-well CMOS technology is developed to realize the ULSI RAM, integrating 1.6 million elements on a 6.68×8.86 mm² chip. The RAM offers, typically, 46 ns access time, 10 mW operating, and 30 μW standby power.**

## I. INTRODUCTION

THE memory capacity of CMOS static RAM's has been quadrupled every two years during the last four generations. This rate of increase is faster than dynamic RAM's. In 1982 64 kbit CMOS static RAM's (C/SRAM's) were announced [1]–[3], and in this paper a 256 kbit CMOS static RAM with high-resistive polyload 4-transistor cells is reported, a herald of a ULSI's (ultra large scale integrations), including 1.6 million elements on a chip.

The advantages of a CMOS static RAM over a dynamic RAM lie in its high speed, low power, and highly reliable operation, without any complex refresh controls. These salient features of CMOS static RAM's are positively pursued in this 256 kbit C/SRAM, resulting in 46 ns access time and 10 mW power dissipation at 1 MHz.

Key technologies for realizing the high performance C/SRAM are summarized in Table I, from the standpoint of both circuitry and processing. In the table, the purpose and effects are made clear.

The fast and low power operation is achieved by using a unique word line scheme, called dynamic double word line (DDWL). The DDWL is a combination of a double word line (DWL) structure [4]–[6] and an automatic power down (APD) scheme. In order to implement the APD function, a word line is activated dynamically by a pulse wider than the access time. The DDWL cuts down the operating power at 1 MHz to about 1/15 that of a conventional device. Address transition detectors (ATD's) [1] are incorporated in the RAM to generate the activation pulse for the APD function. This ATD also provides a means for equilibration of bit lines (BL's) and sense lines (SL's), which turn out to be very effective in realizing a fast access time. The equilibration circuitry, together with the DDWL scheme, reduces the access time to about one-half, compared with a conventional RAM. As for yield optimization, a new redundancy circuitry has been proposed which does not sacrifice the fast access time.

An advanced 1.2 μm p-well CMOS process with double polysilicon and double aluminum was developed to integrate 1.6 million elements on a chip of reasonable size, with a cell size of 11×13.5 μm². The high packing density of this level is achieved with the help of bird's beak free C-SEPOX (CMOS selective polysilicon oxidation) isolation technology [7]. Since peripheral circuitry speeds up as the supply voltage increases, 5 V operation is preferred over lower voltages for high speed operation. Reliable 5 V operation of submicron channel length MOSFET's was demonstrated by using an LDD (lightly doped drain)

TABLE I
KEY TECHNOLOGIES FOR HIGH SPEED AND LOW POWER 1.6 MILLION ELEMENT ULSI RAM

| TECHNOLOGY | PURPOSE: HIGH SPEED | PURPOSE: LOW POWER |
|---|---|---|
| 1. Double Word Line Structure<br>Double Metal<br>16 Sections | Y | Y |
| 2. Automatic Power Down Function<br>ATD Circuitry<br>Word Line Pulse Wider than Access Time | | Y |
| 3. BL and SL Equilibration<br>ATD Circuitry | Y | |
| 4. Reliable 5V 1.2um Device Process<br>C-SEPOX Isolation<br>SEPOS LDD | Y | |

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structure fabricated by SEPOS (self-defined polysilicon sidewall structure) process [8].

In Sections II and III, the process and circuit technologies are described in detail. Resulted performances and other features of the 256 kbit C/SRAM are treated in Section IV. Section V concludes the paper.

## II. 1.2 $\mu$m CMOS Process Technology

An advanced 1.2 $\mu$m p-well CMOS process is developed to fabricate the RAM. A p-well process, where all memory cells are embedded in the well, is chosen to mitigate soft errors. The potential barrier of the p-well reflects the long-term drift component of alpha-particle induced current. For a short-term drift component, so-called funneling, an *RC* time-constant isolation technique can be effective [9]. The cell layout technique also reduces the soft error rate associated with the drift component [10].

Design rules of the 256 kbit C/SRAM are listed in Table II, where comparison with the previous generation 64 kbit C/SRAM [1] are made. 1.5 $\mu$m $n^+$–$n^+$ spacing is achieved by using bird's beak free C-SEPOX isolation technology, the details of which are reported in [7]. As seen from the table, the effective channel length of an n-channel MOSFET is 0.8 $\mu$m. A conventional n-channel MOSFET of this submicron channel region suffers from the notorious hot carrier problem. A newly developed SEPOS LDD process [8] has been successfully applied to make reliable submicron MOSFET's for 5 V operation. The SEPOS process offers better controllability and wider margins and results in very small degradation of drain conductivity with respect to conventional transistors. The reliable 5 V operation of submicron MOSFET's, together with double-metal interconnects, which decrease *RC* delay of word lines and jumper lines, are indispensable for a fast circuit operation.

The double-level polysilicon process has a small chip size, which contributes not only to higher gross productivity but also to reduction of parasitic capacitance. The first level poly layer is used for the gates of MOSFET's, while the second layer, whose sheet resistivity is over 100 G$\Omega/\square$, serves as the high-resistive polyloads for the memory cells, realizing a low standby power of 30 $\mu$W and enabling battery backup of stored data. The second layer is also used for $V_{dd}$ supply lines for memory cells, where the sheet resistivity is lowered to less than 50 $\Omega/\square$ through a selective doping.

## III. Circuit Design

Fig. 1 shows the trend of delay components in scaled-down C/SRAM's. As seen from the figure, the core area delay time, namely WL, BL, and SL delay, dominates the access time. This is basically because the peripheral circuitry speeds up by the scaling, but the capacitance of bus lines cannot be scaled since the number of memory cells for one bus line is doubled. Some remedies should be used to achieve high speed operation of scaled C/SRAM's. Our solutions are DWL structure for WL delay, and equilibration for BL and SL delay, which will be discussed in Sections III-A and III-D.

TABLE II
Design Rules of 64 and 256 kbit CMOS Static RAM

| PARAMETERS | 64K-CMOS RAM | 256K-CMOS RAM |
|---|---|---|
| PROCESS | DOUBLE-LEVEL POLY-Si SINGLE-LEVEL Al | DOUBLE-LEVEL POLY-Si DOUBLE-LEVEL Al |
| GATE LENGTH (NMOS) | 2.0 $\mu$m | 1.2 $\mu$m |
| GATE LENGTH (PMOS) | 2.2 $\mu$m | 1.5 $\mu$m |
| GATE OXIDE THICKNESS | 450 Å | 250 Å |
| JUNCTION DEPTH ($N^+$) | 0.25 $\mu$m | 0.20 $\mu$m |
| JUNCTION DEPTH ($P^+$) | 0.50 $\mu$m | 0.35 $\mu$m |
| DIFFUSION (WIDTH/SPACING) | 1.6 $\mu$m/2.6 $\mu$m | 1.2 $\mu$m/1.5 $\mu$m |
| POLY-Si (WIDTH/SPACING) | 2 $\mu$m/2 $\mu$m | 1.2 $\mu$m/1.2 $\mu$m |
| 1st Al (WIDTH/SPACING) | 2 $\mu$m/2 $\mu$m | 1.2 $\mu$m/1.6 $\mu$m |
| 1st CONTACT HOLE | 2 $\mu$m/2 $\mu$m | 1.2 $\mu$m×1.2 $\mu$m |
| 2nd Al (WIDTH/SPACING) | —— | 2.0 $\mu$m/2.0 $\mu$m |
| 2nd CONTACT HOLE | —— | 2.0 $\mu$m×2.0 $\mu$m |

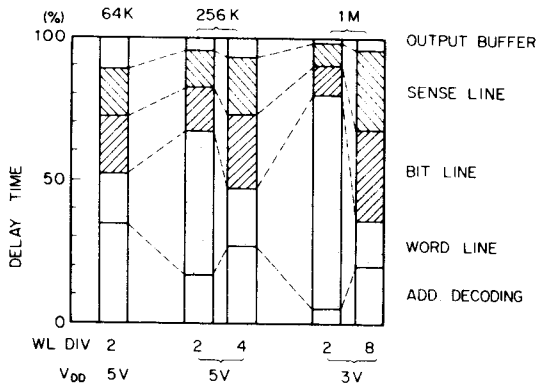


Fig. 1. Trends of delay component in scaled-down C/SRAM's. The trends are calculated by assuming a simple scaling law with a fit at 64 kbit C/SRAM. Mobility degradation due to the scaling is obtained from measured data of up to 0.8 $\mu$m MOSFET's. Two-dimensional effects are taken into account in estimating capacitances [11]. Output capacitance is set to zero because it depends on the external circumstances.

The scaled RAM also suffers from large power dissipation because the number of the activated cells have been doubled, if simple shrinkage is adopted. The DDWL is one of the solutions for this problem. As for a yield problem, a new redundancy circuitry is devised, which is treated in Section III-E.

### A. Double Word Line Structure

The basic configuration of DDWL is shown in Fig. 2. Word lines are doubly placed, namely main word lines (MWL's) and section word lines (SWL's) [4]–[6]. Since an MWL is not directly connected to memory cells, capacitance of the MWL is relatively small, reducing the WL delay. The MWL is made by the second aluminum layer, which also reduces the delay. Low power dissipation is expected because only one SWL is selected at a time, and consequently only a small number of memory cells are activated. From a viewpoint of delay time and power dissipation, the greater the number of sections, the better the performance is. However, the chip area of the SWL

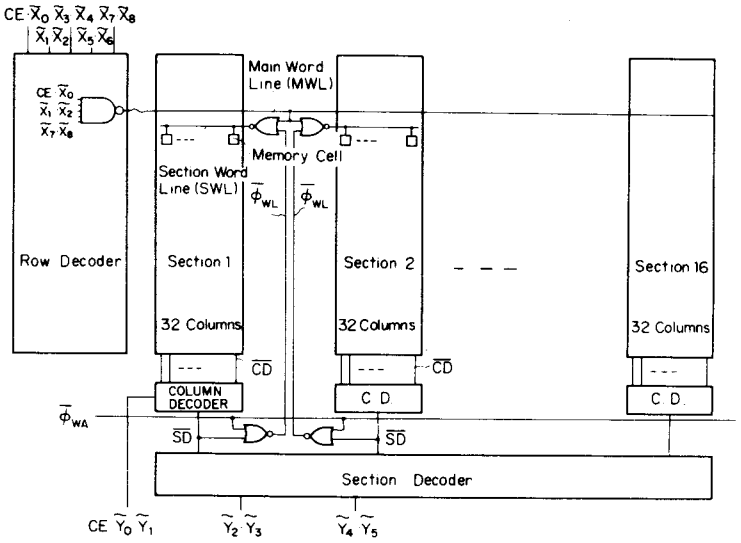


Fig. 2. Basic configuration of the dynamic double word line (DDWL) scheme.

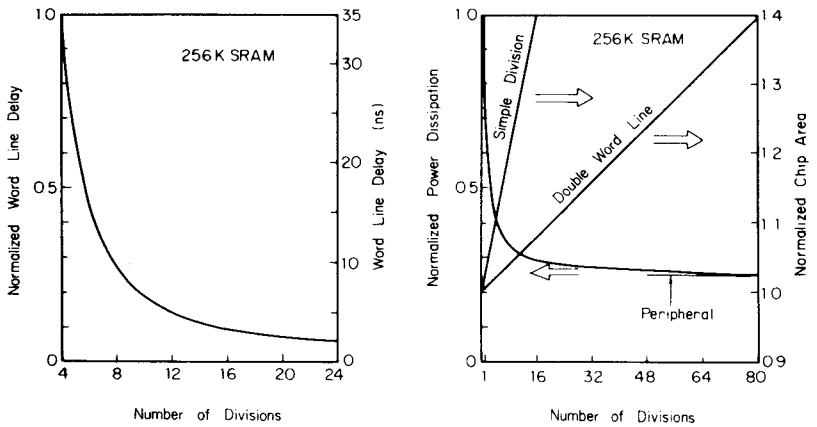


Fig. 3. Tradeoff among delay, power, and area for double word line structure. Step voltage is incident at a word line drive point. Section word line delay is estimated by using 3-step pi ladder circuit, which turned out to be the best circuit to simulate *RC* lines [14].

select NOR circuits, taking 2.5 cell areas each, increases linearly as the number of sections increases. Therefore, the number of sections cannot be set too large, although the area overhead is much smaller than a simple division of WL's, where many row decoders are required. This tradeoff is illustrated in Fig. 3. In the present device, the number of sections chosen is 16, where the delay and power improvement are saturated. At this point, the delay and power reduction are about 30 ns and 30 percent, respectively, with the chip area being the same, compared with the 4-divided conventional poly-WL structure.

Predecoding of address signals [12] is also effective in reducing the access time.

### *B. Automatic Power Down Function*

A rough sketch of internal waveforms and a schematic diagram of a core part are shown in Fig. 4. When an address changes, address transition detectors (ATD's) create two classes of clocks, namely equilibration clocks and activation clocks. The equilibration clocks ($\phi_{BE}$ and $\phi_{ME}$) are explained in Section III-D. The activation clocks consist of sense amplifier activation clocks ($\phi_{SA}$ and $\phi_{MA}$) and a word line activation clock ($\phi_{WA}$). The clock-controlled word lines are one of the main features of the DDWL scheme. These activation clocks have a pulse width wider than an access time, and control sense amplifiers and SWL's so as to cut all the dc path in the RAM after a read operation is over. Consequently, no dc power is consumed. This is the principle of the automatic power down (APD) function. Since the activation pulse width is set at about 100 ns, the supply current depends linearly on the operation frequency below 10 MHz, as shown in Fig. 5. The activation pulse should have a width of 1.5–2.0 times the access time in order to salvage the slowest bits and to improve yield. A typical operation frequency for low power portable systems, where battery operation is a must, is around 1 MHz. The operation power at 1 MHz is reduced to about 1/10 that of a conventional RAM through the action of the APD function only.

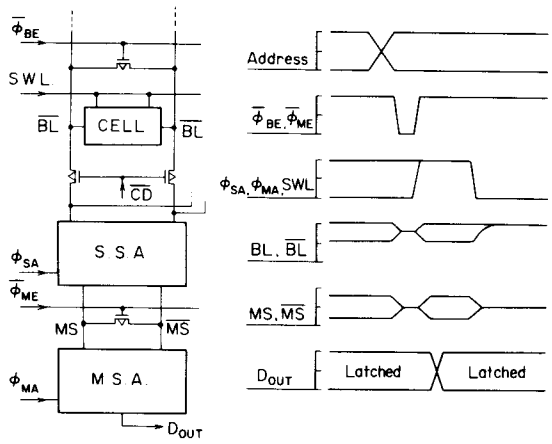


Fig. 4. A rough sketch of internal waveforms and a schematic diagram of a core part.

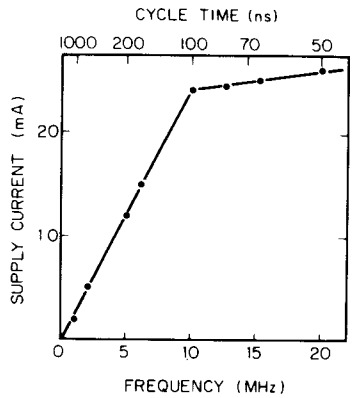


Fig. 5. Measured supply current versus operation frequency. Since the activation pulse width is set to about 100 ns, the supply current depends linearly on the operation frequency below 10 MHz. The measurement is carried out with no load and a supplied voltage of 5 V. The read cycle is repeated with output "1" and "0" alternated every cycle time.

### C. Sense Amplifiers and Double Sense Line Structure

The two-stage current-mirror sense amplifiers shown in Fig. 6 are used to realize fast sensing. In the case of a latch-type amplifier commonly used in dynamic RAM's, the timing of the latch clock is very critical. The latch timing should come after the slowest memory cell pushes out the stored information to bit lines, unless a malfunction should occur. However, if the latch timing is very late, it degrades the access time. In the current-mirror amplifier, which is essentially static, there is no tradeoff between clock timing and access time. That is, yield and access time are always optimized. Moreover, the relatively small voltage swing of the bit lines is indispensable for fast equilibration. It should be noted that, although the RAM is internally controlled by clocks, the timing variation of these clocks does not give rise to malfunctions of the device.

Corresponding to the DWL, hierarchical structure is also adopted for sense lines, namely section sense lines (SS's) and main sense lines (MS's). This double sense line structure reduces the capacitance of MS lines and as a result the sensing delay.

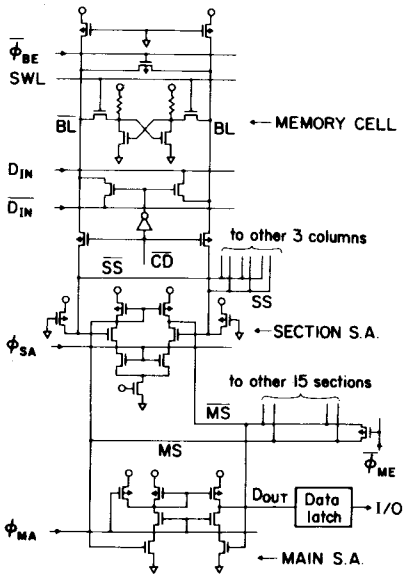


Fig. 6. Two-stage current-mirror sense amplifiers and double sense line structure.

### D. Equilibration Scheme

Before stored information is read out from memory cells, bit lines and sense lines are equilibrated by using the equilibration clocks $\phi_{BE}$ and $\phi_{ME}$ (see Figs. 4 and 6). The equilibration is done in parallel with address decoding, exerting no delay in the sensing operation [13]. Instead, 20 ns access time reduction by the equilibration is observed by a computer simulation. This is because considerable time is required to cancel the effect of previous data if there is no equilibration.

### E. Redundancy

Spare cells are widely included in VLSI RAM's [1]–[3] to improve fabrication yield. In 8 bit I/O RAM's, the spare row approach has more freedom in cell replacement and/or less overhead for redundancy circuitry than the spare column approach. Therefore the spare row approach is used in this RAM.

Simple calculation is carried out to determine the number of spare rows that optimizes the gross-yield product. Let $Y_0$ be the normalized initial yield. $Y_0$ is unity when all rows are safe. Then the probability that one row is safe ($P1$) is $Y_0^{(1/N)}$, where $N$ is the total number of normal rows ($N = 512$ for a 256 kbit C/SRAM). The normalized yield ($Y$) by using $S$ spare rows is the probability that at least $N$ rows are good in $(N + S)$ rows. $Y$ should be multiplied by a factor if column fault mode and peripheral fault mode are considered, but for spare row number optimization this factor can be omitted.

$$Y = \sum_{j=0}^{S} {}_{(N+S)}C_j \cdot P1^{(N+S-j)} \cdot (1 - P1)^j.$$

However, gross productivity decreases as $S$ increases due to overhead area consumed by redundancy circuits. To take this effect into account, $Y$ is multiplied by $1/(1 + v_1 \cdot$

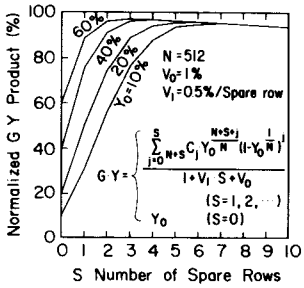


Fig. 7. Normalized gross-yield product versus number of spare rows. Four spare rows are adopted as optimum.

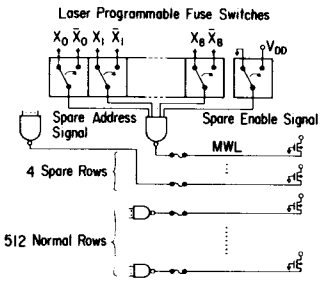


Fig. 8. Redundancy circuitry. The switches in the figure are constructed by using similar techniques as those in [1]. Disabling of a normal row is done not by an electrical signal but by blowing a fuse, which is good for the fast access time.

$S + v_0$), where $v_1$ stands for the overhead area factor to include one spare row and accompanying redundancy circuits, and $v_0$ for the overhead area factor to incorporate the redundancy scheme itself. The resulted expression for gross-yield product ($G \cdot Y$) is shown in Fig. 7, together with $G \cdot Y$ curves for this device. Consequently, four spare rows are chosen.

The new redundancy circuitry is shown in Fig. 8. When a spare row is selected, the corresponding normal row should be disabled. Conventionally, this disabling process is executed by an electrical signal. The signal is generated after deciding if an input address is one of the repaired addresses. This process is rather slow. Since the row selection should be done after the diselection, unless row multiselect should happen, a conventional redundancy scheme would degrade the access time. In the new circuit, the disabling is done by blowing off the poly fuse and no sacrifice of access time occurs. Moreover, if a replaced spare row malfunctions, then the spare row can be replaced again by another spare row.

## IV. Performance and Other Features

The internal waveforms of the RAM in read operation are shown in Fig. 9. The measured data are obtained by a strobo SEM tester. Voltage swings of BL and MS are fitted to computer-simulated values because the strobo SEM tester does not provide an absolute value of a node voltage but only a relative value. In the measurement, I/O pins are not loaded with an external capacitance and the suspected I/O voltage response for 100 pF output capacitance is indicated by a broken line. The waveforms of the clocks

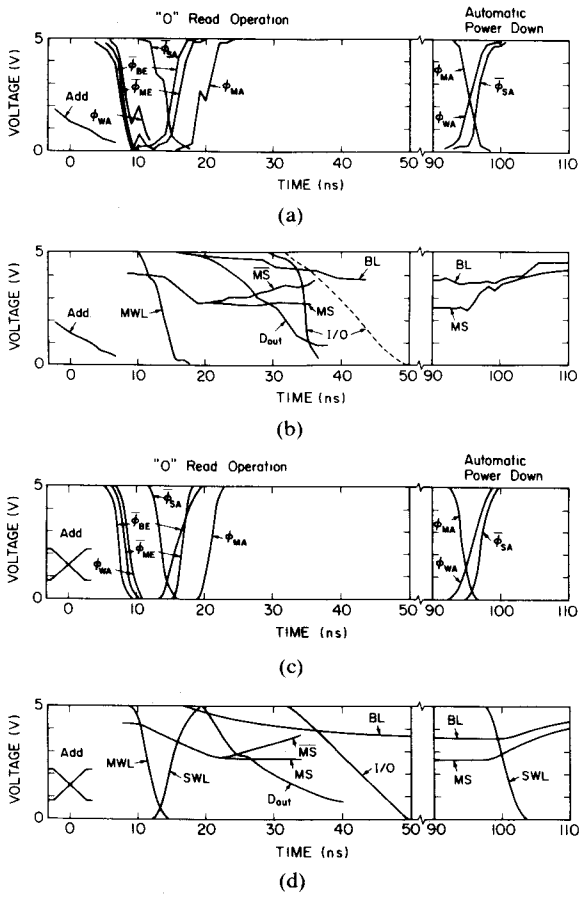


Fig. 9. Internal waveforms of the RAM. (a) Measured clocks. (b) Measured bus line signals. (c) Simulated clocks. (d) Simulated bus line signals. The measurement is carried out by a strobo SEM tester, which is a very useful tool for examining the debugging ULSI C/SRAM's. The simulation is done by SPICE2.

and bus lines are plotted in separate figures for easier reading. As seen from the figures, the power down function is initiated at about 95 ns after an address changes. As a whole, the measured waveforms are in good agreement with the simulation and the successful realization of the above-mentioned design concepts has been assured. This agreement also suggests the effectiveness of the SPICE2 circuit simulation program in ULSI CMOS RAM design. Fig. 10 is a Schmoo plot of the present device, showing 46 ns access time at 5 V.

Fig. 11 is a chip microphotograph. As seen from the photograph, the cell area occupies about 70 percent of the total chip. This high value of occupation is attributed to the 1.2 $\mu$m process, the DWL structure, and the laser blown fuse redundancy circuits. The white vertical lines in the cell area are the place where $\phi_{WL}$ lines are located.

The typical RAM characteristics are tabulated in Table III. The 256 kbit C/SRAM is internally clocked by the ATD, but fully asynchronous externally. So that no severe control of address skews is required, in contrast with dynamic RAM's where careful on-board design should be done for RAS and CAS timing.

I/O buffers are TTL compatible with three-state output. The package is a standard 600 mil 28 pin DIP and the pin

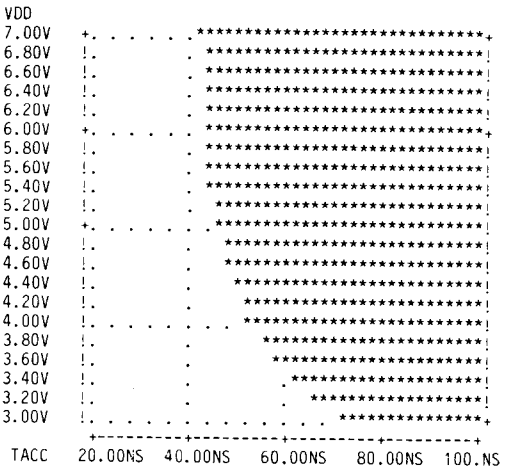


Fig. 10. Schmoo plot of the present device, showing 46 ns access time at 5 V.

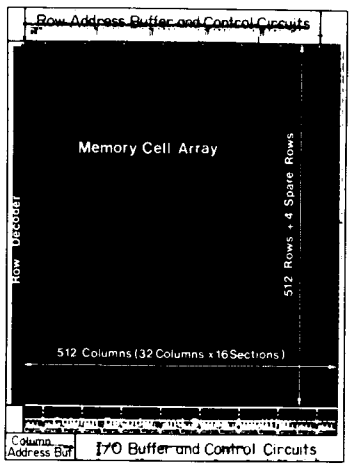


Fig. 11. Microphotograph of 256 kbit CMOS static RAM. The chip size is $6.68 \times 8.86$ mm$^2$.

configuration is shown in Fig. 12. This pin configuration is compatible to 64 kbit CMOS static RAM's.

## V. Conclusion

A fast and low power 32K×8 bit CMOS static RAM with high-resistive polyload memory cell has been developed. An advanced 1.2 $\mu$m p-well CMOS process with bird's beak free C-SEPOX isolation technology was applied for integrating 1.6 million elements on a $6.68 \times 8.86$ mm$^2$ chip. Double poly and double aluminum process contributes to the high packing density and fast circuit operation. The fast circuit operation is also supported by submicron channel length MOSFET's fabricated by SEPOS LDD process, which enables reliable 5 V operation.

As for the circuit design, the double word line (DWL) structure together with bit line and sense line equilibration, reduced the core area delay time drastically and a typical access time of 46 ns was achieved.

The dynamic double word line (DDWL) scheme, a combination of automatic power down (APD) circuitry and DWL structure was successfully applied to realize 10 mW at 1 MHz and 120 mW at 10 MHz operation. Considering the resulting high speed and low power operation of the 256 kbit C/SRAM, the DDWL scheme seems to be very promising for future ULSI memories, not only for static RAM's but also for ROM's, EPROM's, and EEPROM's.

Address transition detectors (ATD's) are incorporated in the RAM to generate equilibration and activation control clocks. The use of ATD's can be a mainstream technique of ULSI static RAM's to achieve internally clocked but externally fully asynchronous operation, that is, to build a high performance and easy-to-use RAM.

For cost minimization, newly developed redundancy circuits with 4 spare rows are used, which optimize yield without degrading the fast access time.

TABLE III
Typical RAM Characteristics

| | |
|---|---|
| OPERATION | FULLY ASYNCHRONOUS (ADDRESS ACTIVATED CLOCKED OPERATION) AUTO POWER DOWN FUNCTION |
| ORGANIZATION | 32K WORDS x 8 BIT |
| REDUNDANCY | 4 SPARE ROWS |
| CHIP SIZE | 6.68 x 8.86 mm$^2$ |
| CELL SIZE | 11 x 13.5 $\mu$m$^2$ |
| I/O INTERFACE | TTL COMPATIBLE |
| ADDRESS ACCESS TIME | 46 ns |
| ACTIVE POWER | 10 mW (1 MHz) |
| STANDBY POWER | 30 $\mu$W |
| PACKAGE | STANDARD 28PIN DIP |

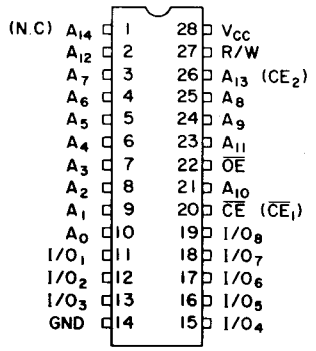


Fig. 12. Pin configuration of 256 kbit CMOS static RAM. The pin configuration is compatible with 64 kbit CMOS static RAM, whose pin configuration is shown in parentheses.

## Acknowledgment

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