RELIABILITY DEGRADATION of small geometry MOSFETs due to hot carriers is one of the most serious problems that prevail for high speed and high density VLSIs. It is known\(^1\) that the threshold voltage shift and conductance degradation are closely related to the substrate current that serves as a good monitor of the amount of generated hot carriers. Continuing efforts are being made to characterize degradation by dc measurements and also ac measurements of n-ch inverter\(^2\). This paper will describe a substrate current circuit simulator, applied to CMOS unit circuits and CMOS VLSIs. It was found that $V_{gs}-V_{ds}$ trajectory control is effective to improve circuit reliability. Circuits to suppress the hot carrier generation will be proposed. Many VLSI design implications have been obtained by the analysis, and applied to actual VLSI designs.

The substrate current model is basically a combination of earlier models\(^3\), modified to include substrate bias effects in the form of Taylor's expansion, which is shown in Figure 1 with a concrete expression. Previous models failed to reproduce $V_{th}$ effects. Matching of the measured results for a 1.0\(\mu\)m gate LDD MOSFET to model calculation was very good. Fitting was also successful down to the 0.8\(\mu\)m gate length conventional device with an oxide thickness of 16nm.

Figure 2 offers a comparison between simulated and measured substrate current waveforms for a CMOS inverter consisting of 1\(\mu\)MOSFETs. The agreement was satisfactory. Figure 3 shows dependence of the substrate current of an inverter on load capacitance. The $V_{gs}-V_{ds}$ trajectories with the constant substrate current plot in Figure 4 illustrates this dependence. It should be noted that the substrate current of a typically-loaded circuit, generated by a falling step voltage, is negligibly small (by over two orders of magnitude) compared with a rising step, and thus, lower load capacitance is preferable.

NAND circuits (Figure 5) offer improved characteristics over inverters and OR gates. The serial connection of n-ch MOSFETs relaxes drain voltage of each MOSFET and hence

FIGURE 2—Substrate current waveforms of an submicron inverter: (a) measured waveform including charging-discharging current of capacitances which is not hot, (b) simulated.

Add. buffer

0.5%

Add. buffer
duty = \frac{\int I_{sub} \, dt}{I_{cycle} \times I_{sub, peak}}

FIGURE 3—Substrate current for various load conditions.

FIGURE 4—V_{gs}-V_{ds} trajectories of CMOS inverters and equi-Isub plot.

FIGURE 5—Calculated duty ratios in typical (a)—NAND gate, (b)—C MOS gate, (c)—transmission gate, (d)—normally-on MOSFET inserted gate, (e)—limited voltage swing buffer.

FIGURE 6—Hot carrier duty ratios for 256Kb CMOS SRAM.