[See page 364 for Figure 4.]

SESSION XVIII: LOGIC ARRAYS AND MEMORIES

FAM 18.7: A 1Mb Virtually SRAM

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THE STORAGE CAPACITY OF STATIC RAMs has quadrupled every two years for three generations[1]. The 1Mb SRAM development program has not been able to match this pace, because of lithographic limitations notwithstanding the increasing demand for larger capacity SRAMs. This paper will offer a Virtually Static RAM (VSRAM) employing dynamic RAM cells, that virtually act as a static RAM in that no refresh operation is required by the user.

The basic operation of the VSRAM is shown in Figure 1. Refresh operation takes place in parallel with either address decoding or output driving, when word lines and bit lines are not occupied by normal access operation. Since the refresh operation is totally transparent to the users, the VSRAM is different from a pseudo SRAM.

Figure 2 shows a diagram of the basic structure. The refresh timer reveals when a refresh operation is needed and generates a refresh-request signal intermittently. If the memory cell array of the RAM is busy with a normal access, then, the refresh operation waits until the cell data is handed to a buffer register, which drives the output circuits. And vice versa, a normal access waits until the refresh operation ends. A normal/refresh selector serves as an arbiter[2] and provides necessary judgement. When the address changes, a normal request signal generated by an address transition detector inhibits refresh operation first, and then the normal operation begins after a 15ns wait period for an address skew.

Since high-speed operation of the memory core is a vital requirement in realizing a small overhead by the background refresh, bit lines are divided into 16 blocks, and double bit-line architecture[3] reduces capacitances as shown in Figure 3. Moderately LDD 1μ NMOSFETs[4] also help to obtain fast operation with sufficient reliability under 5V supply voltage. Normally-On Enhancement Mosfet Insertion (NOEMI) technology[5] is applied selectively to bootstraped nodes to endow hot-carrier resistancy to the circuits. N-channel memory cells are embedded in a P-well for protection from the minority carrier injection from I/O pins and alpha-particle induced electrons. No substrate bias is applied to reduce the standby current.

Process related parameters are listed in Table 1. A double-level poly-Si and double level Al process has been employed for circuit speed. The cell capacitor is planar and the design rule is 1.2μm.

A microphotograph of the chip is shown in Figure 4. Figure 5 demonstrates a typical address access time of 62ns. The slower access is the worst case access time; i.e., refresh operation taking place in advance of the normal access. The faster access is without refresh. This measurement is carried out by a test enable pin that affords control of the refresh-request signal externally. Since the access time without refresh is 48ns, the access time overhead by the background refresh is 29%. Electron beam tested internal waveforms are also shown in Figure 5. Quick switch from refresh to normal operation can be achieved by the dual bootstrap system, where one system is precharged when the other one is in operation. The pin configuration is shown in Figure 6.

The SRAM is believed to be a promising substitute for large-capacity SRAMs.

Acknowledgments

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Technology	Twin well CMOS
Layers	Double poly-Si and double Al
Gate length	1.0μ(NMOS), 1.2μ(PMOS)
Junction depth	0.20μ(N+), 0.35μ(P+)
Cap. oxide thickness	10nm
Gate oxide thickness	20nm
Poly-Si (Width/Space)	1.0μm / 1.4μm
1st Al (Width/Space)	1.3μm / 1.5μm
Contact hole	1.1μm / 1.4μm
2nd Al (Width/Space)	1.8μm / 1.9μm
Via hole	1.8μm / 2.0μm

TABLE 1—Process parameters.

[1] Isobe, M., Matsunaga, J., Sakurai, T., Ohtani, T., Sawada, K., Nozawa, N., Iizuka, T. and Kohyama, S., "A 46ns 256Kb CMOS RAM", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 214-215; Feb., 1984.

[2] Barber, F., Eisenberg, D., Ingram, G., Strauss, M. and Wik, T., "A 2K x 9 Dual Port Memory", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 44-45; Feb., 1985.

[3] Sakurai, T. and Iizuka, T., "Double Word Line and Bit Line Structure for VLSI RAMs", *15th Conf. on Solid State Devices and Materials, Extended Abstract*, p. 269-272; Aug., 1983.

[4] Kinugawa, M., Kakumu, M., Yokogawa, S. and Hashimoto, K., "Submicron MLDD NMOSFETs for 5V Operation", *Symp. on VLSI Tech.*, p. 116-117; 1985.

[5] Sakurai, T., Kakumu, M. and Iizuka, T., "Hot-Carrier Suppressed VLSI with Submicron Geometry", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 272-273; Feb., 1985. "Hot-Carrier Generation in Submicron VLSI Environment", *IEEE JSSC*; to be published.

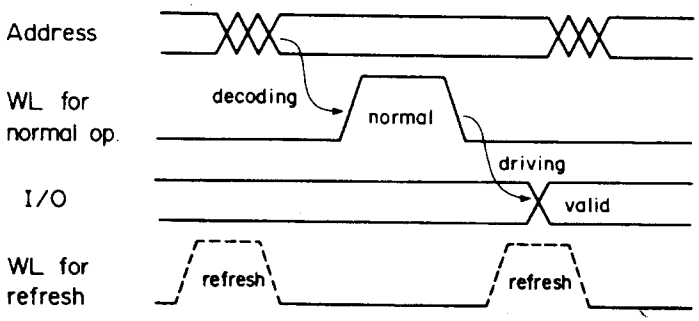

FIGURE 1—Basic operation of VSRAM.

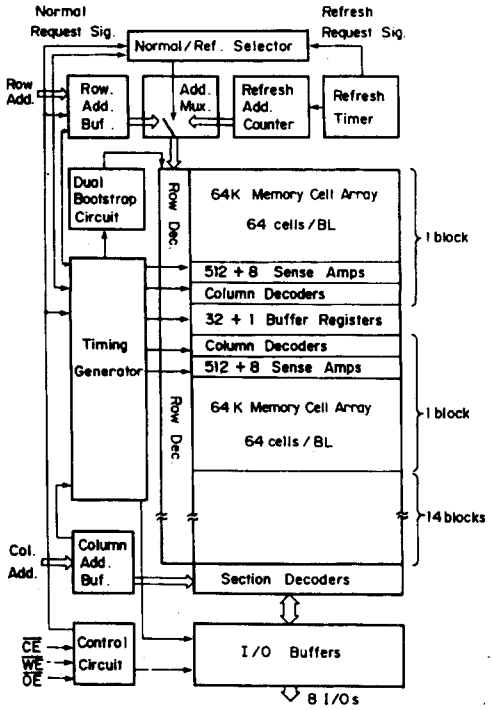

FIGURE 2—Schematic of basic structure.

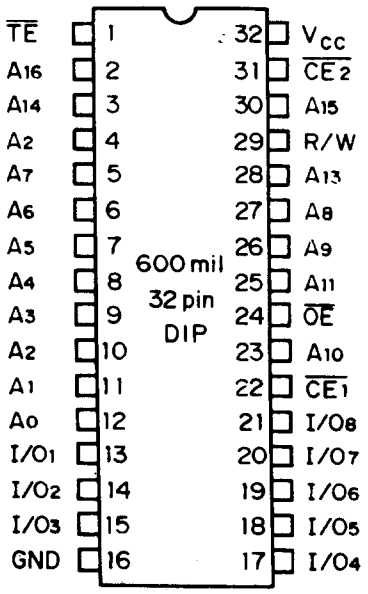

FIGURE 6—Pin configuration.

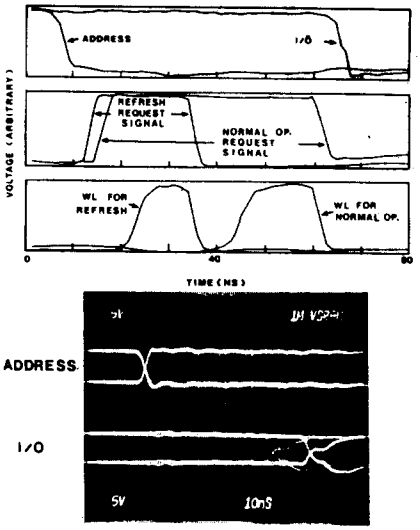

FIGURE 5—(*Top*) Address access time with and without refresh; (*bottom*) EB tested internal waveforms.

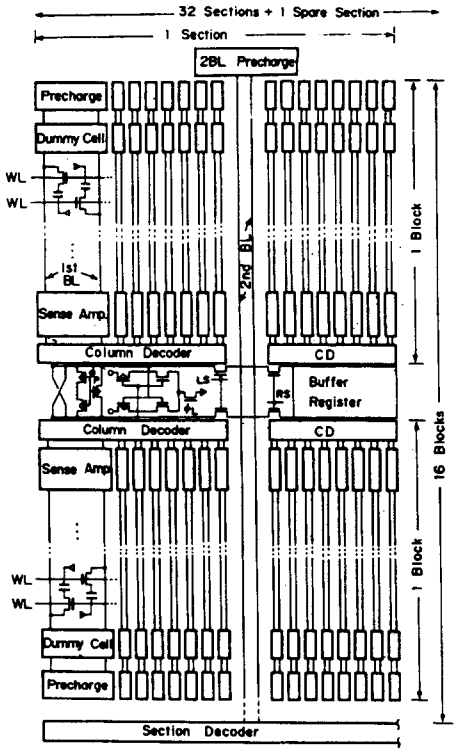

FIGURE 3—Basic architecture of memory array.

Organization	128KW x 8b
Chip size	5.99mm x 13.8mm
Cell size	3.5μm x 8.4μm
Address access time	62ns
Operating current	21mA (t_{cycle} = 150ns)
Standby current	400μA
Package	32 pin, 600mil DIP
Laser fuse redundancy	4 columns

TABLE 2—Performance list.

(Continued from Page 215)