Self-Aligned Refresh Scheme for VLSI Intelligent Dynamic RAMs

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1. Introduction

Recently, intelligent dynamic RAMs have been proposed to ease a cumbersome refresh timing control and to enable a battery back-up operation. Among them are a self-refresh dynamic RAM, a pseudo SRAM (PSRAM)[1] and a virtually SRAM (VSRAM)[2]. The last one completely frees the users from the refresh operation. The key circuit technology in making these intelligent DRAMs is a construction of a refresh timer, which tells the time when a refresh operation is needed. Conventionally, a ring oscillator has been used for this refresh timer. However, the voltage, temperature, and process dependencies of the ring oscillation frequency are far from being optimized. Therefore, one or two orders of magnitude higher refresh frequency is to be chosen to keep a margin, resulting in a high standby current of the RAM.

A self-aligned refresh scheme, namely a leak sensor, is newly proposed in this paper to fully overcome this problem. Since the leak sensor determines the refresh intervals in a self-aligned way with the memory cell charge leakage, it offers the optimized refresh frequency. Novel preset scheme cancels the circuit instabilities caused by the process fluctuations. Leakage characteristics of a capacitor is also investigated in relation to the leak sensor. The effectiveness of the leak sensor is demonstrated by a 1Mbit VSRAM.

2. Basic Idea of Leak Sensor

Figure 1 shows the circuit diagram of the leak sensor. In order to fully track the retention characteristics of DRAMs, the voltage of representative memory cells (C_1 and C_2) is monitored. If the voltage is lowered to the error level, the leak sensor fires and generates Φ_{RFSH} signal. Φ_{RFSH} signal triggers the conventional ring oscillator which is not shown in the figure and every row of the DRAM is refreshed once and then the RAM waits for the next Φ_{RFSH} signal so that the refresh is carried out intermittently.

The heart of the sensor part is a p-ch MOSFET T2, which monitors the voltage of node N1 and turns on when the voltage goes below $V_{DD} - V_{TP}$, where the second term is a threshold voltage of T2. The node N1 is first precharged to $V_{DD} - V_{TP}$ by using MOSFET T1. Then, it is bumped up to $V_{DD} - V_{TP} + V_{mgn}$ through the coupling of the C_1 as shown in Fig.2. Although a refresh interval is a strong function of V_{mgn} ($= V_{DD}\, C_1/(C_1 + C_2)$), V_{mgn} is not influenced by the process fluctuation on V_{TP} and the absolute value of the capacitance.

3. Results

Figure 2b is the internal waveforms measured by an electron-beam tester, which show good agreement with simulated results of Fig.2a. The minimum gate length is 1.0μm and n-ch memory cells are embedded in p-well.

Figure 3 and 4 show the voltage and temperature dependence of the circuit. It is clear that the leak sensor ideally tracks the retention characteristics of DRAMs. At room temperature where the usual battery back-up operation is carried out, the conventional oscillator gives more than 10 times higher refresh frequency than required. Even at the higher temperature, the refresh frequency of the leak sensor can be lowered by a factor of two to three compared with the conventional timer due to the optimized voltage and process margins.

The refresh intervals of the leak sensor coincide within 10% difference for V_{TP} = -0.2V and -0.6V. The power consumption of the leak sensor is measured 5μA at 80°C.

Figure 5 shows photomicrograph of 1Mbit VSRAM including the leak sensor. The area occupation is as small as 0.1% of the total chip, so that it is applicable to logic VLSIs with on-chip DRAMs. The standby current of the chip decreases from 400μA to 30μA as decreasing temperature from 85°C to 23°C.

4. Design Considerations

V_{mgn} should be trimmed according to the sensing circuit margins of a DRAM. The measured dependence of the refresh interval on C_1 is plotted in Fig.6. Trimming of C_1 can be achieved by using the fusible link in the initial design. If intra-chip fluctuation is considerable, plural leak sensors are placed on a chip and the earliest Φ_{RFSH} is designed to start the refresh.

Several capacitors with different peripheral lengths and with the same capacitance are made and charge decay curves are measured, some of which are demonstrated in Fig.7. The average leak velocity for initial 0.5V down from 5V is expressed as 5.6 + 19.2 L/S (mV/sec), where L is a peripheral length in μm and S is a capacitance area in μm^2. If the V_{mgn} happens to be too small, the monitor cell capacitor can be designed to have a longer peripheral length than the memory cell capacitor.

5. Conclusion

A leak sensor is proposed and shown to be promising to drastically improve the stand-by current of VLSI intelligent DRAMs, to enable a long term battery back-up operation, and to endow the RAM non-volatility.

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Reference

1) S.Tsuchida et al, "A 64K Pseudo Static RAM with N-well CMOS Technology," 1983 Symp. on VLSI Tech., pp.36-37.
2) T.Sakurai et al, "1Mbit Virtually Static RAM," 1986 ISSCC submitted.

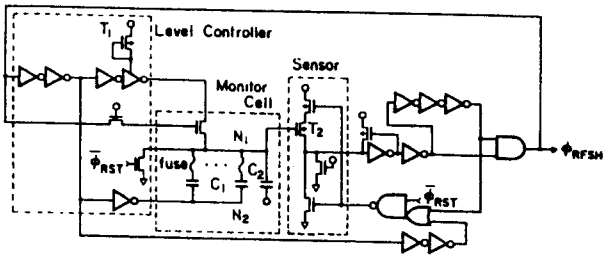

Fig.1 Circuit diagram of leak sensor.

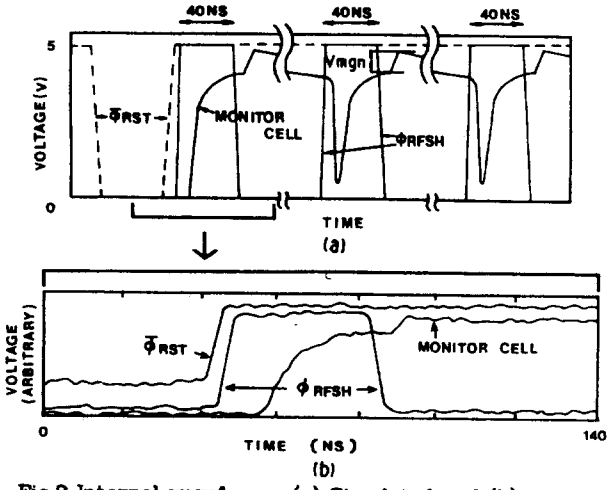

Fig.2 Internal waveforms. (a) Simulated and (b) measured by EB tester.

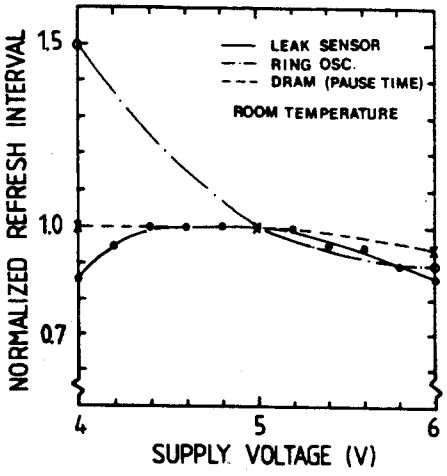

Fig.3 Measured supply voltage dependence of refresh interval.

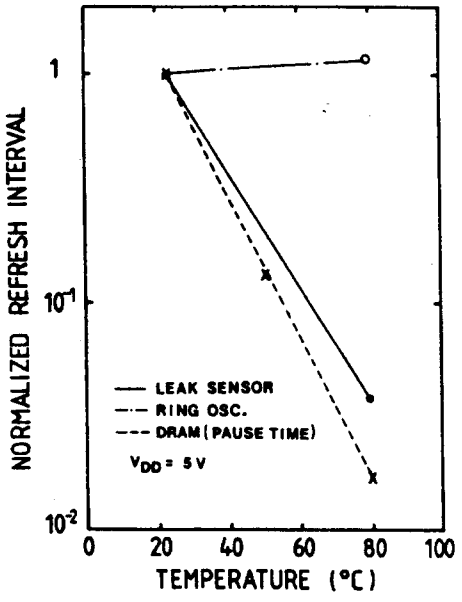

Fig.4 Measured temperature dependence of refresh interval.

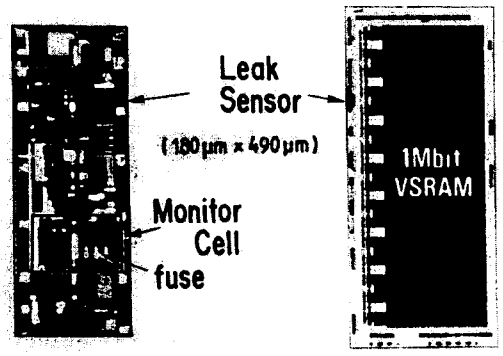

Fig.5 Photomicrograph of leak sensor and 1M VSRAM chip.

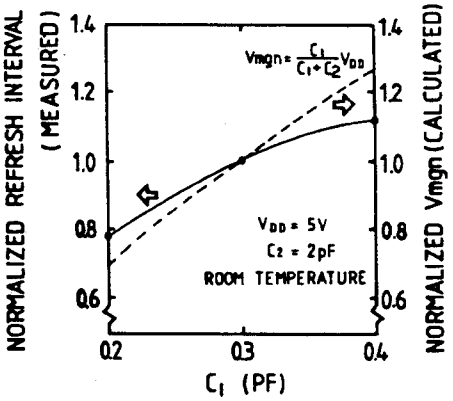

Fig.6 Refresh interval trimming by fusible links.

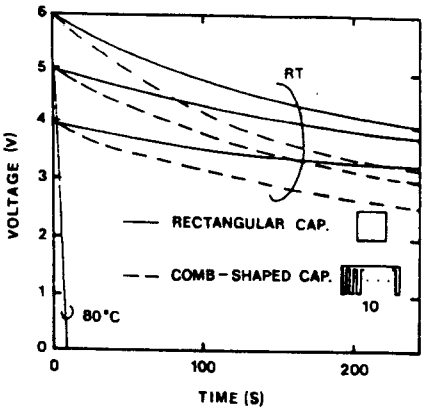

Fig.7 Measured charge decay curves of various capacitor under voltage and temperature variation.

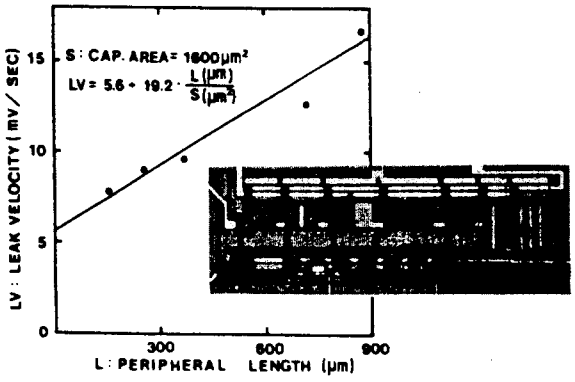

Fig.8 Measured leak velocity variation on peripheral length and TEG chip photomicrograph.