1-MBIT VIRTUALLY STATIC RAM

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Abstract—A new type of 1-Mbit static RAM (SRAM), named a
virtually static RAM (VSRAM), is proposed and successfully made, using
a one-transistor and one-capacitor type dynamic memory cell. Since all the
refresh-related operations are done on chip, the RAM virtually acts as a
static RAM. The refresh operations are merged into the normal operation,
which is called a background refresh and is the key principle of the
VSRAM. To realize the background refresh, the RAM includes an intelligen
ton-chip refresh control circuit. Since the fast operation of the core
part of the RAM is crucial to minimize the access-time overhead by the
background refresh, 16 divided bit lines and parallel processing techniques
are employed. Novel hot-carrier resistant circuits are applied selectively
to boosted nodes for high hot-carrier reliability. N-channel memory cells
are embedded in a p-well, which gives a low soft error rate of less than 10FIT.
As for process technology, 1-μm N-MOSFET's with moderately lightly
doped drain (MLDD) structures offer fast 5-V operation with sufficient
reliability. An advanced double-level poly-Si and double-level Al twin-well
CMOS technology is developed for the fast circuit speed and high packing
density. The memory cell size is 3.5×8.4 μm², and the chip size is
5.99×13.8 mm². Address access time is observed typically at 62 ns, with
21-mA operating current and 30-μA standby current at room temperature.

I. INTRODUCTION

STORAGE capacity of static RAM's (SRAM's) has
been quadrupled every two years for three generations
[1]. One-megabit SRAM's, however, are difficult to make
in this development speed because of a lithography limit,
although the demand for larger capacity SRAM's is ever
increasing. To realize 1-Mbit SRAM with high-resistive
poly load four-transistor cells, 0.8-μm process technology
is required, which is not matured as yet.

In this paper, a new type of a static RAM, called a
virtually static RAM (VSRAM), is introduced as a new
approach [3] to overcome this situation. The conventional
approach to solve the above-mentioned problem was a
pseudo SRAM (PSRAM) [2]. The PSRAM is a no address-
multiplexed version of a dynamic RAM (DRAM) using
one-capacitor cells. Since the chip size is small, the 1-Mbit
PSRAM can be made with 1.0-1.2-μm technology but a
PSRAM requires cumbersome refresh operations on the
user's side. On the other hand, the conventional SRAM
needs no refresh operations but the cost is much higher
because of its larger memory cell area and moreover a
1-Mbit SRAM cannot be made now because of the above-
mentioned lithography problem.

The VSRAM is proposed to combine the low cost of the
PSRAM and the easy-to-use features of the conventional
SRAM. The VSRAM employs a one-transistor and one-
capacitor type small dynamic memory cell, but since all the
refresh-related operations are done on a chip, the
refresh operations are completely transparent to the users.
It frees the users from the refresh timing control and the
irregular time loss caused by the refresh and virtually acts
as a SRAM. The VSRAM can be directly connected to the
CPU without any aid from a refresh controller, as opposed to
the PSRAM.

A chip size comparison among the VSRAM, the PSRAM,
and the conventional SRAM is shown in Fig. 1. The
PSRAM has the smallest chip size but it requires refresh
operations, which is contrary to the conventional SRAM.
The VSRAM combines the merits of these two.

Section II describes the basic idea of the VSRAM, called
a background refresh. This background refresh is a method
to make the refresh transparent to the users by merging the
refresh into a normal access operation, which is a key
principle of the VSRAM. In Section III, on-chip refresh
control circuits and new core architecture are proposed as
circuit ideas. High-speed high-reliability process technolo-
gies are described in Section IV. Performance results and
other features of 1-Mbit VSRAM are summarized in Sec-
 tion V. Sections VI and VII are dedicated to discussions
and conclusions, respectively.

II. BASIC IDEA OF VSRAM

In a SRAM, an address transition or a chip-enable
signal transition triggers a chain of circuit actions: address
decoding, word-line driving, cell data sensing, data transfer
to output circuits, and output driving. In this process, in
the address decoding and the output driving period, a core
part of the RAM is not occupied by the normal access
process. Here, the core part means word lines, bit lines,
memory cells, and sense amplifiers.
Fig. 2. Basic operation of VSRAM. Refresh operations are merged in either the address-decoding or output-driving period of the normal access cycle, where the core part of the RAM is not occupied through the normal access process. This background refresh is the key concept of the VSRAM.

In the VSRAM, the refresh operations, if necessary, can take place in this time period so that the refresh can be merged into normal access operation without much degrading of the access time. The refresh operation is triggered only when an on-chip refresh timer tells that the refresh should take place soon, which is rather frequently. This feature is shown in Fig. 2, where a refresh word-line waveform is shown by a dotted line. This is the basic idea of the VSRAM, named a background refresh.

The faster the refresh operation, the smaller the overhead of the background refresh on the access time. Fast operation of the core part is important for effectively realizing the VSRAM and is pursued through circuitry and processing.

III. CIRCUIT DESIGN

Circuit technologies employed in making 1-Mbit VSRAM are summarized in Table I. In the table, the purpose and effects are made clear for each item.

An on-chip refresh control circuit to achieve the background refresh is described in Section III-A. The core architecture is discussed in Section III-B, including a 16 divided double bit-line structure, a buffer register, a half-\( V_{cc} \) bit-line precharge, and a half-\( V_{cc} \) cell plate. A dual bootstrap system, which helps in fast switching between the refresh and normal operations, is treated in Section III-C. In Section III-D, a method to endow hot-carrier resistancy to the circuits is described.

A. On-Chip Refresh Control Circuit

Fig. 3 shows a schematic diagram of the basic structure. An on-chip refresh control circuit is composed of a refresh timer, a normal/refresh selector, a refresh address counter, and an address multiplexer.

The refresh timer tells the time when a refresh operation is needed and generates a refresh-request signal intermittently. This timer is made with a novel charge leakage monitoring technique, named leak sensor [4]. Since the leak sensor determines the refresh intervals which are synchronized with the memory cell charge decay, it offers the optimized refresh frequency and improves the standby current of the RAM.

The normal/refresh selector serves as an arbiter [5] and is intelligent enough to judge which of the refresh and the normal operations is to be active when a contention occurs between these two. If the memory cell array of the RAM is busy with a normal access, then the refresh operation waits
until the core part of the RAM is freed from the normal operation, and, vice versa, a normal access waits until the refresh operation ends. The normal access-time overhead of the background refresh will be shown to be 29 percent in Section V. The normal operation request signal is generated by address transition detectors and a chip-enable transition detector.

The refresh address counter generates a row address for a refresh operation. The address multiplexer is a switch circuit controlled by the normal/refresh selector and provides either the normal or the refresh addresses to row decoders according to the judgement of the normal/refresh selector.

This on-chip refresh control circuit acts automatically without any operations on the user's side and enables the RAM to be easily used.

B. Core Architecture

Fig. 4 shows a schematic diagram of the core part. Double bit-line structure [6] is adopted for high-speed operation of the core part. First bit lines are divided into 16 blocks and each bit line has only 64 memory cells, which is half in number compared with the conventional DRAM's. This makes a bit line 30 percent lighter in capacitance and enables faster operation of the core part. As for word organization, 128K word × 8 bit is adopted, being best fit for the smaller systems.

The other unique core architecture is a buffer register placed near the sense amplifier. When the data of a memory cell are read out to the sense amplifier, it is handed to the buffer register and then the buffer register in turn drives the output circuits, during which the sense amplifier can be used for a refresh operation at the same time. This parallel processing is another key to the fast operation of the core part. Besides, combination of the buffer register and the double bit-line structure enables fast data transfer because of larger drivability of a buffer register and reduced line capacitance of the second bit line.

A half-$V_{cc}$ bit-line precharge scheme realizes a fast serial operation of refresh and processes because of the shorter precharging time. It also decreases the power consumed by data readout and rewrite. A half-$V_{cc}$ cell-plate voltage scheme reduces the voltage applied to the capacitance oxide, increasing the reliability.

C. Dual Bootstrap System

The dual bootstrap system is introduced in the RAM to realize fast switching between a refresh and a normal operation. If only one bootstrap circuit is incorporated on a chip, a fast precharge of a large capacitor in the bootstrap circuit around 5 ns will be needed. Such a fast precharge will produce current noise which will degrade the circuit stability and reliability of the RAM.

The dual bootstrap system is an elegant solution for this problem. When one bootstrap system is in operation, the other bootstrap circuit is in precharge mode to prepare for the next bootstrap of a word line. Each bootstrap circuit, therefore, is given a sufficient precharging period, say 25 ns typically. The system can be said to take advantage of parallel processing.

D. Hot-Carrier Resistant Circuit Technology

In submicrometer channel-length MOSFET's, hot-carrier-induced degradation becomes a serious problem. The situation is very serious in those RAM's where word lines and other related nodes are driven up to a boosted voltage which is typically 1.5–2.0 times the supply voltage. This means that the chip is operated as a 10-V system although the supply voltage is 5 V. Concerning this point, DRAM's have a more serious problem than SRAM's.

In the VSRAM, special remedies are taken for eliminating this problem, namely a hot-carrier resistant circuit technology [7], [8]. The salient feature of the circuit is the normally on enhancement MOSFET insertion (NOEMI) at the top of the n-channel logic technology as shown in Fig. 5. This type of circuit is applied selectively to boosted nodes, where two to three orders of magnitude larger amounts of hot carriers are generated in discharging the node. Conventionally, the discharging NMOSFET operates mostly under the condition that the drain voltage is higher than the gate voltage, and therefore a large amount of hot carriers is generated, degrading the NMOSFET.
Using the NOEMI technology, two serially connected NMOSFET's are used for discharging boosted nodes. This configuration relaxes the drain-source voltage of each MOSFET and about three orders of magnitude smaller hot-carrier generation is observed compared with the conventional configuration, since the hot-carrier generation shows exponential dependence on the drain-source voltage. For this reason, NOEMI technology can be said to be an effective method to suppress hot-carrier generation that offers high reliability without changing any processing steps. It is not effective to use a longer channel device for this purpose, because the hot-carrier generation is mainly determined by the local electric field near the drain, which is a strong function of the oxide thickness and the impurity profile but does not show sufficiently strong dependence on the gate length.

IV. CMOS Process Technology

An advanced double-level poly-Si and double-level Al twin-well CMOS technology is developed to fabricate the RAM. Process technologies for 1-Mbit VSRAM are listed in Table II. Here 1-μm NMOSFET's and 1.2-μm PMOSFET's help to achieve the high-speed circuit operation. The NMOSFET's are made with moderately lightly doped drain (MLDD) structure [9] to assure sufficient reliability under 5-V supply voltage. Although the minimum dimension is 1 μm for poly gate, the basic design rule for the other layers is 1.2 μm, which optimizes the performance and the production yield trade-offs.

Fig. 6 is a cross-sectional view of the 1-Mbit VSRAM. The RAM does not include an on-chip substrate bias generator in order to minimize the standby current, thus the n-type substrate is biased to \( V_{cc} \). If a voltage overshoot occurs at the I/O pins, the p-channel MOSFET drains are forward biased and minority carriers are generated and may destroy the memory cell data. Memory cells are embedded in a p-well for protection from the minority carriers. In fact, no error mode is observed even with \( V_{cc} + 3 \)-V overshoot and \( V_{ss} = -3 \)-V undershoot at the I/O pins.

This p-well also improves alpha-particle immunity [10]. The soft error rate is observed to be as small as 10 FIT at 150-ns cycle time and the cell mode soft error rate is less than 0.1 FIT. The reason for the low soft error rate is considered threefold. As for the diffusion component, the p-well potential barrier is effective in rejecting the alpha-particle-induced minority carriers and the small memory size is helpful in the sense that the minority carriers are shared by adjacent cells to decrease collection efficiency. As for the drift component, a rather high well impurity concentration of \( 4 \times 10^{19}/\text{cm}^2 \) diminishes the so-called funneling effect [11]. The memory cell capacitor is a planar type and the technology is already well established.

The double-level Al process contributes to the fast operation of the core part due to the inherent low resistivity and the reduced parasitic capacitance. The first level is used for bit lines and its low resistivity enables fast cell data sensing and fast bit-line precharge. The second level is used for word lines and is shunted to the poly word lines every 128 cells. The RC delay of the word lines is decreased to less than 1 ns, which should be compared with about 50 ns without the Al word-line stripping.

V. Performance

Internal waveforms of the 1-Mbit VSRAM are measured by an electron beam tester as shown in Fig. 7. It can be seen from this figure that the above-mentioned normal/refresh selector successfully judges which of the refresh and normal operations is to be active when both of the request signals occur simultaneously, and that refresh operation is completed in 25 ns. In this measurement, the refresh operation is externally triggered by using the test-enable pin, because the electron-beam tester needs a number of repeated operations to get accurate waveforms and
the refresh should take place synchronously with the normal access.

Fig. 8 shows address access time of 62 ns. The faster access time of 48 ns is observed when a refresh does not take place in advance of a normal access. This observation indicates that access-time overhead by background refresh is 29 percent. This 14-ns overhead should be compared with about 80-ns overhead by the user-controlled refresh ... the conventional PSRAM. Of course, in the PSRAM case, the refresh is achieved only by careful refresh control on the user's side.

Fig. 9 is a microphotograph of the 1-Mbit VSRAM with a chip area of 83 mm². The area increase by the arbiter is about 0.1 percent.

The achieved performances are listed in Table III. The low operating current of 21 mA at cycle time of 150 ns can be achieved by the bit-line capacitance reduction. The standby current is measured to be as small as 30 μA at room temperature which enables battery backup operation of the RAM.

VI. DISCUSSIONS

Differences between VSRAM and the conventional SRAM are listed in Table IV.

The first difference is in the maximum write pulse-width specification. The basic idea described in Section II is the case for a READ operation where a word line can be pulsed, that is, a word line can be shut off when stored data are read out to the output. In this case, the refresh can be inserted after the word-line shut-off, so that no problem occurs even if a very long READ cycle is used. However, in a WRITE operation, a word line should be opened statically because WRITE data may be changed at any time during the WRITE operation. Then, if a very long WRITE cycle is used, the refresh operation cannot be inserted at all, which will destroy the stored data. Because of this situation, the duration time of a WRITE enable pulse is limited to a finite period, say 10 μs in this design. However, it may not limit the VSRAM application seriously, since a WRITE operation is usually done in a synchronous mode, where a WRITE enable signal width is not more than 1 μs.

The second issue is about the data retention voltage. The conventional SRAM guarantees a data retention at 2 V, but for DRAM cells a voltage bump from 2 to 5 V is very severe. The retention voltage of the VSRAM is thus restricted to around 5 V, but since the retention current is small, a battery backup operation is possible.

The last point of difference is an address skew. The address skew is limited up to 15 ns in this design. This is
due to a data destroying nature of a DRAM readout. The fast access users can achieve this level of on-board address skew and the slow access users can use the VSROM in a synchronous mode.

VII. CONCLUSIONS

The virtually static RAM was proposed to realize an easy-to-use refresh-free RAM with storage density of a dynamic RAM. The key principle of the VSROM is a background refresh, where refresh operation is merged into normal access operations. The circuits to fully control the refresh-related operations were discussed in detail.

A 1-Mbit VSROM was successfully made using an advanced twin-well CMOS technology, and the validity of the VSROM concept is assured. In order to minimize the access time, hierarchical structures and parallel processing are pursued in various aspects. Since the VSROM can be made about two years earlier than the conventional SRAM, it is quite competitive in the large-capacity SRAM field and can be a promising substitute for future high-density SRAM's.

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