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VLSI Circuit Reliability under AC Hot-carrier Stress

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Introduction

The hot-carrier problems are one of the most serious obstacles in making high-density, high-speed VLSI with submicron geometry. Consequently, the MOSFET device level degradation under DC and AC stress has been investigated intensively in the past few years. However, little work has been carried out on the circuit level[1]. This paper deals with two new aspects of the circuit behaviors under AC hot-carrier stress.

One is on a hot-carrier resistant circuit structure called NOEMI (Normally-On Enhancement Mosfet Insertion)[2]. The verification of the effectiveness of the NOEMI through a direct experiment is carried out for the first time, and the circuit optimization strategy for the NOEMI is described. The other is a proposal of a new simple model which can give insights to the relation between the hot-carrier MOSFET degradation and the circuit behavior.

Experiments on NOEMI

The NOEMI is a circuit structure where serially connected MOSFETs relax drain-source voltage of each MOSFET to suppress hot-carrier generation as shown in Fig.1. The figure demonstrates the NMOSFET hot-carrier degradation comparison between the conventional CMOS inverter and the NOEMI inverter under 9V AC stress. In this experiment, 1μm MLDD NMOS[3] and 1.2μm conventional PMOS were used. In the conventional inverter after 10^5 sec AC stress, the transconductance of the triode region, g_m, and the drain saturation current, I_{do}, show degradation more than 30% and 7%, respectively. On the contrary, the NOEMI inverter shows no significant change. It is seen from Fig.1 that the NOEMI has at least three orders of magnitude stronger resistancy to the hot-carrier compared with the conventional inverter. Therefore the NOEMI will be indispensable to assure sufficient reliability for bootstrap circuits in sub-micron DRAMs[4], where 8V AC stress is applied even if the supply voltage is 5.5V.

NOEMI Optimization

There are two parameters in the NOEMI structure that should be optimized, namely, the gate voltage(V_{GG}) and the channel width(W) of the normally-on MOSFET. V_{GG} and the size relate with the reliability and the circuit speed, respectively. Figure 2 shows measured I_{sub} plot on V_{DD}-V_{GG} plane together with simulated propagation delay plot. It is found from Fig.2 that there is an optimum V_{GG}, $V_{GG,OPT}$, in terms of reliability when the supply voltage is given, since I_{sub} was shown to be a good monitor of the hot-carrier degradation[5]. It is also seen from the figure that the speed remains almost constant even if V_{GG} is increased above the optimum point. $V_{GG,OPT}$ is approximately expressed as

$$V_{GG,OPT} \approx \frac{1}{2}V_{DD} + V_{TH'}$$

where $V_{TH'}$ denotes the threshold voltage with substrate bias effect. In Fig.3, the I_{sub} of the optimized NOEMI in comparison with the conventional inverter is re-plotted to clarify the difference.

Figure 4 shows the relationship between propagation delay and the size of the normally-on MOSFET, (W_{n1}), with the PMOS size(W_p) as a parameter. When both of W_{n1} and W_p are around $2W_{n2}$, the circuit shows the minimum delay. The reason is as follows. If W_{n1} is small the effective drivability for discharging is small, but if W_{n1} is too large the junction capacitance of the normally-on MOSFET degrades the speed. Varying W_{n1} does not affect the reliability because the maximum voltage of the middle node V_m depends on V_{GG} but not on W_{n1}.

Model for Circuit Degradation

Figure 5 shows the typical DC characteristics of 1μm MLDD NMOS before and after AC hot-carrier stress. The device shows the degradation especially in a triode region, being same as the DC stress degradation. How does this LDD type of degradation affect the circuit speed? In order to understand the relationship between the triode region degradation and circuit delay, a simple model as shown in Fig.6 is proposed. The advantage of this model is the freedom of varying triode and pentode characteristics independently. R_3 and R_5 signify the effective MOSFET resistance in the triode region and in the pentode region, respectively. With this model the switching delay t_{pd} is expressed as follows.

$$\frac{t_{pd}}{CR_5} = 0.9 + \frac{R_3}{R_5}\ln\frac{10R_3}{eR_5}$$

If R_3 is changed from R_3 to $R_3+\Delta R_3$ due to the hot-carrier effects, the change in t_{pd}, Δt_{pd}, is expressed as

$$\left(\frac{\Delta t_{pd}}{t_{pd}}\right) / \left(\frac{\Delta R_3}{R_3}\right) = \frac{(R_3/R_5)\ln(10R_3/R_5)}{0.9 + (R_3/R_5)\ln(10R_3/eR_5)}$$

The above model calculation agrees well with the SPICE2 simulation using AC hot-carrier degraded MOSFETs as shown in Fig.7. The figure suggests that the change rate of t_{pd} is small when R_3/R_5 is small. The R_3/R_5 decreases for smaller MOSFETs because of the velocity saturation of carriers by gate voltage. As a result, even if 10% change is observed in $\Delta R_3/R_3$ by the hot-carrier degradation, the circuit speed becomes less sensitive to the hot-carrier degradation for smaller MOSFETs.

Conclusions

The NOEMI circuit technology is experimentally shown to be effective in realizing reliable sub-micron VLSIs, and found to have the optimized gate voltage and the optimized size for the normally-on MOSFET. Secondly, a simple model is proposed which helps to understand the relationship between the LDD MOSFET degradation and the circuit degradation.

Acknowledgement

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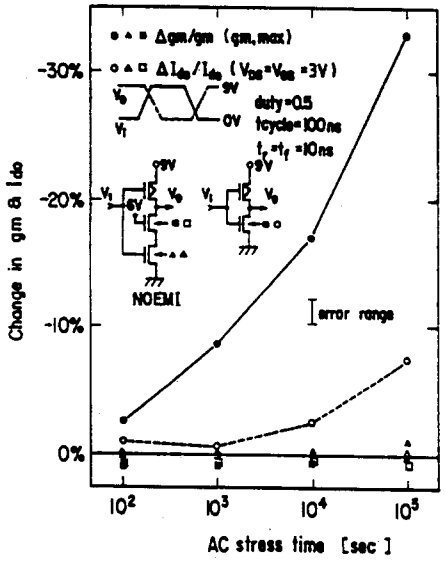
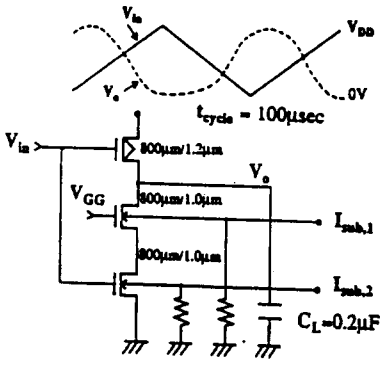


Fig.1. Measured reliability comparison between NOEMI and conventional inverter



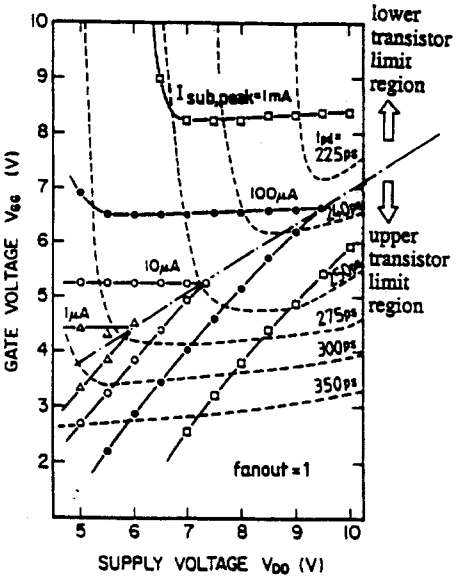


Fig.2. Measured I_{sub} plot on NOEMI gate voltage V_{GG} and V_{DD} plane

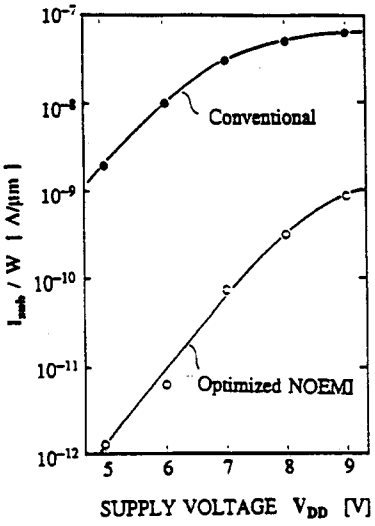


Fig.3. Substrate current comparison between optimized NOEMI and conventional inverter

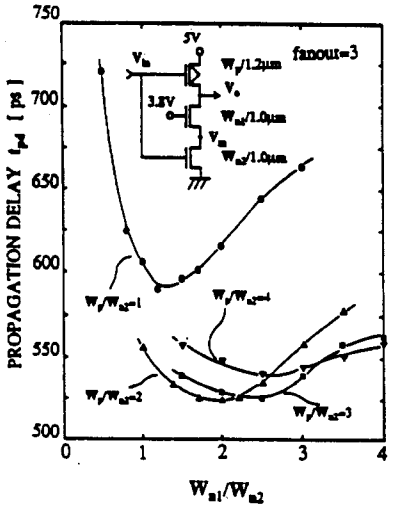


Fig.4. Optimization of normally-on MOSFET size

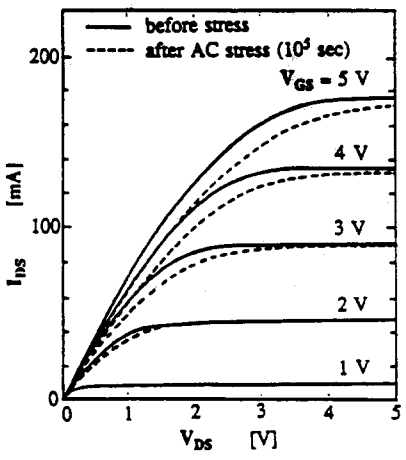
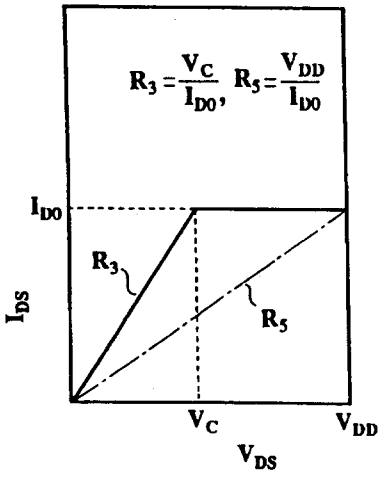


Fig.5. DC characteristics of LDD MOSFET before and after AC hot-carrier stress



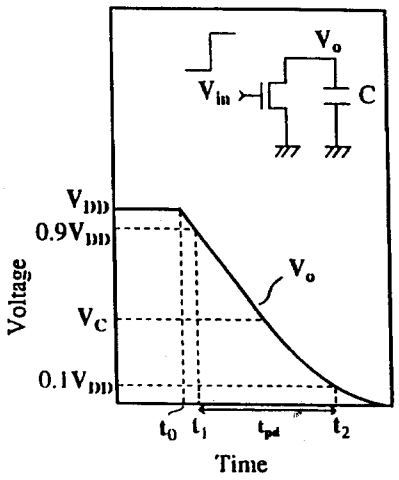


Fig.6. A simple model to clarify triode and pentode region contribution to circuit delay

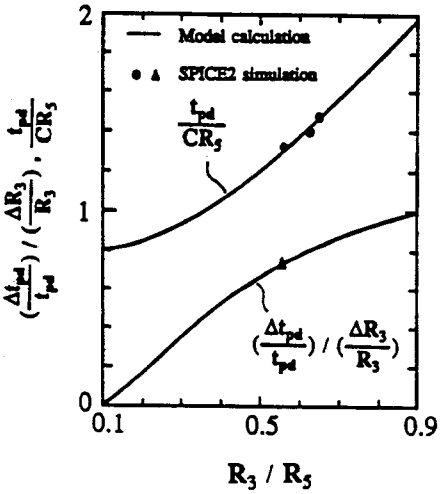


Fig.7. t_{pd} and Δt_{pd} dependence on (R_3/R_5)