A 30-μA Data-Retention Pseudostatic RAM with Virtually Static RAM Mode

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Abstract—**This paper describes a newly developed 1-Mbit (128K×8) pseudostatic RAM (PSRAM). A unique feature of the RAM is its inclusion of a virtually static RAM (VSRAM) mode, while being fully compatible with a standard PSRAM. The RAM changes into the VSRAM mode when the $\overline{RFSH}$ pin is grounded, even in active cycles. The RAM can be used either as a fast PSRAM of 36-ns access time or as a convenient VSRAM of 66-ns access time. The typical operation current and data-retention current are 30 mA at 160-ns cycle time and 30 μA, respectively. In order to achieve high-speed operation, low data-retention current, and high reliability, the RAM uses several new design technologies, that is, delay-time tunable design, a new current-mirror timer, hot-carrier resistant circuits, and an optimized arbiter. These technologies are applicable to general advanced VLSI's.**

I. INTRODUCTION

RECENTLY, demands for easy-to-use DRAM's have increased for microcomputers, computer peripherals, and portable equipments. Several kinds of intelligent DRAM's have been proposed to meet this demand. Among them are a pseudostatic RAM (PSRAM) [1] and a virtually static RAM (VSRAM) [2], [3].

The PSRAM is no address-multiplexed version of a DRAM. The PSRAM requires refresh timing control on the user's side, but the operation speed is fast. On the other hand, the VSRAM is slower than the PSRAM but is completely refresh-free and can be used as a SRAM. The VSRAM is slower because the normal operation may wait until an internal background refresh ends. Both the PSRAM and the VSRAM are byte-wide RAM's and their data-retention current is relatively low, which is convenient for small system applications.

In this paper, a fast and low power 128K×8-bit PSRAM with a VSRAM mode is described. The unique feature of the present RAM is inclusion of a VSRAM mode, while being fully compatible with the conventional PSRAM, so that the RAM can be used either as a fast PSRAM or a convenient VSRAM. The RAM uses several new design technologies, that is, delay time tunable design, a current mirror timer, and an optimized arbiter, to achieve high speed, low power, and high reliability. These technologies are applicable to general VLSI circuit design.

Section II describes the difference between the PSRAM mode and the VSRAM mode. In Section III, key design items employed in the RAM are discussed. Section IV summarizes process technologies and the features of the RAM. Comments on the suitability of the design as a DRAM macro in a logic library and the points of functional difference between the VSRAM and the ordinary SRAM are given in Section V. Section VI is dedicated to conclusions.

II. PSRAM AND VSRAM MODE

Fig. 1 explains the difference between the PSRAM and the VSRAM. As an architecture, the VSRAM is a superset of a PSRAM, including a refresh-normal arbiter. The arbiter judges which of the refresh and the normal operations will be active when contention occurs between a normal operation request and an internal refresh request. Since the arbiter occupies only 1-percent silicon area of the total chip, the inclusion of the VSRAM mode causes very small overhead in the cost over the conventional PSRAM.

The mode switching between the PSRAM mode and the VSRAM mode is electrically done by controlling the $\overline{RFSH}$ pin. The RAM changes into the VSRAM mode when an $\overline{RFSH}$ pin is grounded even in active cycles as shown in Fig. 2, which is prohibited in the conventional PSRAM. When in the VSRAM mode, the RAM can be directly connected to the CPU without any refresh controller, in other words, the RAM can be used as a synchronous SRAM.

Another unique feature of the RAM to reduce the user's load is the maximum cycle time. The maximum cycle time of the RAM is set to infinity with the aid of a leak compensation circuit for boosted word lines and the word-line auto shutoff technique. Even if the boosted word-line level is compensated, there exists the problem of internal background refresh in the VSRAM mode. If the word line is opened for a long time, it is not possible to activate the internal background refresh. Therefore, the

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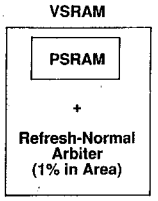

Fig. 1. Comparison between PSRAM and VSRAM. As an architecture, VSRAM is a superset of PSRAM.

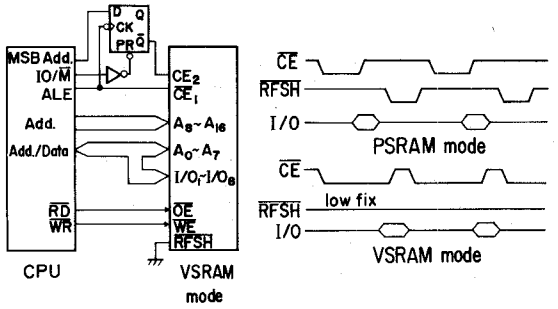

Fig. 2. Switching between PSRAM mode and VSRAM mode. In VSRAM mode, the RAM can be directly connected to CPU without any refresh controller in-between.

RAM is designed to shut off the word line automatically after a certain period—10 μs in this design. This technique does not limit a long-cycle READ operation because stored data are transferred to a data latch in an output buffer and the readout operation by $\overline{OE}$ pin can be done statically even after the word line is shut off. Only the maximum value of write pulse width is constrained up to 10 μs, but it does not set any limitation to usual applications, so that a static address latch enable (ALE) signal can be directly applied to a $\overline{CE}$ pin, unlike the conventional PSRAM. If the maximum cycle time is not infinity, some extra external circuits should be added to make the ALE signal active only in a limited time span. In connecting the RAM to CPU's, the number of the external IC's can be quite small, even smaller than the SRAM's because address latches are required in case of SRAM's to demultiplex address and data.

Fig. 3(a) shows access waveforms of a typical chip in PSRAM mode and VSRAM mode under the conditions of 5 V and room temperature. The faster access time of 36 ns corresponds to the PSRAM mode and the slower access time of 66 ns to the VSRAM mode. In the measurement, I/O pins are loaded with 100 pF, which is a commonly used condition. Fig. 3(b) shows internal waveforms for the VSRAM mode measured by an electron beam (EB) tester. It can be seen that the refresh-normal arbiter correctly resolves the contention between refresh and normal operation. Only in the EB tester measurement, are I/O pins set in the high-impedance state and not loaded with external capacitances. A broken line indicates estimated I/O voltage response for 100-pF output capacitance. In the figure it looks like the word line for normal operation has a certain noise level when the refresh word line is activated. This is because measured adjacent word lines influence each other in the electron EB tester measurement; that is the local electric field effect.

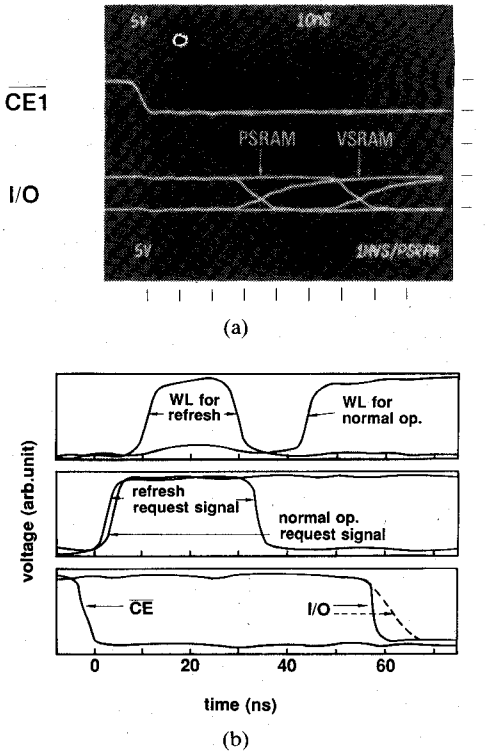

Fig. 3. (a) Access waveforms. The faster access of 36 ns corresponds to the PSRAM mode and the slower access of 66 ns to the VSRAM mode. (b) Internal waveforms for VSRAM mode measured by electron-beam tester. It can be seen that refresh-normal arbiter correctly resolves the contention between refresh and normal operation.

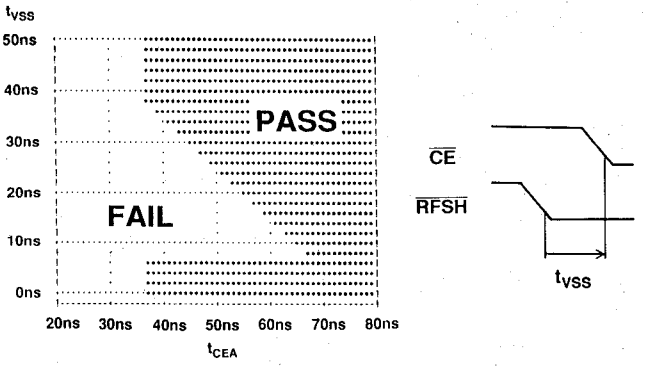

Fig. 4. Access-time schmoo plot versus t_{VSS}. t_{VSS} is the time delay from $\overline{RFSH}$ falling edge to $\overline{CE}$ falling edge. The access time depends on t_{VSS} because the internal refresh takes place in advance to the normal access.

Fig. 4 shows a schmoo plot of CE access time t_{CEA} versus t_{VSS} which is the time delay from the $\overline{RFSH}$ falling edge to the $\overline{CE}$ falling edge When t_{VSS} is very large, that is, there is no contention between the normal request and the refresh request, the RAM shows the fastest access of 36 ns. When t_{VSS} gets smaller, the internal refresh takes place in advance to the normal access, and consequently, the access time becomes slower. The slowest access time is 66 ns, which is the access time in the VSRAM mode. The slowest case occurs when the $\overline{RFSH}$ pin falls 6 ns before the $\overline{CE}$ pin falls. This 6 ns indicates the difference between $\overline{RFSH}$ and $\overline{CE}$ buffers. When t_{VSS} is less than 6 ns, the internal refresh takes place after the normal operation ends, and the access time returns to the fastest one.

III. Design Aspects

Several design technologies are introduced to achieve high speed, low power consumption, and high reliability. First, delay-time tunable design is described in Section III-A. This technology is useful to obtain high-speed operation even in complicated VLSI's. Secondly, a new current-mirror timer with good stability and low power dissipation is discussed in Section III-B. As for reliability, experimental verification of a hot-carrier-resistant circuit and an arbiter optimization are reported in Section III-C and III-D, respectively.

A. Delay-Time Tunable Design

The RAM shows a fast access time of 36 ns in the PSRAM mode, which is fast in the 1-Mbit level. Al shunted word lines, double bit-line structure, 16 divided bit lines, a dual boot system, and buffer registers [2] contribute to the high speed. However, a very important contribution comes from the use of delay-time tunable design. Generally, RAM's have many critical delay timings to determine the access time. Among them are, for example, in this RAM, enable timing of sense amplifiers and buffer registers, output buffer delay, internal refresh pulse width, and precharge time from refresh to normal operation. Every critical delay is designed to be tunable by means of a laser blow of the second-Al link as shown in Fig. 5. If the fuse is blown, the capacitance is cut off and delay is shortened. In the photograph, three of the fuses have been blown. In the first design the timing margins are set large and the access time is rather slow. When the chip is processed and functionality is verified, the timing margins are adjusted to shorten the access time by laser blow. The second Al is chosen because it blows easily and precisely compared with the other lower layers, for example, first Al or poly-Si. The space between second-Al links should be more than 5 μm to avoid a miss-blow. More than 90 percent of the links are successfully blown through the experiments.

In this way, the timing optimization can be carried out not only through simulation but also through experiments, which greatly enhances the precision of the optimization and also speeds up the development. When the optimization has been done, only the second-Al mask is to be modified. Chip-area penalty is less than 0.01 percent of the total chip area. This approach becomes important when the VLSI gets more complicated and the prediction of parasitic capacitance and resistance becomes more difficult.

B. Current-Mirror Timer

The RAM shows small data-retention current of 30 μA. This is accomplished by exclusion of self substrate bias circuit and by a novel current-mirror ring-oscillator timer for refresh as shown in Fig. 6. The timer is measured to

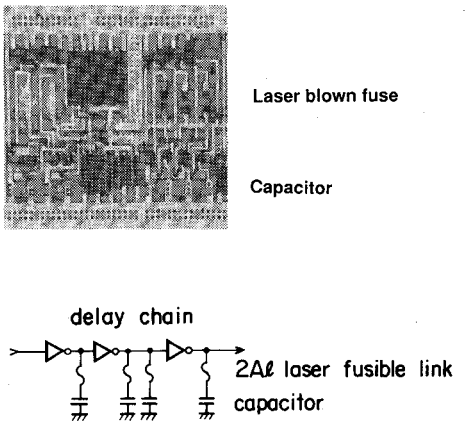

Fig. 5. Delay-time tunable design with laser-blown fuses. If the fuse is blown, the capacitance is cut off and delay is shortened. In the photograph, three of the fuses have been blown.

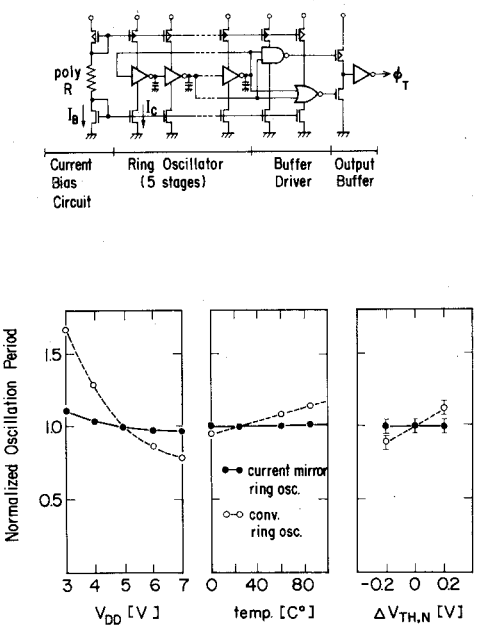

Fig. 6. Current-mirror ring-oscillator timer. The timer shows better stability than conventional ring oscillators.

show 6-μA current dissipation and much better stability over temperature, V_{th}, and V_{DD} fluctuation than a conventional ring-oscillator refresh timer. This is because the charging and discharging current is determined not by MOSFET's but by a poly-Si resistor whose resistance is in the order of megaohms. The circuit fits in a distributed refresh scheme, which is not the case for the formerly reported refresh timer [4]. Since the poly-Si resistor can be laid out under the V_{DD} or V_{SS} line without an extra mask to normal process flow, the area overhead is less than 0.1 percent of the total chip area.

This poly-R biasing scheme can be applied to any logic circuits that require stability over temperature, V_{th}, and V_{DD} fluctuation, and if the current bias control has a special dependence on temperature, V_{DD}, etc., the logic circuits reflect the dependence.

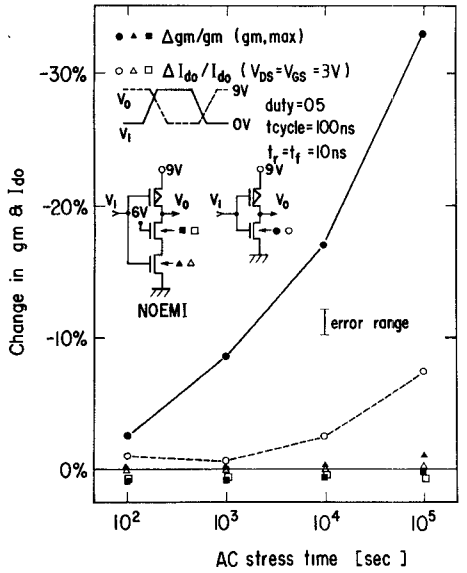

Fig. 7. Measured hot-carrier degradation under ac stress. The NOEMI structure has at least three orders of magnitude larger hot-carrier resistancy than the conventional inverter.

C. Hot-Carrier Resistant Circuit

The RAM employs 1-μm LDD NMOS and hot-carrier degradation is one of the keen issues. In order to ensure sufficient reliability, the RAM employs normally-on enhancement MOSFET insertion (NOEMI) circuit technology in every boosted nodes. The NOEMI is a circuit structure where serially connected MOSFET's relax the drain–source voltage of MOSFET to suppress hot-carrier generation as shown in Fig. 7. The figure shows the NMOSFET hot-carrier degradation cmparison between the conventional CMOS inverter and the NOEMI inverter under 9-V ac stress. Details of the experiments are in [5].

In the conventional inverter, after 10^5-s ac stress, the transconductance of the triode region and the drain saturation current show degradation of more than 30 and 7 percent, respectively. On the contrary, the NOEMI inverter shows no significant change. It is seen from the difference between degradations after 10^2 and 10^5 s in Fig. 7 that the NOEMI inverter has at least three orders of magnitude stronger resistancy to the hot carrier compared with the conventional inverter. Therefore, the NOEMI is indispensable to assure sufficient reliability for boosted nodes, where about 8-V ac stress is applied even if supply voltage is 5.5 V.

D. Arbiter Optimization

The metastability related with arbiters and synchronizers is one of the serious problems [6] that prevail in recent complex VLSI systems. However, the soft-error possibility due to metastability is sometimes overlooked in memory design, although the problematic circuits are included unconsciously. For example, arbiters are used to decide quit/continue operation of self-refresh in PSRAM's, and to eliminate a glitch whose pulse width is less than a certain value.

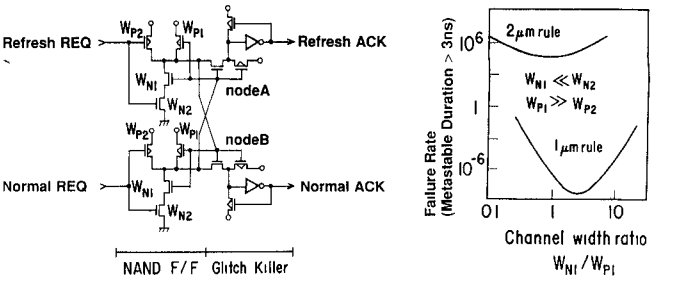

Fig. 8. Optimized arbiter with a CMOS glitch killer. For 1-μm MOSFET's, the optimum ratio for W_{N1}/W_{P1} shifts to about two, instead of the predicted value of unity by the simple model of Flannagan [7].

The present RAM includes a refresh-normal arbiter as shown in Fig. 8, which has a new CMOS glitch killer to prevent a malfunction in the metastable duration. In order to minimize the metastable duration, the optimization method is developed using a realistic model of SPICE2. The two NAND's are assumed to be symmetrical since it can be demonstrated that the asymmetry does not help the minimization.

First, nodes A and B are shorted with a dummy MOSFET and then the nodes are cut apart, followed by the exponential development of the voltage difference between nodes A and B. The coefficient of the exponential development is to be maximized by changing the MOSFET sizes. For 1-μm MOSFET's, the optimum ratio for W_{N1}/W_{P1} shifts to about two, instead of the prediction of unity from the simple model of Flannagan [7]. This is due to the velocity saturation by gate voltage. In addition to that, it is found that the larger W_{N2} is and the smaller W_{p2} is, the shorter the metastable duration [8]. As a result, 3 ns turns out to be enough to resolve the metastability when MOSFET sizes are optimized. The accelerated test shows that the error rate of the refresh-normal arbiter is less than 1 FIT, that is, negligibly small even in the worst condition, that is, at 4.5 V. However, careless design of arbiters is vital because the error rate depends exponentially on MOSFET sizes.

IV. Process Technology and Features

The fast operation is partly due to the double-Al process and an advanced 1-μm LDD NMOS with 1.2-μm basic design rule, whose parameters are listed in Table I. For NMOS poly gate 1.0 μm is used for high performance and 1.2 μm for the other layers is for high production yield. These are wafer values and gate length shows poly-Si width in a transistor, which differs from effective channel length L_{eff}. PMOS L_{eff} is measured to be 0.8 μm but NMOS L_{eff} cannot be precisely determined because of LDD type.

Memory cells are embedded in an isolated p-well [2] to be protected from minority carriers generated by I/O pins and α-particle hits. Fig. 9 shows a measured α-particle-induced soft error rate (SER) versus cycle time. As seen from the figure, the SER is limited by a cell mode. The unit of the vertical axis is arbitrary but is almost equal to

TABLE I
PROCESS PARAMETERS

Technology	Twin well CMOS with N-substrate
Memory cell	Parallel plate cap. in P-well
Layers	Double poly-Si & Double Al
Gate length	1.0μm(LDD NMOS) , 1.2μm(PMOS)
Cap./Gate oxide	10nm / 20nm
Poly-Si (Width/Space)	1.0μm / 1.6μm
1st Al (Width/Space)	1.2μm / 1.4μm
Contact hole	1.2μm x 1.2μm
2nd Al (Width/Space)	1.6μm / 1.8μm
Via hole	1.4μm x 1.6μm

TABLE II
PERFORMANCE LIST

Organization	128K words x 8bit
Chip size	5.60 x 13.07mm^2
Cell size	3.6 x 8.2μm^2
PSRAM access time	36ns
VSRAM access time	66ns
Operating current	30mA (t_{cycle}=160ns)
Self-refresh current	30μA (0 ~ 85°C)
Package	32pin 600mil DIP
Laser fuse redundancy	4 columns & 4 rows
Tolerable bump rate	±20%

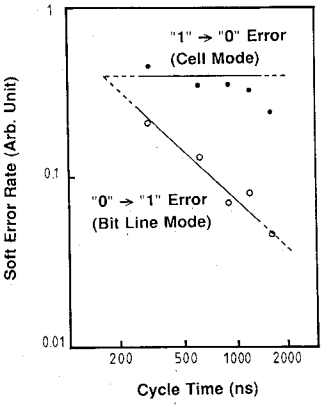

Fig. 9. α-particle-induced SER. The unit of vertical axis is almost equal to FIT.

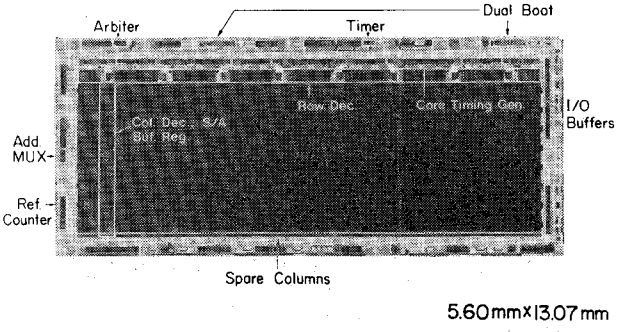

Fig. 10. Chip microphotograph of the RAM.

FIT. Therefore, the SER is 1-FIT order. The reasons for the low SER are threefold. As for a diffusion component of the α-particle-induced carriers, the p-well potential barrier is effective in rejecting the carriers and the small memory size reduces a capture cross section for the carriers. As for a drift component, high doping density of the p-well reduces the funneling effects.

Fig. 10 is a microphotograph of the chip. The features of the RAM are summerized in Table II. Chip size is 5.60×13.07 mm^2 and memory cell size is 3.6×8.2 μm^2. The peak current is about 100 mA and average typical operating current is 30 mA at 160-ns cycle time and data-retention current 30 μA in the temperature range from 0 to 85°C. The low data-retention current enables the RAM to be used for battery backup applications. Four spare columns and four spare rows are included to improve yield. Tolerable maximum bump rate is measured to be ±20 percent. Pin connection of the RAM is fully compatible with the conventional 1-Mbit PSRAM [1] and is also compatible with a 1-Mbit (128K×8) SRAM [9] except that the #1 pin of the RAM is used as an $\overline{RFSH}$ pin.

V. DISCUSSION

Before going to the conclusions, let us comment on the suitability of this device as a DRAM macro in logic environments. Memory-embedded logic IC's open a way to high-performance VLSI's. This is because a performance bottleneck exists usually on a memory bus, and the embedded memories minimize the bus communication delay. The reasons why this RAM fits for a DRAM macro are threefold. The first merit is that the RAM uses double-poly-Si and double-Al processes. Only one poly-Si layer is to be added onto the standard logic process to make this RAM embedded in the logic VLSI's. On the contrary, in case of triple-poly-Si and single-Al process DRAM's, two poly-Si layers should be added on. The second merit is the no substrate bias design. Usually, CMOS logic cells are not substrate biased. So the RAM is very suitable for macro libraries. The last point is about the VSRAM mode. The easy-to-use features of the VSRAM mode such as no refresh control aids in the easy RAM modeling for computer-aided design. All these merits make the RAM attractive as a DRAM macro used with various logic design.

The next discussion is on the functional differences between this device in VSRAM mode and the conventional SRAM. The first difference is the address access. The conventional SRAM allows the address access but this RAM should be used in synchronous mode, that is, only *CE* access is allowed. Usually when used with CPU, this constraint is not serious and rather preferable because the RAM has address latches inside thanks to this constraint.

The second difference is the data-retention voltage. Because memory cells of the RAM are one-transistor and one-capacitor type, large supply voltage bump can destory

stored data. Therefore, the data-retention voltage of the RAM is restricted to 5 V $\pm$10 percent. Since the data-retention current of the RAM is as small as 30 μA, it can be battery backed up even though the voltage should be higher than the conventional SRAM.

The third is maximum write pulse width. The RAM is designed to shut off a word line automatically at 10 μs after the RAM is accessed. It is for the internal background refresh so that WRITE operation should be finished in 10 μs, that is, maximum write pulse width is constrained up to 10 μs, although there is no limitation for READ cycle time and *CE* active time. Since the WRITE operation can be done at most in several hundred nanoseconds, this specification does not limit the application at all.

The last difference is in the initialization. In power-up, 1-ms initialization time in a standby mode is required before going into normal operation, which is not required for the conventional SRAM. For usual applications, this can be considered a minor difference.

As for a test aspect, the RAM includes a test mode in which an I/O pin outputs low when an internal refresh takes place.

VI. Conclusions

A 1-Mbit PSRAM with VSRAM mode is successfully developed. The PSRAM mode fits for high-speed applications. The VSRAM mode provides the easy-to-use features of SRAM's with the storage density of DRAM's. In this way, the RAM can meet a wide variety of user demands.

New circuit technologies are introduced to achieve easy-to-use feature, high speed, low power, and high reliability, that is, delay-time tunable design, a current-mirror timer, and arbiter optimization. These technologies are promising for advanced VLSI's.

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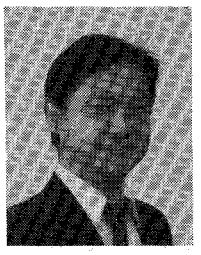

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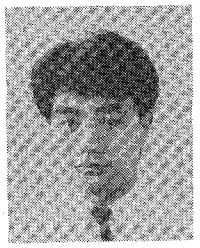

Katsuhiko Sato was born in Aomori, Japan, on November 17, 1959. He received the B.S. degree in electronic engineering from Shibaura Institute of Technology, Tokyo, Japan, in 1984.

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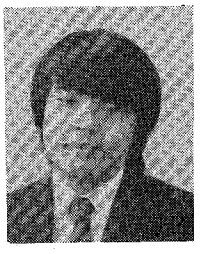
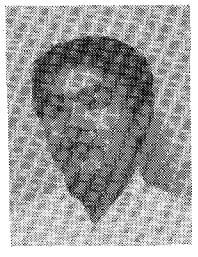


Tsukasa Shirotori was born in Nagano, Japan, on December 27, 1963. He received the B.S. degree in chemistry from Ikutoku University, Kanagawa, Japan, in 1986.

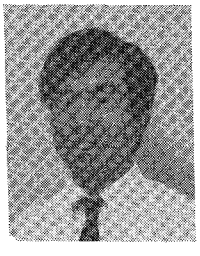
In 1986 he joined Toshiba Microcomputer Engineering Corporation, Kawasaki, Japan, and since May of 1986 he has been at the Toshiba Semiconductor Engineering Laboratory. He has been engaged in the research and development of CMOS LSI memory.



Masakazu Kakumu was born in Nagoya, Japan, on January 11, 1956. He received the B.S. and M.S. degrees, both in electrical engineering, from Waseda University, Tokyo, Japan, in 1979 and 1981, respectively.

In 1981 he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan. His initial research was in the silicide materials for application to CMOS VLSI's. Since 1983 he has been engaged in the development of advanced CMOS technologies.

Mr. Kakumu is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers of Japan.



Shigeru Morita was born in Tokyo, Japan, on September 21, 1955. He graduated from Koganei Industrial Senior High School, Tokyo, Japan, in 1974.

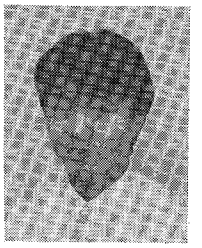
In 1974 he joined the IC Laboratory of the Toshiba Research and Development Center, Kanagawa, Japan, where he mainly studied chemical vapor deposition technology. Since December of 1978 he has been at the Toshiba Semiconductor Device Engineering Laboratory, studying the development of the fabrication process for nonvolatile ROM's and CMOS RAM's.

Mr. Morita is a member of the Japan Society of Applied Physics and Institute of Electronics, Information and Communication Engineers of Japan.

Masaaki Kinugawa was born in Hyogo Prefecture, Japan, on July 24, 1958. He received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1981 and the M.S. degree in applied physics from Tokyo University, Tokyo, Japan, in 1983.

In 1983 he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan. He has been engaged in the development of static RAM's, especially in process technologies and device physics of submicrometer MOSFET's.

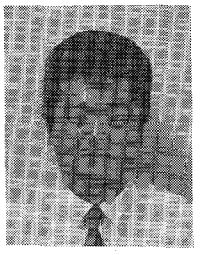
Mr. Kinugawa is a member of the Japan Society of Applied Physics.



Tetsuya Asami was born in Fukuoka, Japan, on January 25, 1966. He graduated from Chikushi Technical Senior High School, Fukuoka, Japan, in 1984.

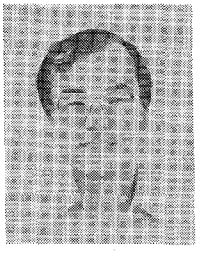
In 1984 he joined Toshiba Microcomputer Engineering Corporation, Kawasaki, Japan. Since October of 1984 he has been at the Toshiba Semiconductor Engineering Laboratory studying process technologies for static RAM's. He is now also studying electronic engineering at Tokai University.

Mr. Asami is a member of the Japan Society of Applied Physics.



Kazuhito Narita was born in Aomori, Japan, on August 29, 1967. He graduated from Towada Industrial Senior High School, Aomori, Japan, in 1986.

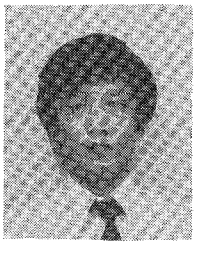
In 1986 he joined Toshiba Semiconductor Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan. He has been engaged in the development of advanced CMOS technologies, especially in isolation process. Now he is also engaged in the development of submicrometer EPROM's.



Jun-ichi Matsunaga was born in Oita Prefecture, Japan, on May 11, 1948. He received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1972 and the M.S. degree from the University of Tokyo, Tokyo, Japan, in 1974.

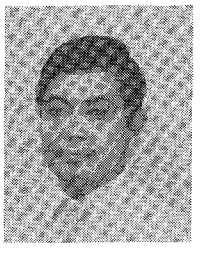
In 1974 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He had been engaged in development of dynamic RAM's and microprocessors, particularly in process characterization and device physics investigation. Since 1979 he has engaged in the deveopment of advanced CMOS process in the Semiconductor Device Engineering Laboratory (SDEL), Toshiba Corporation, Kawasaki, Japan. He developed 64K and 256K CMOS static RAM's. He is currently Manager of the advanced SRAM and EPROM process group of SDEL.

Mr. Matsunaga is a member of the Japan Society of Applied Physics.



Akira Higuchi was born in Kanagawa Prefecture, Japan, on February 10, 1957. He graduated from the Tokyo Technical College, Tokyo, Japan, in 1977.

In 1977 he joined the IC Memory Application Engineering Semiconductor Division, Toshiba Corporation, Kawasaki, Japan. He was engaged in the study of MOS memory application beginning in April of 1977. He is currently working on the development of video processing memories at the IC Memory Application Engineering Integrated Circuit Division, Toshiba Corporation, Kawasaki, Japan.



Mitsuo Isobe was born in Niigata Prefecture, Japan, on January 3, 1948. He received the B.S. and M.S. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1971 and 1973, respectively.

In 1973 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he has worked on the research and developmentt of NMOS/SOS LSI. From 1979 to 1987 he was engaged in the research and development of CMOS/SOS memory LSI and CMOS/bulk memory VLSI at the Semiconductor Device Engineering Laboratory. He is currently the Deputy Manager of the IC Memory Application Engineering Department, Integrated Circuit Division.

Tetsuya Iizuka (M'79) was born in Ibaraki, Japan, on April 17, 1947. He received the B.S. degree in applied physics, and the M.S. and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1970, 1972, and 1975, respectively.

In 1975 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in research on I^2L and CMOS/SOS devices and in the development of dynamic RAM testing methods. In 1979 he joined a newly organized laboratory, the Semiconductor Device Engineering Laboratory (SDEL), Toshiba Corporation. He developed first generations of 16K, 64K, 256K, and 1-Mbit CMOS SRAM's. He developed a new concept of SRAM called the virtually static RAM (VSRAM), an advanced concept of PSRAM which is based on the DRAM cell but usable as SRAM. A commercially available 1-Mbit VSRAM was developed. He also developed a high-speed 64K Bi-CMOS SRAM with bipolar sense amplifiers. He worked on new circuit techniques such as hot-carrier-resistant logics. In 1981 he stayed for one year at Integrated Circuit Laboratory, Hewlett-Packard Laboratories, Palo Alto, CA, as a Visiting Engineer. He studied CMOS latch-up modeling and bird's beak free isolation MOST analysis. He is currently Manager of the Memory Embedded Logic VLSI Design Group of the SDEL.

Dr. Iizuka is a member of the Institute of Electronics, Information and Communication Engineers of Japan. He has served as a Program Committee Member for the 1985, 1986, and 1987 Symposiums on VLSI Technology, and as Integrated Circuit Subcommittee Member of the 1985 and 1986 IEDM's.