Digital ICs with Embedded Memory

Synopses of Introductory Statements by Panelists

Large-scale integration of functionality into ASICs has led to greater use of embedded memories. To decrease logic design time, it's advantageous to maintain generators for configurable memories with flexible I/O interfaces. Wherever possible, the addition of built-in self-test to embedded memories can increase greatly their testability, while decreasing their test vector generation and testing costs. However, special features or asynchronous timing on the I/O interfaces may compound the testability problems. — *D.R. Aadsen*

It is becoming increasingly common for ASIC customers to use embedded memories in their designs to take advantage of the improved performance and functionality this affords. However, if the ASIC design system and methodology are inadequate, these memories can end up poorly simulated and virtually untestable. The selection of different memory organizations and sizes is quite limited in many ASIC libraries. A solution to this is memory compiler software on the engineering workstation, but with the increased flexibility comes potential for software errors and product engineering complexity. — *B. Barton*

As semiconductor geometries shrink and fabrication techniques improve, larger dies can be built and more devices can be integrated. All of this permit a system level integration at the chip level. Along with systems is a demand for embedded memories and functions. The performance gained in both speed and area can be significant, and a new set of disciplines is needed to handle the generation, testing, modeling, and use of these devices. — *S. Chan*

Embedded memories in a multi-chip RISC architecture such as that used in microprocessors allow the integration of special functions such as 2-way set associativity, full associativity, very wide word sizes, dual port and set and clear functions. Specialized logic such as multiplex and compare blocks can be integrated for high speed. Availability of clock signals in a synchronous environment allows the use of pre-charge techniques. Embedded modules lead to difficulties in debugging during development and in test and characterization later. Limited controllability and observability of address, data and control signals restrict the range of tests. For these and other reasons, conservative design techniques have been used, for example, using 6-transistor cells rather than resistor loads. Other applicable test approaches include built-in self-test and scan path. — *D. Draper*

VLSI chips which have large amounts of embedded memory present unique testing problems, both for test vector generation and test time. But, perhaps more importantly, most test approaches in use today only verify the dc functionality of the bits. For large arrays embedded in fast logic/processor applications, measuring the ac performance or detecting *soft* failures is required. This requires a dedicated path for high speed memory-type testers to access directly the array as a separate functional module. This is a major challenge for circuit designers and test engineers to ensure that the quality and reliability of the embedded memory is equal to that of commercial memory chips. — *P. Reed*

Access time of a cache is usually set 1/3 of the time span from when a CPU sets an address and to when the CPU obtains the data. The remaining 2/3 are for I/O pin delay and peripheral IC delay. Embedding can optimize this absurd delay distribution and also solve memory chip problems related to V_{IL}/V_{IH}, ESD, and output noise. Design compatibility and tunability are important since a memory design can be compared to a subroutine in a software library that can be used for many other chip designs. — *T. Sakurai*

D.R. Aadsen

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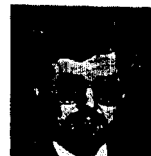
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