Optimization of CMOS Arbiter and Synchronizer Circuits with Submicrometer MOSFET's

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Abstract—**This paper deals with an optimization method and results for CMOS arbiter and synchronizer circuits with submicrometer geometry. A convenient optimization method is described using a circuit simulator SPICE2 with realistic models for short-channel MOSFET's and capacitances. By using this method, MOSFET size optimization is carried out and it is found that the optimum size ratio of NMOS versus PMOS shifts from the simple theory of Flannagan [22]. NMOS size should be larger than PMOS size. This is due to the velocity saturation of carriers in short-channel MOSFET's. The effects of the parasitic PMOS and NMOS sizes, supply voltage, and temperature are also considered. It is also shown that asymmetry of the cross-coupled NAND's and insertion of cascaded inverters do not help the optimization.**

I. Introduction

IN RECENT VLSI's, arbiters and synchronizers have been used quite frequently [1]–[3]. These circuits have been pointed out to have a probabilistic error mode, called a metastability problem. For example, in an arbiter, if two request signals occur simultaneously, the arbiter cannot decide for a while which of the two requests is to be acknowledged. However, this problem is sometimes overlooked, for example, in designing the stop/continue decision circuit of self-refresh of pseudostatic RAM's, input latches, and some glitch killers which cut off pulses whose pulse width is larger than a certain width.

Some may think that this problem can be solved by a system-level design, but every solution is only a shift of the problem from one circuit to another circuit. It is like the paradox of the goat starved to death between two haystacks. The goat wants to go and eat the larger haystack first, but if the two stacks seem equal, there is a possibility that he will die because of too long a decision delay.

The metastability problem in electronic circuits was first suggested by Carr [4] and experimentally demonstrated by Chaney *et al.* [5]–[7]. After that, many works were reported on the theoretical basis [8], on the experimental basis [9]–[13], and on both bases [14]–[19]. Veendrick [20] showed that the metastability problem is independent of noise and is quite essential. This is because although in some cases the metastable state is resolved by a noise, there is the same amount of chance of going into a metastable state by the noise. The above-mentioned earlier works are all on discrete SSI's such as SN7400 families. Since these discrete IC's are already designed and in production, their interests are mainly in the characterization of the problem. The one exception is [8] which is purely theoretical.

Recently, however, the interest of this field has changed from characterization to optimization [20]–[23], because, in VLSI designs, it is possible to choose any MOSFET size in designing arbiters and synchronizers. Some of the papers treated NMOS circuits [20], [21], but CMOS has become a mainstream in VLSI implementation. For CMOS circuits, Flannagan [22] carried out the optimization by a very simple MOS model. The work is valuable in the sense that it first gave a comprehensive view to the optimization strategy. However, the result is not practically satisfactory because MOS and capacitance models are much too simplified. As for the analysis method, the previously reported works employed rather complicated analytical approaches [20], [21], [23], which are not easy to use in designing a specific VLSI.

In this paper, a simple optimization method is described based on widely used SPICE2 simulation [24]. MOS and capacitance models can be precise and the method can be applied to any circuit environment. By applying the method, an optimization is carried out for short-channel MOSFET's and it is shown that the optimum size of the arbiter/synchronizer shifts from the value calculated by Flannagan [22]. The effects of the parasitic PMOS and NMOS sizes, supply voltage, and temperature are also considered. It is shown that asymmetry of the cross-coupled NAND's and insertion of cascaded inverters do not help the optimization.

An optimization method is described in Section II and the choice of circuit configuration is discussed in Section III. Optimization results for short-channel MOSFET's are given in Section IV and the reason why the optimum design shifts from the simple model is given in Section V. Sections VI and VII are dedicated to considerations and conclusions, respectively.

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II. Metastable State Duration Minimization Method

Fig. 1 shows a popular cross-coupled CMOS NAND arbiter [1]–[3] with a CMOS glitch killer. Usually the essential part of an arbiter/synchronizer is this cross-coupled NAND/NOR gate even if the total circuit is complex. The glitch killer suppresses an undesired pulse in a metastable duration, but it does not mean to completely solve the problem. If the metastable duration is long, errors can occur in the system level. So the metastable state duration should be as short as possible.

In order to minimize the metastable state duration, an optimization method is proposed using realistic models of SPICE2. SPICE2 provides satisfying models for short-channel MOSFET's (MOS level 3 model) and capacitances. The method is described by using Fig. 2. Here, a cross-coupled CMOS NAND arbiter is used as an example, but the method is applicable to NOR-type and/or E/D-type circuits. The method is also applicable to the case where there are considerable fan-out circuits to an arbiter/synchronizer, although many fan-outs turn out to degrade the error probability.

First, output nodes of cross-coupled NAND's, Out1 and Out2, are shorted by a dummy MOSFET (expressed as a switch in Fig. 2(a)). The mobility of the dummy MOSFET is set physically impossibly large and the channel width is set very small so as to reduce the coupling capacitance to a negligible level although the shorting is perfect. The use of the MOSFET is a trick to emulate a switch, and in SPICE3, the trick is not needed because a switch model is already implemented as a standard element [25]. The nodes Out1 and Out2 are then cut apart, followed by an increase of voltage difference between the nodes Out1 and Out2 as shown in Fig. 2(b). The voltage-difference resolution (expansion) is strictly exponential as shown in Fig. 2(c). The so-called metastable state is an initial stage of the resolution process as is indicated in Fig. 2(b).

In order to minimize the metastable state duration and to minimize the error rate related to the metastable state, the coefficient of the exponential resolution is to be maximized by changing the MOSFET sizes. It is easy to calculate the exponential coefficient from a SPICE2 output file by using the programming language "awk" in Unix [26].

A formerly reported simulation technique to obtain the exponential slope is by adjusting the timing of the two request inputs and generating a metastable state [21]. However, it is cumbersome to find out the proper timing, because the timing adjustment is very subtle and 0.01 ns of misadjusting fails to generate the metastable state long enough to calculate the exponential coefficient.

III. Choice of Optimum Circuit Configuration

The two NAND's in Fig. 2(a) are assumed to be symmetrical since it can be demonstrated as follows that asymmetry does not help the optimization. The essential part of an

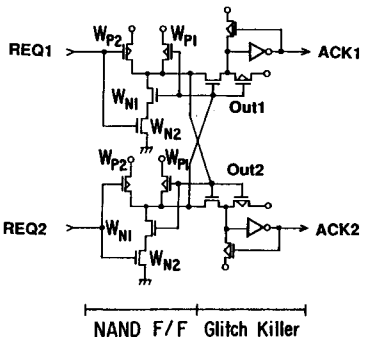

Fig. 1. Widely used cross-coupled CMOS NAND arbiter with CMOS glitch killer.

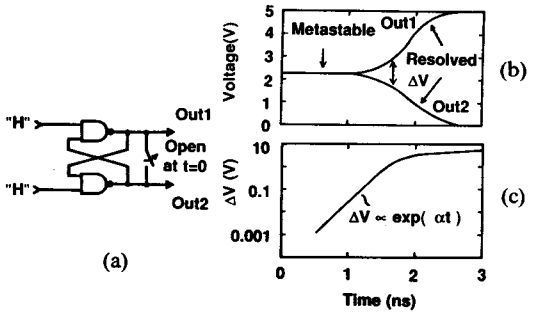

Fig. 2. Optimization method. (a) Output nodes of cross-coupled NAND's, Out1 and Out2, are shorted by a dummy MOSFET whose mobility is set physically impossibly large. (b) The nodes are then cut apart followed by the voltage difference increase. (c) The development of the voltage difference is strictly exponential in a metastable state.

arbiter/synchronizer is cross-coupled inverters as shown in Fig. 3(a). This inverter corresponds to a circuit consisting of MOSFET's $N1$ and $P1$ in Fig. 1. The MOSFET's $N2$ and $P2$ are rather parasitic devices for resolution process.

In Fig. 3(a), an equivalent circuit of the cross-coupled inverter is also shown. V_m is a metastable voltage and about 2.3 V in the case of Fig. 2(b). g_m signifies an equivalent transconductance of the inverter near the metastable voltage. V_1 and V_2 are output voltages of the inverters 1 and 2, respectively. The parasitic capacitances of the output nodes are denoted as C_1 and C_2. The differential equations which govern the voltage expansion are as follows:

$$\begin{cases} C_1 \dfrac{dV_1}{dt} = -g_{m1}(V_2 - V_m) & \text{(1a)} \\ C_2 \dfrac{dV_2}{dt} = -g_{m2}(V_1 - V_m). & \text{(1b)} \end{cases}$$

From these equations, the resolution of the voltage difference, ΔV ($= V_1 - V_2$), is expressed as

$$\Delta V = \Delta V_{init} \exp(\alpha t) \quad \text{(2a)}$$

$$\alpha = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \quad \text{(2b)}$$

where ΔV_{init} is initial voltage difference at $t = 0$. This expression suggests that the parasitic capacitance of the

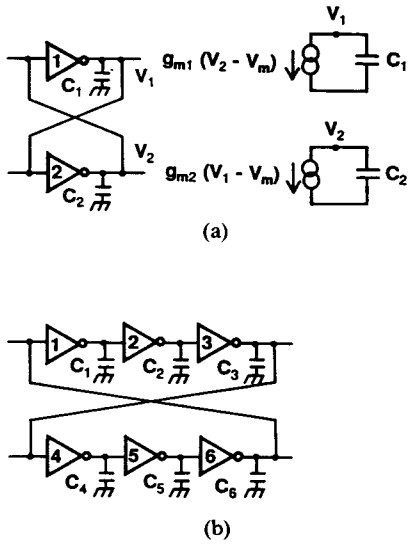

Fig. 3. Configuration choice. (a) Cross-coupled asymmetrical NAND's and equivalent circuit. (b) Arbiter/synchronizer with inserted inverters.

output node should be as small as possible and that the conductance of the inverter should be as large as possible to improve the resolution characteristics of the circuit. More concretely, an arbiter/synchronizer should be designed with large transistor sizes and the next gates, in other words, fan-out gates, should be designed using small transistor sizes.

The calculation method of the error rate from the resolution coefficient (expansion factor) has been given by Veendrick [20]. By using the above-mentioned formula, the error rate is written as

failure frequency per year

$$= 2y \cdot f_1 \cdot f_2 \frac{\Delta V_{\text{final}}}{V_{DD}} t_T \cos(-\alpha t_W) \quad (3)$$

where y is seconds per year ($= 31.5 \times 10^6$) and f_1 and f_2 are frequencies of two asynchronous clocks, that is, the frequencies of two requests for arbiters, and data and latch clock frequencies for synchronizers. ΔV_{final} is the voltage difference at which the next gate acknowledges that the metastable state resolution is completed, usually about 2–3 V. V_{DD} is a supply voltage and t_T is a transient time of the two asynchronous clocks. t_W is a system wait time assigned to an arbiter/synchronizer to fully resolve the voltage difference.

Denoting the size of the inverter as x_1 and x_2, the following expressions hold:

$$\begin{cases} C_1 = k_{CG}x_2 + k_{CJ}x_1 & (4a) \\ C_2 = k_{CG}x_1 + k_{CJ}x_2 & (4b) \\ g_{m1} = k_{GG}x_1 & (4c) \\ g_{m2} = k_{GG}x_2 & (4d) \end{cases}$$

where k_{CG} and k_{CJ} are gate capacitance and junction capacitance proportional constant, respectively, and k_{GG} is transconductance proportional constant. By substituting (4a)–(4d) for (2b), the resolution coefficient (expansion factor) α yields

$$\frac{1}{\alpha} = \frac{1}{k_{GG}} \left[k_{CG}^2 + k_{CJ}^2 + k_{CG}k_{CJ} \left(\frac{x_2}{x_1} + \frac{x_1}{x_2} \right) \right]^{1/2} \quad (5)$$

Then, the resolution coefficient α takes its maximum at $x_1 = x_2$, that is, when two inverters are symmetrical. The maximum value of α, α_{MAX}, is given as follows:

$$\alpha_{\text{MAX}} = \frac{g_{m1}}{C_1} = \frac{g_{m2}}{C_2} = \frac{k_{GG}}{k_{CG} + k_{CJ}}. \quad (6)$$

Another design choice is insertion of inverters in the cross-coupled loop as shown in Fig. 3(b). This configuration might help the resolution coefficient because the gain of the loop is increased. A similar treatment of the circuit leads to the resolution coefficient expressed as

$$\alpha = \left(\frac{g_{m1}g_{m2}g_{m3}g_{m4}g_{m5}g_{m6}}{C_1C_2C_3C_4C_5C_6} \right)^{1/6} \quad (7)$$

where g_{mi} and C_i denote transconductance and capacitance of the ith inverter, respectively. Corresponding to (4a)–(4d), these quantities can be written as

$$\begin{cases} C_i = k_{CG}x_{i+1} + k_{CJ}x_i, & (8a) \\ g_{mi} = k_{GG}x_i, \quad i = 1,2,3,4,5,6 & (8b) \end{cases}$$

where $i = 7$ is defined as $i = 1$. By substituting (7) with (8a) and (8b), α is rewritten as

$$\frac{1}{\alpha} = \frac{1}{k_{GG}} \left[\prod_{i=1}^{6} \left(k_{CG} \frac{x_{i+1}}{x_i} + k_{CJ} \right) \right]^{1/6}. \quad (9)$$

Differentiating this equation in x_i, the maximum value of the resolution coefficient α, α_{MAX}, is obtained as

$$\alpha_{\text{MAX}} = \frac{k_{GG}}{k_{CG} + k_{CJ}} \quad (10)$$

when all inverter sizes are equal. This value coincides with the maximum value of α without inserted inverters (see (6)). So it is useless to insert the inverter chains to improve the metastable problem. Since this type of inverter chain is easy to oscillate, the best configuration for an arbiter/synchronizer is the circuit given in Fig. 3(a) and Fig. 1.

IV. Optimum Design with Short-Channel MOSFET's

Optimization procedure is carried out using the method described in the previous section. The results are shown in Fig. 4. The essential part of an arbiter/synchronizer is cross-coupled inverters consisting of MOSFET's $N1$ and $P1$. As shown in Fig. 4(a), the optimum value of the size ratio of these MOSFET's, W_{N1}/W_{P1}, is about 2 for 1-μm MOSFET's, instead of the prediction of unity by Flannagan's simple analytical model [22]. This is because the velocity saturation of MOS transistors and the mobility

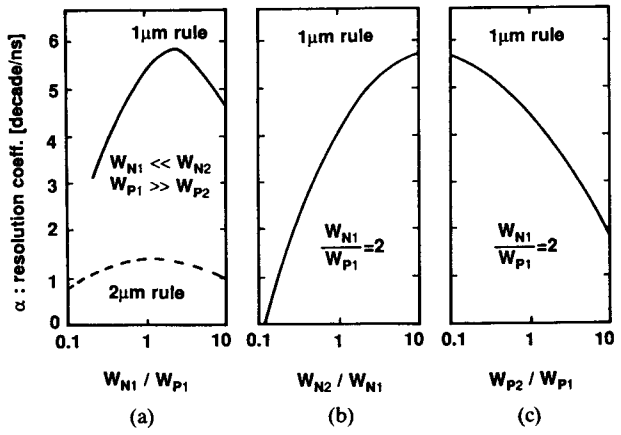

Fig. 4. Optimization with short-channel MOSFET's. (a) Resolution coefficient dependence on channel width ratio of NMOS and PMOS. For 1-μm MOSFET's, a larger size should be chosen for NMOS and PMOS. (b) Resolution coefficient dependence on channel width of serially inserted NMOS W_{N2}. The larger W_{N2}, the better. (c) Resolution coefficient dependence on channel width of parallel added PMOS W_{P2}. The smaller W_{P2}, the better.

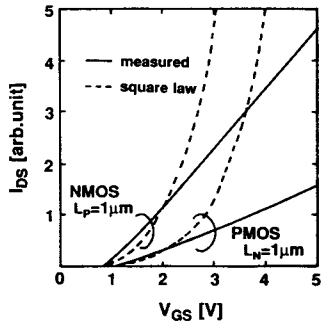

Fig. 5. Drain current characteristics of short-channel MOSFET's. The dependence of I_{DS} on gate–source voltage V_{GS} is not in square law but rather in nth power where $1 < n < 1.5$ due to velocity saturation by gate voltage.

of NMOS are larger than those of PMOS. A detailed discussion of the relationship between the velocity saturation and the optimum W_{N1}/W_{P1} shift is given in the next section.

Anyway, the size of NMOS should be chosen larger than that of PMOS to improve the resolution speed in the submicrometer regime. Near the optimum point of W_{N1}/W_{P1}, the curve is smooth and the value of the resolution coefficient does not change drastically even if process fluctuation occurs. However, if the design is not done optimally and process fluctuation takes place, the circuit becomes unstable since the error rate depends exponentially on α (see (3)), that is, the size of the MOSFET's.

MOSFET's $N2$ and $P2$ are rather parasitic elements to arbitration and synchronization operation and do not help to resolve the voltage difference between the nodes Out1 and Out2. Rather, they hinder the resolution process. Therefore, the size of $N2$, W_{N2}, should be large and the size of $P2$, W_{P2}, should be small as is shown in Fig. 4(b) and (c). If W_{N2} is small, the equivalent transconductance becomes small and if W_{P2} is large, the parasitic capacitance of the output nodes becomes large and degrades the resolution coefficient.

V. Cause of Optimum W_{N1}/W_{P1} Shift from Simple Model

As is mentioned in the last part of the previous section, the essential parts of the arbiter/synchronizer in Fig. 2(a) are reduced to the cross-coupled inverters shown in Fig. 3(a). In Fig. 3(a), the output voltages V_1 and V_2 are the same in the metastable state. That is, the output and the input voltage of the inverter are the same and the MOSFET's in the inverter are operated in a saturated region. Taking these circumstances into account, an input–output shorted inverter is analyzed in this section without degrading the precision.

Fig. 5 shows measured drain current characteristics of short-channel MOSFET's. The horizontal axis is gate–source voltage. It is seen from the figure that the curves do not fit in the classical square law employed by Flannagan. Rather, the drain current of PMOS, I_P, and that of NMOS, I_N, are expressed in the following manner:

$$\begin{cases} I_P(V_{\text{OUT}}) = K\mu_P W_{P1}(V_{DD} - V_{\text{OUT}} - V_{TP})^{n_P} & \text{(11a)} \\ I_N(V_{\text{OUT}}) = K\mu_N W_{N1}(V_{\text{OUT}} - V_{TN})^{n_N} & \text{(11b)} \end{cases}$$

where V_{OUT} is the output voltage of the inverter, V_{DD} is supply voltage, μ_P, μ_N are the effective mobilities for PMOS and NMOS, W_{P1}, W_{N1} are the channel widths of PMOS and NMOS, and V_{TP}, V_{TN} are the threshold voltages of PMOS and NMOS, respectively. Classically, both n_P and n_N are equal to 2 but decrease toward 1 for short-channel MOSFET's because of the velocity saturation of carriers by gate voltage. K is a proportional constant and classically equals $(\epsilon_{ox}/2t_{ox}L_{\text{eff}})$, where ϵ_{ox} is a dielectric constant of gate oxide, t_{ox} is gate oxide thickness, and L_{eff} is effective channel length. The metastable state voltage V_m and the transconductance of the inverter g_m near V_m are calculated as follows:

$$\begin{cases} I_P(V_m) = I_N(V_m) & \text{(12a)} \\ g_m = \left[\dfrac{d(I_N(V_{\text{OUT}}) - I_P(V_{\text{OUT}}))}{dV_{\text{OUT}}}\right]_{V_{\text{OUT}} = V_m}. & \text{(12b)} \end{cases}$$

Since the output node capacitance C is proportional to $W_{P1} + W_{N1}$, the resolution coefficient α reads

$$\alpha = \frac{g_m}{C} \propto \frac{g_m}{W_{P1} + W_{N1}}. \quad \text{(13)}$$

The aim is to maximize α by varying W_{P1} and W_{N1}. For simplicity, $n_P = n_N = n$ and $V_{TP}/V_{DD} = V_{TN}/V_{DD} = v_T$ are assumed without much degrading the approximation. Then,

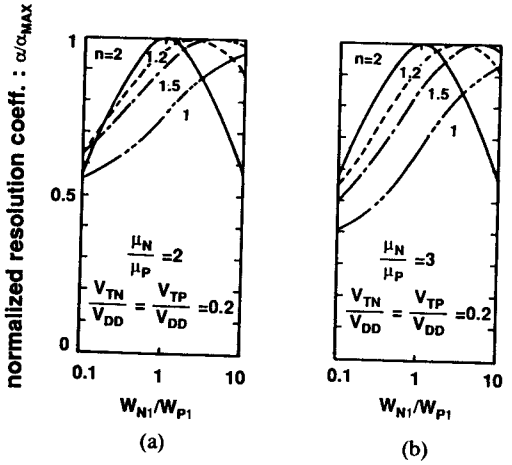

Fig. 6. Optimum W_{N1}/W_{P1} which gives the maximum resolution coefficient. The resolution coefficient is calculated by using (14a)–(14d), and normalized with its maximum value. (a) For the case where μ_N/μ_P is 2. (b) For the case where μ_N/μ_P is 3. The optimum W_{N1}/W_{P1} shifts from unit to infinity as n decreases from 2 to 1.

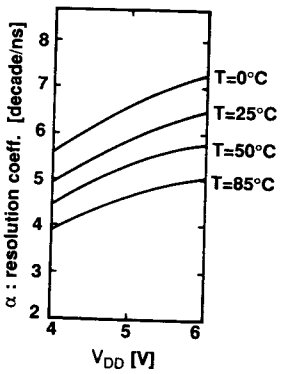

Fig. 7. Dependence of resolution coefficient α on supply voltage V_{DD} and temperature.

α is expressed as follows using (11)–(13):

$$\alpha \propto \frac{1}{1+W_R}\left[\mu_R W_R (v_m - v_T)^{n-1} + (1 - v_m - v_T)^{n-1}\right] \tag{14a}$$

$$v_m = \frac{V_m}{V_{DD}} = \frac{1 - v_T + \mu_R^{1/n} W_R^{1/n} v_T}{1 + \mu_R^{1/n} W_R^{1/n}} \tag{14b}$$

$$W_R = \frac{W_{N1}}{W_{P1}} \tag{14c}$$

$$\mu_R = \frac{\mu_N}{\mu_P}. \tag{14d}$$

For the classical case where $n = 2$, the resolution coefficient α is simplified as follows:

$$\alpha \propto \frac{\sqrt{W_R}}{W_R + 1} \tag{15}$$

so that α reaches its maximum value when W_R $(= W_{N1}/W_{P1})$ is 1. This coincides with the result given by Flannagan.

For the extreme case where $n = 1$, α is calculated as follows:

$$\alpha \propto \frac{\mu_R W_R + 1}{W_R + 1}. \tag{16}$$

Then α reaches its maximum value when W_R $(= W_{N1}/W_{P1})$ is infinity, since μ_R $(= \mu_N/\mu_P)$ is greater than unity. Physically, it is understood like this. When W_{N1} is large, the metastable voltage V_m moves down. If $n = 2$, this causes the transconductance degradation of NMOS. Therefore, there exists an optimum point for W_{N1}/W_{P1}. However, in the extreme case of n being 1, even if V_m moves down, the transconductance of the inverter remains unchanged. The transconductance of the inverter becomes large when the size of NMOS is large, and this means that the larger W_{N1}, the better.

For the intermediate case where $1 < n < 2$, numerical results are given in Fig. 6. It is seen from the figure that optimum value of W_R $(= W_{N1}/W_{P1})$ which gives the peak of α shifts from 1 to ∞ when n decreases from 2 to 1. For the case where $n = 1.2$ and $\mu_N/\mu_P = 2$, the optimum value of W_{N1}/W_{P1} is about 2. This corresponds to the case of Fig. 4(a).

From the discussion above, it is concluded that the velocity saturation in short-channel MOSFET causes the incremental shift in the optimum size ratio of MOSFET's. For MOSFET's with submicrometer geometry, the size of NMOS should be larger than that of PMOS in arbiter/synchronizer design.

VI. Other Considerations

Fig. 7 shows the dependence of the resolution coefficient α on temperature and supply voltage V_{DD}. The unit of the resolution coefficient is in decades per nanosecond. This means that the voltage difference of the output nodes of an arbiter increases 10^{α} times every 1 ns. For example, if the temperature is 25°C, and if the supply voltage changes from 5 to 4 V, then the resolution coefficient decreases from 6 to 5 decade/ns. If a system always waits 5 ns for an arbitration, that is, $t_W = 5$ ns, a 1-V decrease in supply voltage corresponds to the increase of error probability by a factor of $10^{6\ \text{decade/ns} \times 5\ \text{ns}}/10^{5\ \text{decade/ns} \times 5\ \text{ns}} = 10^5$, which is derived from (3). So the temperature and supply voltage fluctuation should be taken into account to determine the system wait time for arbitration/synchronization. As seen from the figure, the worst condition occurs when voltage is low and temperature is high, where transconductance of the resolving inverters shows the smallest value.

The next consideration is scalability of the metastable problem. As seen from (3), the system wait time t_W required for arbitration/synchronization with sufficiently small failure rate is inversely proportional to the resolution coefficient α. Therefore, t_W is proportional to C/g_m. This quantity has the same dependence as a general circuit delay. So the ratio of the arbitration/synchronization de-

lay to the system cycle time is essentially unchanged even if the design rules are shrunk. However, since the number of arbiters/synchronizers used in a system increases and clock frequency increases, a gradual increase in the failure rate will result. This causes the design of the arbiter/synchronizer to be more carefully done.

VII. Conclusions

A simple optimization method for minimizing the error probability of arbiters/synchronizers is proposed based on SPICE2 simulation. The optimization method is applicable to general arbiter/synchronizer designs used in various VLSI environments. Optimization procedure is carried out for short-channel MOSFET's.

The following design strategy is shown to minimize the metastable state duration, in other words, error probability. For the essential inverter part, the size of the NMOS transistor should be larger than the size of the PMOS transistor, in the submicrometer regime. For parasitic MOSFET's, the serially inserted MOSFET should be as large as possible and the parallel added MOSFET should be as small as possible. Another consideration is that the parasitic capacitance of the output nodes should be as small as possible. In other words, the arbiter/synchronizer is to be designed with large transistor sizes and the next gates, in other words, the fan-out gates, are to be designed using small transistor sizes.

Careless design of an arbiter/synchronizer is dangerous because the error probability depends exponentially on MOSFET size.

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References

[1] F. E. Barber, D. J. Eisenberg, G. A. Ingram, M. S. Strauss, and T. R. Wik, "A 2K×9 dual port memory," in *ISSCC Dig. Tech. Papers*, Feb. 1985, pp. 44–45.

[2] T. Sakurai *et al.*, "A 1Mb virtually static RAM," in *ISSCC Dig. Tech. Papers*, Feb. 1986, pp. 252–253; also *IEEE J. Solid-State Circuits*, vol. SC-21, no. 5, pp. 662–669, Oct. 1986.

[3] T. Sakurai *et al.*, "A 36ns 1Mbit pseudo SRAM with VSRAM mode," in *Proc. Symp. VLSI Circuits*, May 1987, pp. 45–46.

[4] I. Carr, "Time loss through gating asynchronous logic signal pulses," *IEEE Trans. Electron. Comput.*, vol. EC-15, pp. 108–111, Feb. 1966.

[5] T. J. Chaney and W. M. Littlefield, "The glitch phenomenon," Computer System Lab., Washington Univ., St. Louis, MO, Tech. Memo. 10, Dec. 1966.

[6] T. J. Chaney, S. M. Ornstein, and W. M. Littlefield, "Beware the synchronizer," in *Proc. COMPCON*, Sept. 1972, pp. 317–319.

[7] T. J. Chaney and C. E. Molnar, "Anomalous behavior of synchronizers and arbiter circuits," *IEEE Trans. Computers*, vol. C-22, pp. 421–422, Apr. 1973.

[8] L. R. Marino, "General theory of metastable operation," *IEEE Trans. Computers*, vol. C-30, no. 2, pp. 107–115, Feb. 1981.

[9] G. Elineau and W. Wiesbeck, "A new J-K flip-flop for synchronizers," *IEEE Trans. Computers*, vol. C-26, no. 12, pp. 1277–1279, Dec. 1977.

[10] W. Fleischhammer and O. Dortek, "The anomalous behavior of flip-flops in synchronizer circuits," *IEEE Trans. Computers*, vol. C-28, no. 3, pp. 273–276, Mar. 1979.

[11] F. Rosenberger and T. J. Chaney, "Flip-flop resolving time test circuit," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 4, pp. 731–738, Aug. 1982.

[12] T. J. Chaney, "Measured flip-flop response to marginal triggering," *IEEE Trans. Computers*, vol. C-32, no. 12, pp. 1207–1209, Dec. 1983.

[13] T. Okamoto and T. Abeyama, "Measurement of device parameters characterizing metastable operation of TTL-NAND latch," *IECE Japan*, vol. J68-D, no. 8, pp. 1545–1546, Aug. 1985.

[14] G. R. Couranz and D. F. Wann, "Theoretical and experimental behavior of synchronizers operation in the metastable region," *IEEE Trans. Computers*, vol. C-24, no. 6, pp. 604–616, June 1975.

[15] M. Pechoucek, "Anomalous response times of input synchronizers," *IEEE Trans. Computers*, vol. C-25, no. 2, pp. 133–139, Feb. 1976.

[16] C. Mead and L. Conway, *Introduction to VLSI Systems*. Reading, MA: Addison-Wesley, 1980.

[17] G. Lacroix, P. Marchegay, and P. Nouel, "Critical triggering of integrated flip-flops in synchronizer circuits," *Int. J. Electron.*, vol. 49, no. 3, pp. 179–184, 1980.

[18] G. Lacroix, P. Marchegay, and N. Hossri, "Prediction of flip-flop behavior in metastable state," *Electron. Lett.*, vol. 16, no. 9, pp. 725–726, Sept. 1980.

[19] T. Okamoto and T. Abeyama, "Estimation of metastable operations for NAND latches," *IECE Japan*, vol. J68-D, no. 6, pp. 1210–1217, July 1985.

[20] H. J. M. Veendrick, "The behavior of flip-flops used as synchronizers and prediction of their failure rate," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 2, pp. 169–176, Apr. 1980.

[21] J. H. Hohl, W. R. Larsen, and L. C. Schooley, "Prediction of error probabilities for integrated digital synchronizers," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 2, pp. 236–244, Apr. 1984.

[22] S. Flannagan, "Synchronization reliability in CMOS technology," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 880–882, Aug. 1985.

[23] T. Kacprzak, A. Albiki, and T. A. Jackson, "Design of N-well CMOS flip-flops with minimum failure rate due to metastability," in *Proc. IEEE ISCAS*, 1986, pp. 765–767.

[24] L. W. Nagel, "A computer program to simulate semiconductor circuits," Univ. of Calif., Berkeley, ERL Memo. ERL-M75/520, May 1975.

[25] T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE 3A7 User's Guide*, Univ. of Calif., Berkeley, Mar. 1986.

[26] A. V. Aho, B. W. Kernighan, and P. J. Weinberger, "Awk—A pattern scanning and processing language," in *Unix Manual*, Bell Lab., Murray Hill, NJ.

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