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A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM

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Abstract

A 1Mbit DRAM is embedded in 72K raw gates channelless gate array with 1.0μm HC²MOS twin well technology. The DRAM design is optimized for embedding, such as the adoption of no substrate bias design and p-well protected n-channel memory cells. The typical delay time of the gate array is 0.4ns and the worst case access time of the DRAM is 60ns.

I. Introduction

Recently, high-density channelless gate arrays up to 130K raw gates are announced[1] to realize a large system on a single chip. In many systems, however, the heaviest intra-chip traffic exists in a memory-bus. This memory-bus bottleneck can not be mitigated by merely integrating many logic gates on a chip. Only embedded memory approach can solve the problem and system speed can be greatly enhanced since the intra-chip communication delay of the order of 10ns is eliminated. Some gate arrays offer medium size SRAM on a chip, say 8Kbit[2], but it is not sufficient for audio/video use and many CPU applications.

In this paper, in order to overcome this memory-bus bottleneck and to save the board area, a high-density DRAM of 1Mbit is embedded in a 72K CMOS channelless gate array. DRAM operation has been considered as unstable or subtle, but once the tuning is completed, the DRAM can have wide margins, even tolerates 3V-5V voltage bumps, and can be embedded in tough environments like in gate arrays.

II. Embedded DRAM Design

The features preferable for the embedded DRAM are not always the same as the standard DRAMs. The unique design aspects of the present embedded DRAM, are summarized as compared with the case of the standard DRAMs. The measures for protecting an embedded DRAM from the adjacent gate array noise are also mentioned.

(1) Double poly-Si and double Al design is employed for process compatibility with the gate array. Process steps for depletion implant, thin oxide and cell plate patterning are to be added and the RAM needs extra 3 masks over the standard HC²MOS process. On the contrary, in case of triple poly-Si and single Al process DRAMs, two poly-Si layers should be added on to the normal logic process.

(2) In standard DRAMs row address and column address are multiplexed and controlled by $\overline{RAS}$ and $\overline{CAS}$. In this DRAM, address is not multiplexed for easier interface and higher speed. This no address-multiplexed mode is called a Pseudo Static RAM (PSRAM) mode.

(3) Many DRAMs have n-channel memory cells in p-substrate with minus bias. No substrate bias design is adopted for compatibility with the ordinary logic and n-channel memory cells are embedded in a protecting p-well as is mentioned in item (6).

(4) Virtually Static RAM (VSRAM) mode[3,4] other than the PSRAM mode is introduced. In the VSRAM mode, all the refresh related operations are done fully automatically and the users are freed from the cumbersome refresh control. Sometimes the design of the refresh control circuit by a gate array is beyond CAD limit. The VSRAM mode is also beneficial for easier RAM modeling for logic simulation.

(5) The RAM also supports a modified VSRAM mode, where the RAM outputs an automatic internal refresh timing as a BUSY signal. If this BUSY signal is applied to HOLD pin of a CPU, the refresh timing overhead is minimized.

(6) It is important to protect a DRAM macro form the noise generated in the gate array part. The noise consists of three components. The first component is by minority-carrier traveling in a substrate, the second is substrate potential fluctuation, and the third is through power supply lines. Figure 1 shows a cross-sectional view of the boundary region of DRAM and gate array. Memory cells are embedded in a p-well to be protected from minority-carrier noise component. the substrate potential fluctuation of the gate array part, especially with twin-well process where deep substrate is resistive and strong substrate potential interaction occurs only near the surface. This 'cut well' protects not only memory cells but also the memory peripheral critical timing circuits. The design of supply voltage is demonstrated in Fig.2. Different power supply pads are assigned for the DRAM macro and the gate array to eliminate the interaction through power supply lines.

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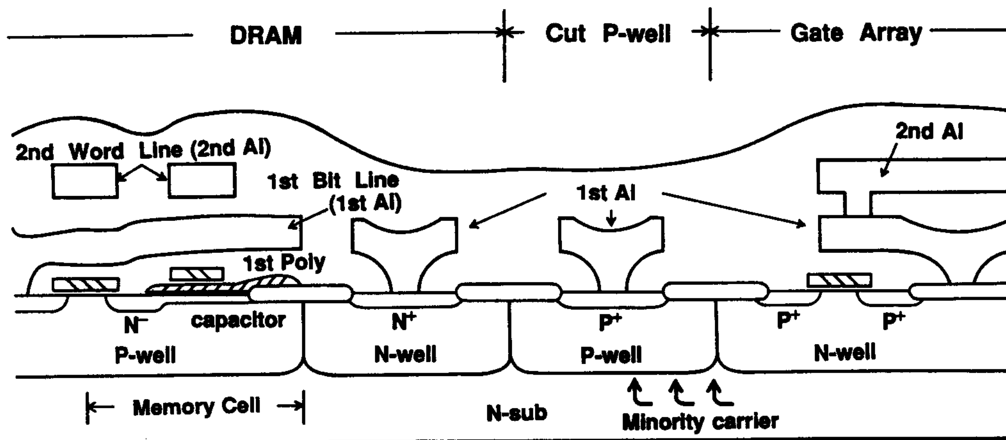

Fig.1. Cross-sectional view of the boundary region between DRAM and Gate Array.

III. Evaluation of Test Device

The micro-photograph of the test chip is shown in Fig.3. Placement and routing of the gate array and connections to the embedded DRAM are done fully automatically by a CAD system. Logic and delay simulations are also supported in the CAD environments. Gate array in this test device includes AC performance evaluation circuits, simultaneous switching circuits for noise generation and a Built-In Self Test(BIST) circuit. The circuit size is about 10K gates.

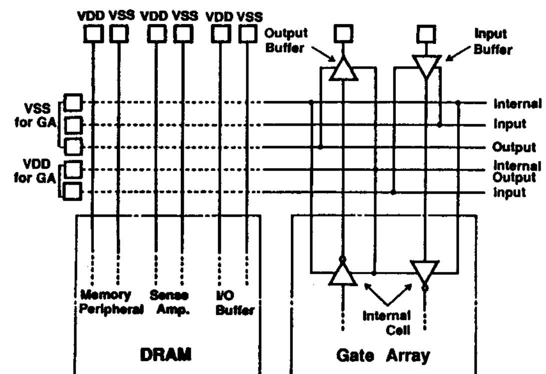

Fig.2. Design of supply voltage.

III-1 Performance and features

The performance and features of the chip are listed in Table I. Chip size is 14.95mm x 14.95mm. Figure 4 shows the measured propagation delay time versus fanout with a comparison with 1.5μm technology counterpart. The typical delay time of the gate array is 0.4ns (2-input NAND, F/O=2, Al interconnect=2mm).

The memory organization is 128Kwords x 8bit and the memory cell size is 3.6μm x 8.2μm. Figure 5 compares DRAM memory cells with gate array basic cells (67.2μm x 18μm). A memory cell is one fortieth of a basic cell. The access time of PSRAM/VSRAM mode is 60ns/125ns at worst condition, that is 85°C and 4.5 volts.

III-2 Noise Disturbance Evaluation

Figure 6 is a measured hardness against carrier injection into substrate. The present DRAM with protecting p-well is fully functional even when ±300mA current is injected into the substrate. On the other hand, the conventional DRAM without protecting p-well begins to fail at an order of μA.

Figure 7 shows a diagram of the simultaneous switching circuit which models noise generation in real application. The circuit controls the number of activated gates and output buffers with external 100pF load, and provides various level and various kind of noise. In parallel with read/write operation or self-refresh operation of the DRAM macro, the simultaneous switching circuit is activated at various

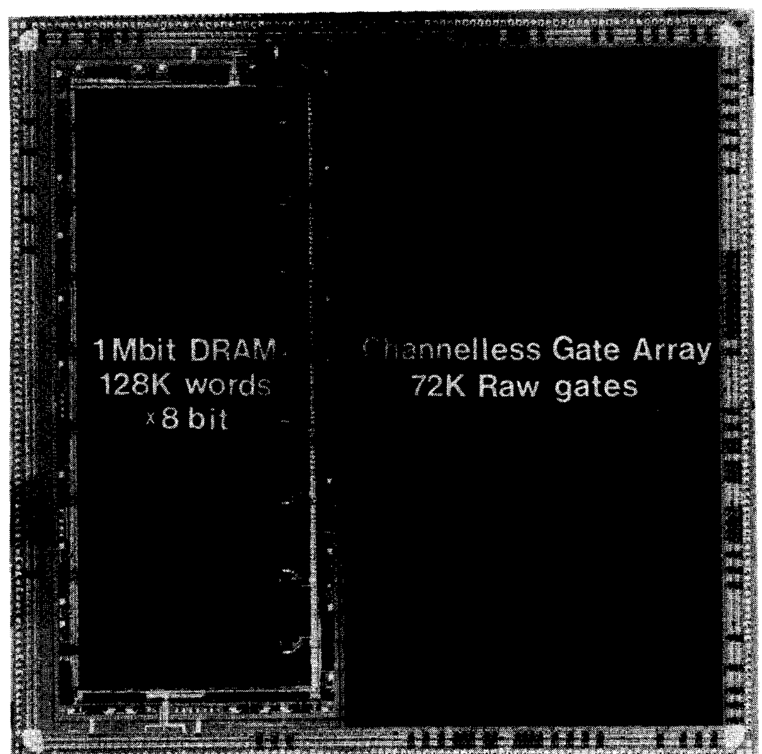

Fig.3. Micro-photograph of the test chip.

frequency. Figure 8 demonstrates the measured results. Even if internal cells of 4.8K gates and 32 output buffers switches simultaneously in both read/write and self-refresh operation, the DRAM can operate without any error. The maximum power consumption is 0.4W about internal cells and 0.8W about output buffers at 10MHz frequency, which represents the severest condition of the gate array part. The hardness of the present DRAM macro against the noise generated in the adjacent gate array can be said satisfactory. The results suggest that a RAM macro based on DRAM cells is a promising approach for a high-density on-chip memory macro[5].

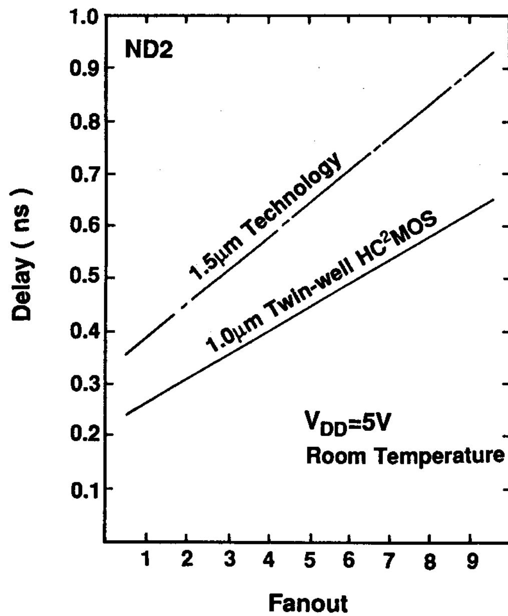

Fig.4. Measured propagation delay time of 2-input NAND.

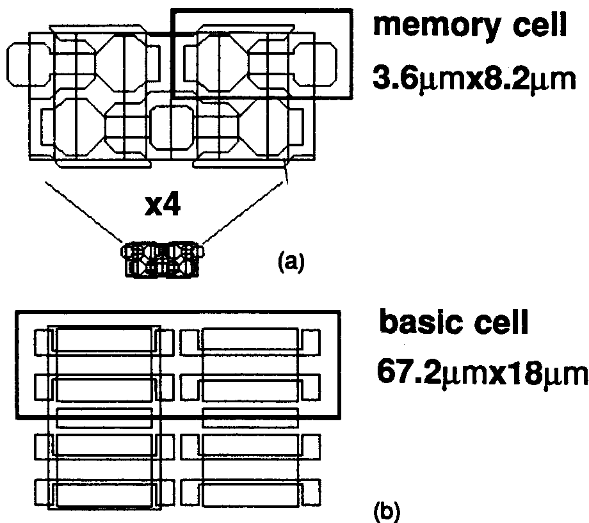

Fig.5. (a) DRAM memory cell. (b) Gate array basic cell.

TABLE I. PERFORMANCE LIST

Chip size	14.95 x 14.95mm^2
Operation voltage	5V ± 10%
Process	1.0μm twin-well HC^{2}MOS
Layers	Double Al & double poly-Si
CHANNELLESS GATE ARRAY	
Propagation delay	0.4ns (2-input NAND, FO=2, Al 2mm)
Density	72K raw gates (usable 30KG)
Interface	TTL/CMOS compatible
Pins	256 I/O pads
EMBEDDED MEMORY	
Organization	128K words x 8bit
Cell size	3.6 x 8.2μm^2
Capacitor	planar (t_{ox}=10nm)
PSRAM access time	60ns (worst)
VSRAM access time	125ns (worst)
Operating current	40mA (t_{cycle}=100ns)
Self-refresh current	20μA (0 ~ 85°C)
Laser fuse redundancy	4 columns & 4 rows
Battery backup voltage	3V

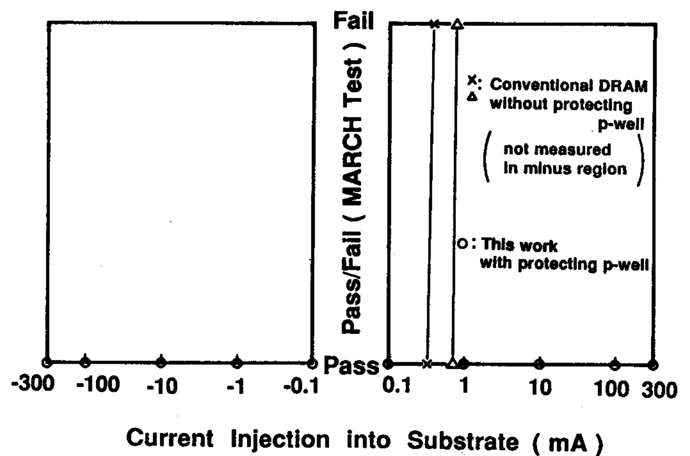

Fig.6. Injection hardness of the embedded DRAM.

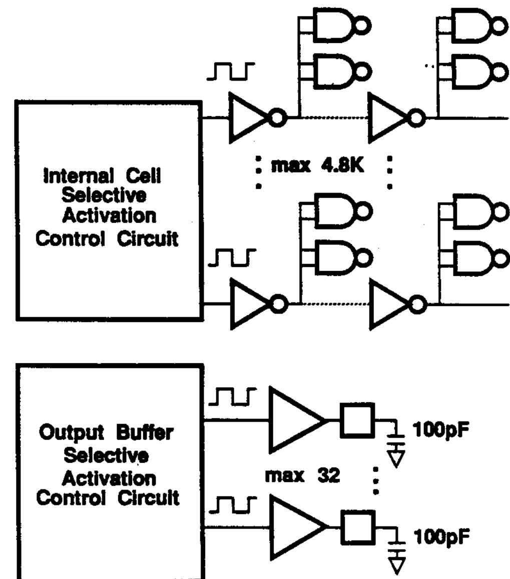

Fig.7. Diagram of the simultaneous switching circuit.

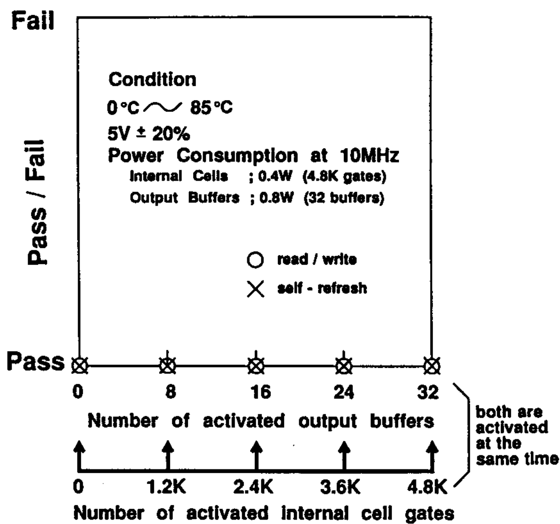

Fig.8. Measured results of noise disturbance using the simultaneous switching circuit.

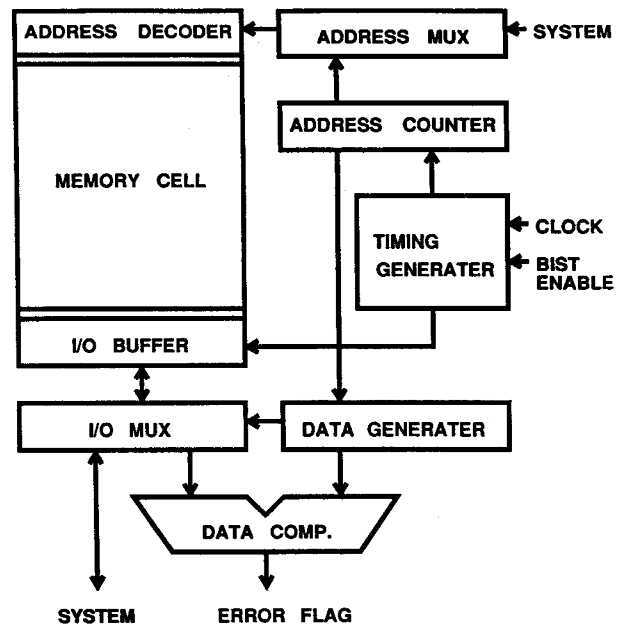

Fig.9. Diagram of Built In Self Test (BIST).

IV. Testing Method

As for testing, the device supports two modes. The first testing mode is a transparent test mode, where the pins of the RAM can be directly accessed from outside and the RAM can be tested as a standard PSRAM/VSRAM. In case of a memory macro with laser fuse redundancy, this transparent mode is indispensable.

The second test mode is a Built-In Self Test (BIST) mode. Block diagram for BIST is shown in Fig.9. Basic idea is as follows. According to the CHECKER BOARD pattern, a data generator, an address counter and a timing generator write a certain data stream into the RAM. Data comparator compares the read-out data with the expected data generated by data generator and generates the error flag when mismatch is detected. The BIST circuit is built with a standard gate array and registered as a soft macro which is about 0.5K gates. In a transparent test mode, it is difficult to measure internal access time precisely because pins are loaded with external capacitances. The BIST approach is useful when internal access time is of interest. As a frequency of BIST clock becomes higher, read error occurs and error flag is set. Internal access time can be calculated from the highest fully functional frequency.

V. Conclusion

A 72K CMOS channelless gate array with embedded 1Mbit Dynamic RAM is successfully developed using 1.0μm HC^{2}MOS twin well process technology. The DRAM design is optimized for embedding. For example, double Al process, no substrate bias, protecting p-well, cut well, and PSRAM/VSRAM mode are adopted. Test device demonstrates that the DRAM macro has sufficient hardness and stability against noise disturbance from gate array part. A DRAM macro approach, in which more than 1Mbit RAM can be realized, is shown to be promising for the future RAM macro.

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