CMOS INVERTER DELAY AND OTHER FORMULAS USING a-POWER LAW MOS MODEL

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CMOS Inverter Delay and Other Formulas Using α-Power Law MOS Model

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Abstract

Simple yet realistic MOS model, namely α-power law MOS model, is introduced to include carrier velocity saturation effect which becomes eminent in short-channel MOSFETs. The model is an extension of Shockley's square law MOS model in the saturation region. Using the model, closed-form expressions are derived for delay, short-circuit power, and transition voltage of CMOS inverters. The resultant delay expression includes input waveform slope effects and parasitic drain/source resistance effects and can be used in simulation and/or optimization CAD tools. It is concluded that the CMOS inverter delay becomes less sensitive to the input waveform slope and short-circuit dissipation increases as MOSFETs becomes small.

Introduction

An expression for CMOS inverter delay was first introduced by J.R.Burns[1]. However, the MOSFET model used in the theory was Shockley's simple formula which can not reproduce voltage-current characteristics of the recent short-channel MOSFETs. Moreover, Burns's expression does not include input waveform slope effect and source/drain resistance effect. The source/drain resistance effect is important in estimating delay degradation by parasitic diffusion resistance of MOSFETs and hot-carrier degradation effect in circuit level[2,3]. Hedenstierna and Jeppson take into account the input waveform slope effect on inverter delay[4], but the theory is also based on Shockley model.

In considering these points, a new MOS model is introduced. Although the model is simple and can be treated analytically, it reproduces the short-channel MOSFET characteristics better than Shockley model. Using the model, closed-form expressions are derived for delay, short-circuit power, and transition voltage of CMOS inverters.

Simple Short-Channel MOSFET Model

Figure 1 shows a comparison between Shockley model and measured MOSFET V_{DS}–I_D characteristics for 1μm NMOS transistor. It is clear that Shockley model fails to reproduce the I-V characteristics of the recent MOSFET. The biggest discrepancy comes from neglect of velocity saturation effect of carriers[5]. Figure 2 shows V_{GS}–I_D characteristics in the saturation region. As seen from Fig.2, drain current I_D is proportional to $(V_{GS}-V_{TH})^{\alpha}$. Shockley model claims that $\alpha=2$, whereas the measured value of α for around 1 μm rule is 1.2 for N-channel MOSFET and 1.5 for P-channel MOSFET because of the velocity saturation by gate-source voltage V_{GS}.

Taking the above discussion into account, α-power law model as seen in Fig.3 is proposed. The model is based on four parameters, V_{TH} (threshold voltage), I_{D0} (drain current at $V_{GS}=V_{DS}=V_{DD}$), V_{D0} (drain saturation voltage at $V_{GS}=V_{DD}$), and α (velocity saturation parameter). All these parameters are easily obtained from measured data, and especially I_{D0} is a good index of the drivability of MOSFETs and frequently used by VLSI designers. The model equations are given below.

$$I_D = \begin{cases} 0 & (V_{GS} \le V_{TH} \quad : \text{cut-off region}) \\ (I_{D0}'/V_{D0}')V_{DS} & (V_{DS} < V_{D0}' \quad : \text{triode region}) \\ I_{D0}' & (V_{DS} \ge V_{D0}' \quad : \text{pentode region}) \end{cases} \quad \text{Eqs.1}$$

,where

$$I_{D0}' = I_{D0}\left[\frac{V_{GS}-V_{TH}}{V_{DD}-V_{TH}}\right]^{\alpha}, \quad V_{D0}' = V_{D0}\left[\frac{V_{GS}-V_{TH}}{V_{DD}-V_{TH}}\right]^{\alpha/2} \quad \text{Eqs.2}$$

Input Waveform Slope and Delay

By using the α-power law model, an expression for the delay is derived. First consider the case of discharging the output capacitance with NMOS as shown in Fig.4, where the input voltage is varied linearly in transient time of t_T. In this case, the effect of PMOS can be neglected as is pointed out by Ref.[4]. Figure 5 shows a comparison of the delay calculated using SPICE MOS level 3 model[6], the α-power law model and the Shockley model. Better agreement is shown between SPICE and the proposed model. After the conventional manipulation of differential equations, the delay, t_{pHL} and t_{pLH} can be expressed as follows.

$$t_{pHL},\ t_{pLH} = \left[\frac{V_{TH}/V_{DD}+\alpha}{1+\alpha} - \frac{1}{2}\right] t_T + \frac{C_L V_{DD}}{2I_{D0}} \quad \text{Eq.3}$$

In the above expression, the first term is the input dependent term which is linearly dependent on the input slope t_T, and the second term is the output capacitance dependent term. This expression is independent of the triode region model of Eqs.1 and 2, when V_{D0} is near or less than half V_{DD}, which is typical. A comparison is made in Fig.6 between SPICE simulation and calculation with the above formula.

It is interesting to note that the delay becomes less sensitive to the input slope when MOSFET becomes miniaturized and α becomes smaller, because the factor $(V_{TH}/V_{DD}+\alpha)/(1+\alpha) - 1/2$ decreases monotonously as α decreases. This is assured by Fig.6, where α for NMOS (t_{pHL}) is 1.2 and α for PMOS (t_{pLH}) is 1.5.

Next step is to approximate the real input waveform by a rumped waveform to obtain effective t_T. As seen from Fig.7, good approximation is achieved by connecting $0.1V_{DD}$ point and

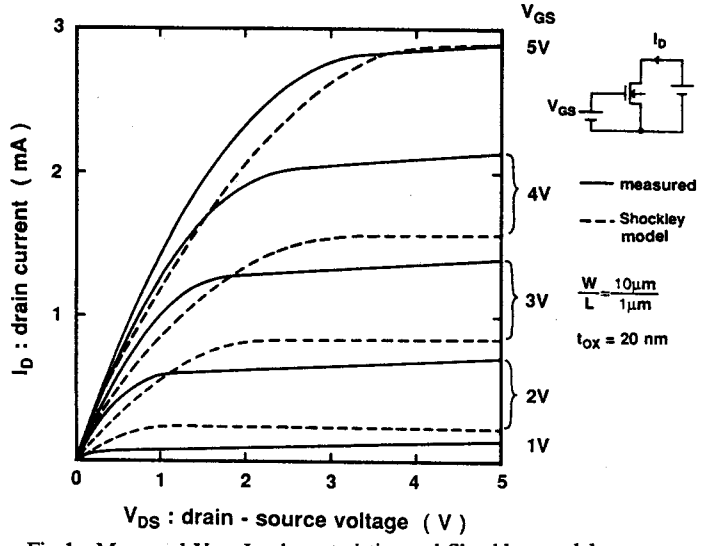

Fig.1. Measured V_{DS}–I_D characteristics and Shockley model.

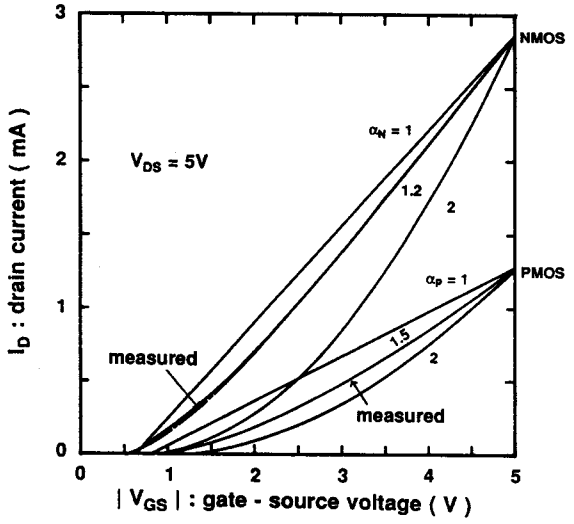

Fig.2 V_{GS}–I_D characteristics

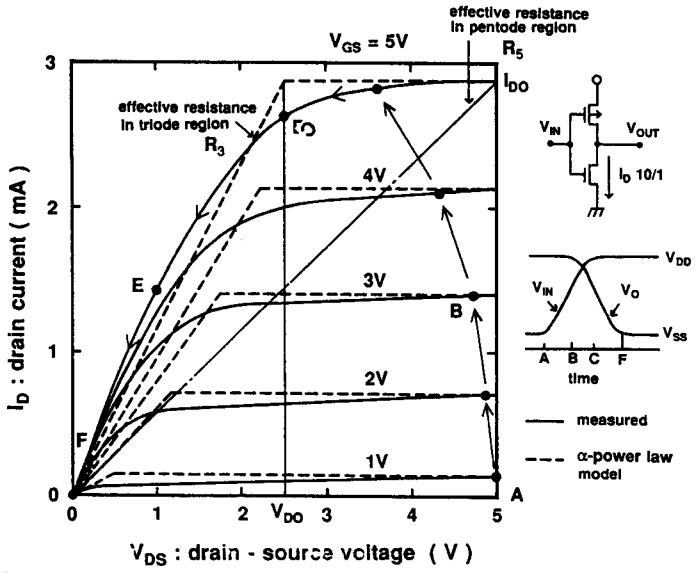

Fig.3 Proposed α-power law MOS model

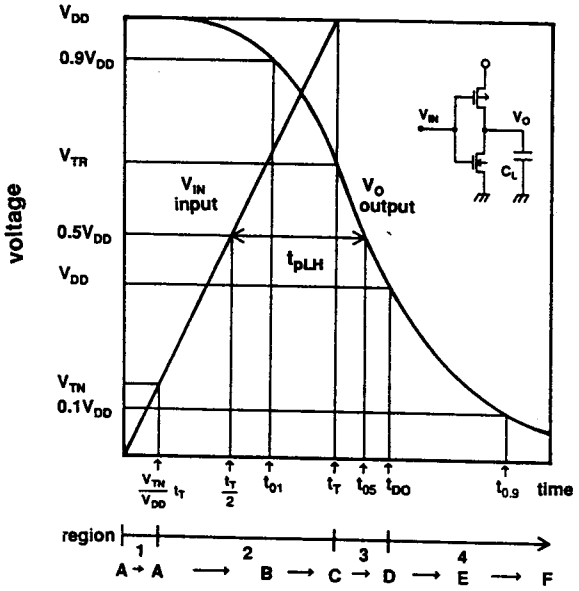

Fig.4 Discharging waveform and notation

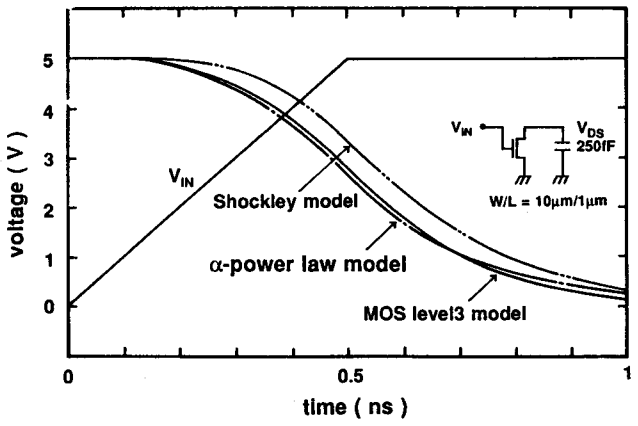

Fig.5 Comparison of discharging waveforms

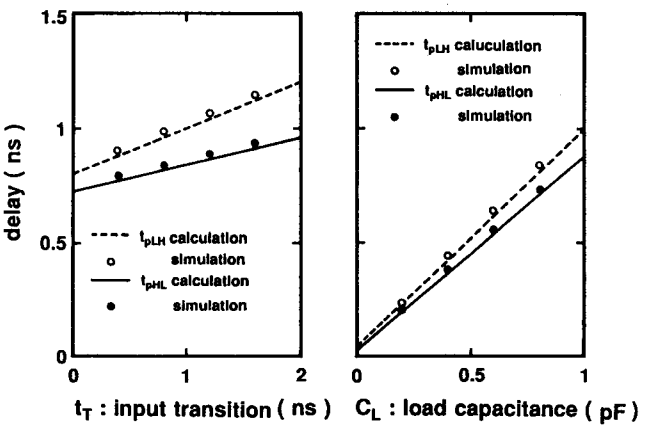

Fig.6 Calculated and simulated value for t_{pLH} and t_{pHL}

$0.9V_{DD}$ point, when the input slope is similar to the output slope, which is often met in real VLSIs. Using this approximation, the delay estimation is carried out for the circuit of Fig.8(a), together with the result in Fig.8(b). Using the same assumption, t_T is expressed as follow, and the normalized delay calculated by this formula is plotted in Fig.9.

$$t_T = \frac{t_{0.9} - t_{0.1}}{0.8} = \frac{C_L V_{DD}}{I_{D0}} \left[\frac{0.9}{0.8} + \frac{V_{D0}}{0.8 V_{DD}} \ln \frac{10 V_{D0}}{e V_{DD}} \right] \quad \text{Eq.4}$$

If it is assumed that V_{D0}/V_{DD}=0.5 and α=1.5, which is typical, the delay of Eq.3 is simplified as $0.75C_L R_S$ using Eq.4, where R_S ($\equiv V_{DD}/I_{D0}$) is an effective pentode resistance of MOSFET as shown in Fig.3.

Figure 10 shows the delay variation with V_{DD}, using the α-power law MOS model. It is seen that the delay dependence on V_{DD} gets milder when the velocity saturation gets worse, that is, α tends to 1.

Effect of Source and Drain Resistance on Delay

Figure 11 is static characteristics of MOSFETs with drain resistance R_D or source resistance R_S. In order to include the source/drain resistance effect, only the following substitutions are to be made. Then, the above discussions and expressions are all valid. These substitutions are easily derived from Eqs.1 and 2.

$$I_{D0} \rightarrow I_{D0} / \left[1 + \frac{\alpha}{1 - V_{TH}/V_{DD}} \cdot \frac{R_S}{R_S} \right],$$

$$\frac{V_{D0}}{V_{DD}} \rightarrow \frac{V_{D0}}{V_{DD}} + \frac{R_D}{R_S} + \frac{R_S}{R_S} \quad \text{Eqs.5}$$

Figure 12 shows a comparison between the calculation by the formula and SPICE simulation. The inverter delay with the resistance inserted turns out to be approximated as follows for around 1μm MOSFETs.

$$\frac{\Delta t_{pHL}}{t_{pHL}}, \frac{\Delta t_{pLH}}{t_{pLH}} \approx \frac{R_S}{R_S} + \frac{1}{3}\frac{R_D}{R_S} \approx \frac{1}{2}\frac{R_S}{R_3} + \frac{1}{6}\frac{R_D}{R_3} \quad \text{Eq.6}$$

,where R_3 ($\equiv V_{D0}/I_{D0}$) denotes an effective triode resistance of MOSFET. If the resistance is inserted only in series with the NMOS and not with PMOS, then the inverter-chain delay degradation is about a half of the above formula.

Short-Circuit Power in Static CMOS Circuit

There is a direct current path in a CMOS inverter when both of the NMOS and PMOS are on. The expression of the power consumed in this mode is first given by Veendrick[7], based on Shockley model. By replacing the MOS model from Shockley model to the α-power law model, the short-circuit power consumed per one switching, P_S, is expressed as follows.

$$P_S = 2 \cdot V_{DD} \cdot 2 \int_0^{t_T/2} I_D(V_{GS} = V_{DD}\, t / t_T)\, dt$$

$$= V_{DD}\, t_T\, I_{D0} \frac{1}{\alpha + 1} \frac{1}{2^{\alpha-1}} \frac{(1 - 2\, V_{TH}/V_{DD})^{\alpha+1}}{(1 - V_{TH}/V_{DD})^{\alpha}} \quad \text{Eq.7}$$

If α is set to 2 as in Shockley model, this formula is reduced to Veendrick's formula. The result is not dependent on the triode model. The plot of the formula is given in Fig.13. It is seen that the short-circuit dissipation component increases as MOSFETs become smaller and the velocity saturation index α decreases to unity.

Transition Voltage

The logic transition voltage, or inverting voltage[8] of a CMOS inverter can also be calculated by the α-power law model. Equating drain current of PMOS and NMOS in the pentode region, the following formula is derived for the transition voltage, Vinv, with an assumption that the threshold voltage of PMOS and NMOS is equal to V_{TH} and the PMOS and NMOS have the same α.

$$\frac{V_{inv}}{V_{DD}} = \frac{(I_{D0,N} / I_{D0,P})^{1/\alpha} (V_{TH} / V_{DD}) + (1 - V_{TH} / V_{DD})}{(I_{D0,N} / I_{D0,P})^{1/\alpha} + 1} \quad \text{Eq.8}$$

,where $I_{D0,P}$ and $I_{D0,N}$ stand for I_{D0} of PMOS and NMOS, respectively. The result is graphically shown in Fig.14, indicating that Shockley model, where α is set to 2, is not a good approximation in estimating the transition voltage. It is seen that as α becomes small, the transition voltage becomes more sensitive to the gate width ratio of PMOS and NMOS, that is, $I_{D0,P} / I_{D0,N}$. This result is not dependent on the triode model.

Summary

Useful delay, power and transition voltage expressions are derived with a new MOSFET model, which can be used for CAD tools. It is shown that as MOSFETs get miniaturized, the CMOS inverter delay becomes less sensitive to the input waveform slope, and to the V_{DD} variation. In addition, short-circuit dissipation increases, and transition voltage becomes more sensitive to the gate width ratio of PMOS and NMOS.

Further extension is preferable for triode region characteristics modeling to increase precision, although the results obtained here remain essentially unchanged. It is because all formulas except Eqs.4 and 5 do not depend on the triode model. Since the proposed model efficiently models the short-channel MOSFET, it can be used to modify the classical expressions based on Shockley model. One interesting application is on a CMOS arbiter optimization[5].

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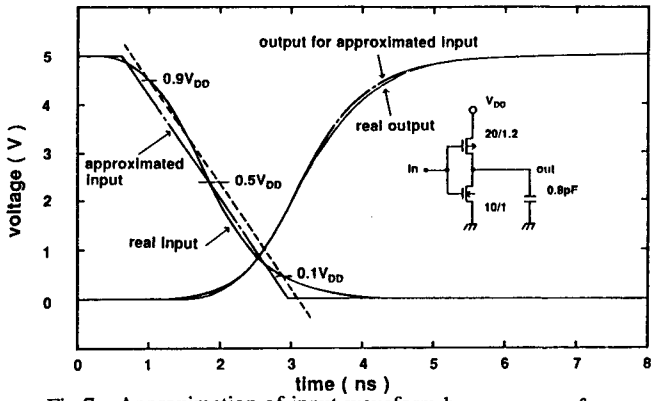

Fig.7 Approximation of input waveform by rump waveform

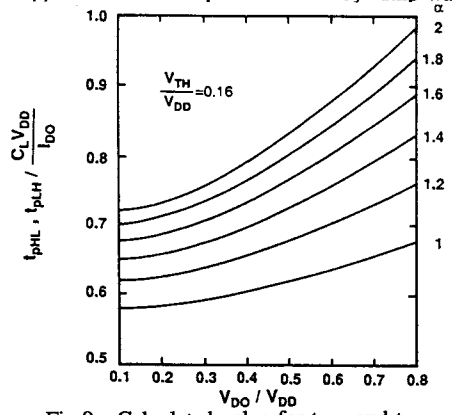

Fig.9 Calculated value for t_{pLH} and t_{pHL}

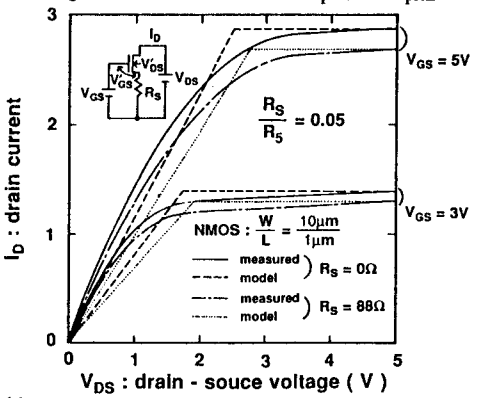

Fig.11 MOS static characteristics with source resistance

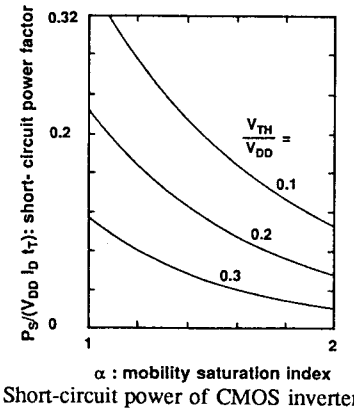

Fig.13 Short-circuit power of CMOS inverter per switching

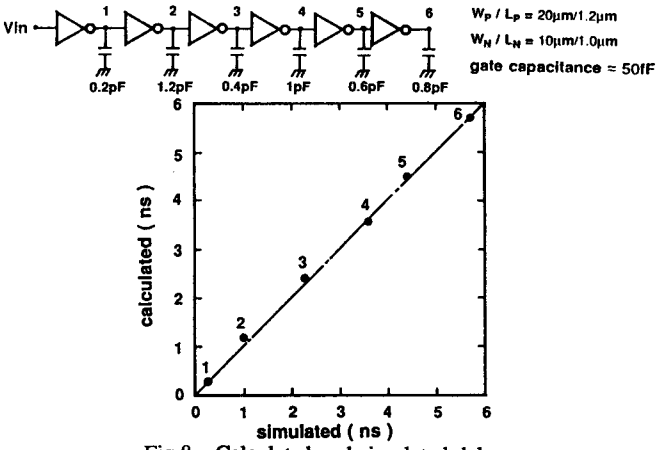

Fig.8 Calculated and simulated delay

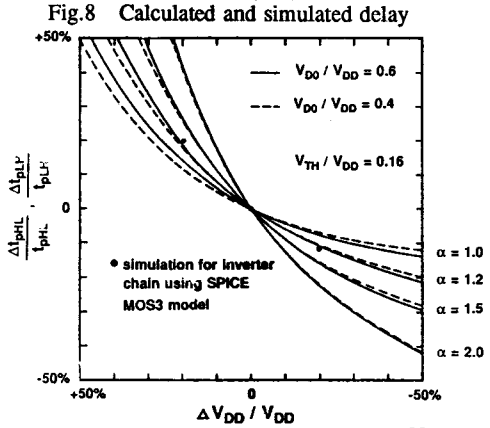

Fig.10 Calculated delay dependence on V_{DD}

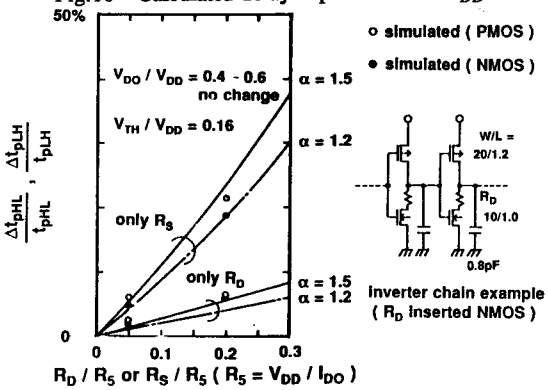

Fig.12 Calculated and simulated delay with source/drain resistance

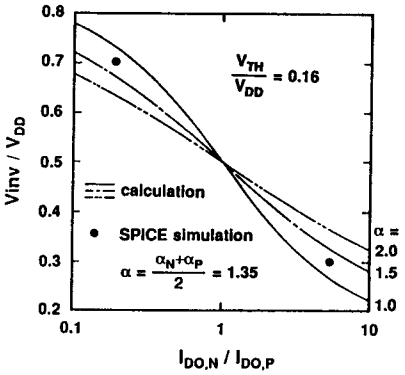

Fig.14 Transition voltage of CMOS inverter