TPM 9.1: 0.5μm 2M-Transistor BipnMOS Channelless Gate Array

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This channelless gate array uses 0.5μm BiCMOS technology integrating more than 2 million transistors on a 14x14.4mm chip. The BipnMOS cell is used to achieve 230ps logic gates with large margins. High-speed and high-density BiCMOS macro cells including RAM, ROM and CAM are also included.

To ensure high reliability of the 0.5μm gate-length MOSFETs and to reduce power dissipation, a power supply voltage of 3.3V is adopted. BinMOS and complementary-BiCMOS gates are used to maintain a speed advantage over CMOS even at low supply voltage.[1,2]

The C-BiCMOS gate requires a pnp transistor with a high transition frequency in addition to an npn transistor and hence suffers from both increased process cost and increased cell area. On the other hand, BinMOS gates can be realized with only an npn transistor. However, the output does not reach VDD but only VDD-VBE, increasing delay time and leakage current of the following gates and hence decreasing margins.

A BipnMOS gate overcomes the above-mentioned difficulties. Figure 1a shows a 2-input NAND BipnMOS gate. A small pMOS transistor is added to the conventional BinMOS gate connecting the output node to the drain of the pMOS transistor when charging the load. The added pMOS transistor enables full output swing. The pMOS gate is controlled by a small inverter which provides an inverted output signal. Figure 1b shows a comparison of the output waveforms of the BipnMOS gate and a BinMOS gate with a resistor between output and drain of the pMOS (BiRnMOS) device. The resistor ensures full swing of the output, but the resistance cannot be too small because it bypasses the base current and hence degrades speed. As seen from the figure, BipnMOS offers high-speed operation without any leakage current of the next logic stage.

Figure 2 shows the layout of a BipnMOS basic cell. Small MOSFETs in the basic cell can also be used in flip-flops, RAM, ROM macros, and other cells. Figure 2 also shows a layout pattern of a D flip-flop cell.

Figure 3 shows a micrograph of an evaluation chip containing ring oscillators and macro cells. A BipnMOS 2-input NAND gate has 230ps propagation delay with fanout of 7 as shown in Figure 4a. The speed advantage over CMOS gates is observed down to 2.5V as shown in Figure 4b. High-density high-speed RAM and ROM macros are necessary in implementing a high performance system on a chip. Recent gate arrays tend to include small MOS transistors in a basic cell to implement a high-density 6-transistor CMOS RAM cell efficiently.[3] In this BipnMOS gate array, the small MOS transistors used in the gate can be used for 6-transistor RAM cells. The bipolar transistors are used in word-line drivers and sense amplifiers.

There are two RAM macros. One is a high-speed memory that occupies one basic cell and the other is a high-density version that occupies half of the basic cell. Figure 5a shows a circuit diagram of the fast RAM macro which has separate write and read ports and can be used as a two-port RAM cell with simultaneous write and read. Write is through the DATA line connected to nMOS N3, which must be larger than N1 for stability.

High-speed operation in the read mode is achieved by: (1) double bit lines with bipolar middle buffers, (2) 0.6V bit-line swing, (3) BiCMOS sense amplifiers with emitter dotted shared transistors.[4] Read out from a memory cell is carried out through pMOS transistor P3 connected to the BIT line. A small transistor is used for P3 in order to limit the swing of the local bit line. The local bit-line level is determined by pMOSFETs P2, P3 and P4, with the low level set at +1.3V and the high level set at +1.9V. This 0.6V swing is transferred to a main bit line through a bipolar middle buffer Q1. Eight memory cells are connected to the local bit line. The bipolar middle buffer drives the highly-capacitive main bit line.

The bipolar middle buffer Q1 is also used as a component of a differential sense amplifier using emitter dotting. The other side of the amplifier consists of bipolar transistor Q2 whose base is controlled by a self-tracking reference voltage generator. The reference generator uses MOSFETs which are the same as a memory cell and 1.5 times wider than the local bit-line load and therefore track process, voltage and temperature variations.

Figure 5b shows simulated delay distributions of the BiCMOS RAM and a pure CMOS RAM macro. Delay from the READ signal to the read word line RWL is reduced to 1.3ns from 1.7ns by using BiCMOS drivers. More drastic delay reduction is observed in the delay from the bit line to the output of the sense amplifier. Typical access time is 2.7ns.

In some applications, density is more important than speed. For these applications, the high-density RAM macro implements two memory cells in one basic cell. Figure 6 shows the circuit diagram of this memory cell. In the read mode only a pMOS transfer gate turns on. In the write mode both pMOS and nMOS transfer gates turn on to ensure cell stability and stable write. The sensing scheme is the same as for the high-speed RAM macro.

For the ROM macro eight memory cells can be realized in one basic cell. The same sensing scheme is used as for the RAM. A CAM macro is realized employing two basic cells per bit. The features of the chip are shown in Table 1, together with the key process parameters of the 0.5μm poly-Si emitter BiCMOS technology with cut-off frequency of 13GHz.

Acknowledgments:

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References

[1]Gamal, A. E. et al., "BiNMOS:A Basic Cell for BiCMOS Sea-of-Gates". CICC'89, pp. 8.3.1-8.3.4, May 1989.

[2]Shin, H. J. et al., "Full-Swing Complementary BiCMOS Logic Circuits," BCTM'89, pp. 229-232, 1989.

[3]Veendrick, H. et al., "An Efficient and Flexible Architecture for High-Density Gate Array", ISSCC DIGEST OF TECHNICAL PAPERS, pp. 86-87, Feb. 1990.

[4]Sakurai, H. et al., "Double Word Line and Bit Line Structurefor VLSI RAMs," Proc. 15th Conf. on Solid State Devices & Materials, Tokyo, pp. 269-272, (A-7-6), 1983.

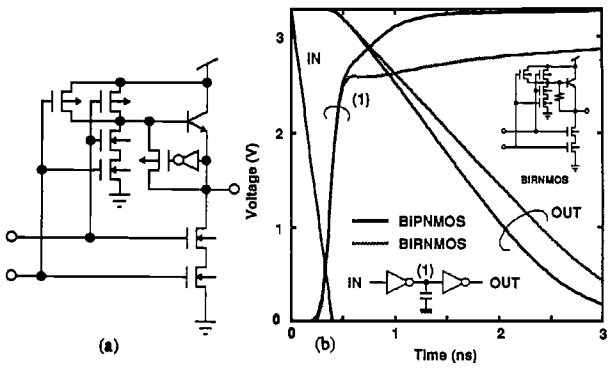

Figure 1: (a) BipnMOS gate (b) Output waveforms of BipnMOS and BinMOS gate

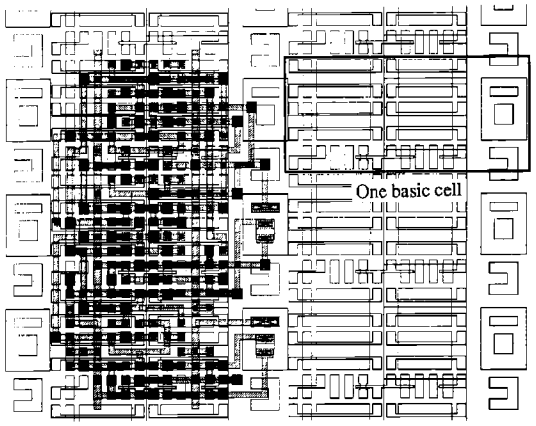

Figure 2: Flip-flop cell layout pattern

FIGURE 3 – *See page 307*

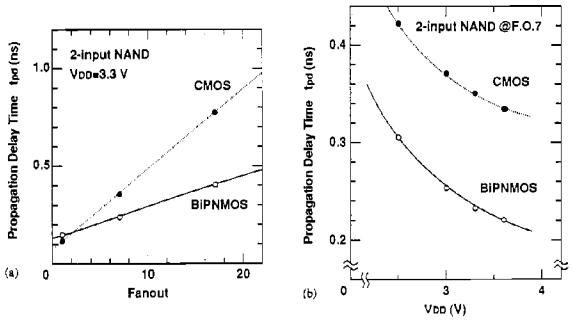

Figure 4: (a) Propagation delay vs. fanout
(b) Supply voltage dependence of delay time

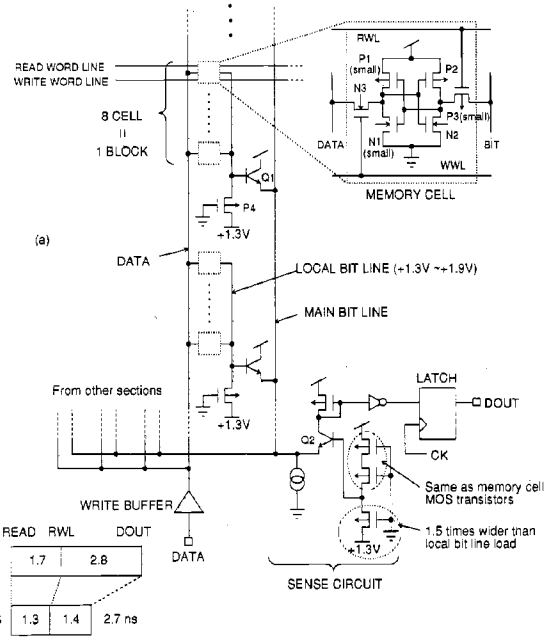

Figure 5: (a) Circuit diagram of fast RAM macro
(b) Simulated access time of BiCMOS RAM macro compared to CMOS

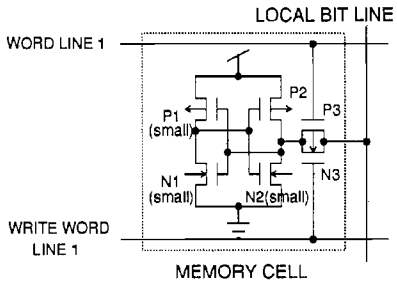

Figure 6: Circuit diagram of high-density RAM cell

Chip size	14x14.4mm
Raw gate count	237,120
I/O cell count	1044
Basic cell area	54.4x25.6μm
Supply voltage	3.3V
Gate delay	230ps (typ., BipnMOS 2NAND, FO=7)
Process	1 poly 3 metal 0.5μm BiCMOS
Bipolar	Poly-Si emitter, f_T=13GHz
	Emitter size = 0.8x2.8μm
MOS	pMOS 12.1/0.6μm
	nMOS 12.1/0.5μm
High-speed RAM	1 memory cell/basic cell
	Tacc=2.7ns (typ. at 512x32b)
High-density RAM	2 memory cells/basic cell
	Tacc=4.0ns (typ. at 256x32b)
ROM	8 memory cells/basic cell
	Tacc= 3.2ns (typ. at 256x32b)

TABLE 1: 0.5μm BipnMOS gate array features

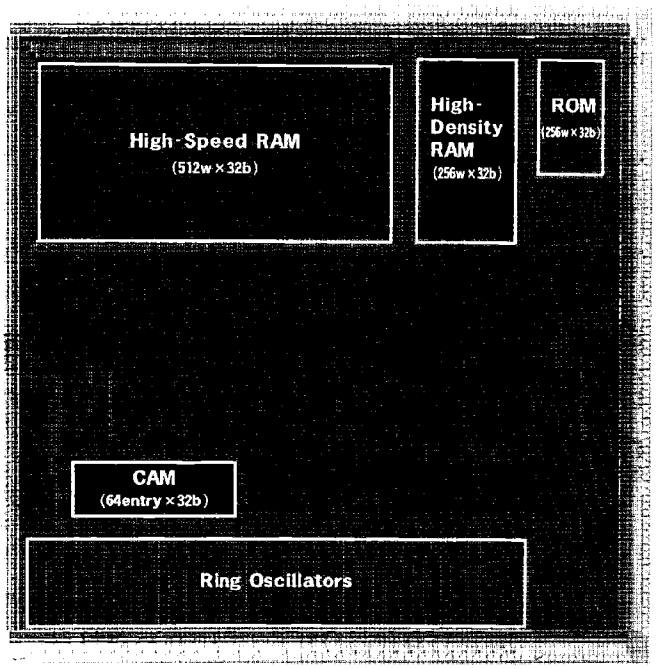

Figure 3: Micrograph of evaluation chip

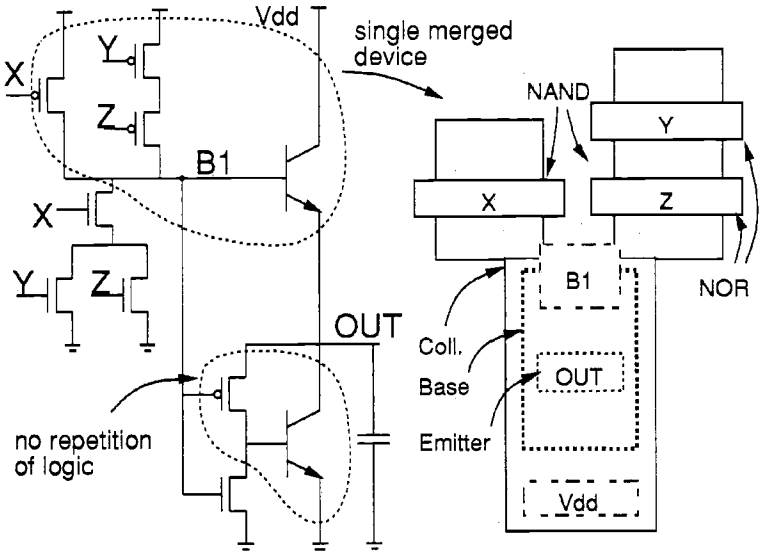

Figure 2: Compact implementation of NAND/NOR functions with MBiCMOS gates