J-SC/26/11//02947

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Reprinted from
IEEE JOURNAL OF SOLID-STATE CIRCUITS
Vol. 26, No. 11, November 1991

0.5-μm 2M-Transistor BiPNMOS Channelless Gate Array

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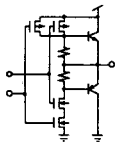
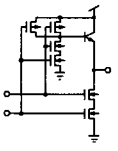
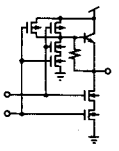
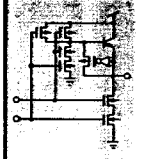
Abstract—**A channelless gate array has been realized using 0.5-μm BiCMOS technology integrating more than 2-million transistors on a 14×14.4-mm^2 chip. A small-size PMOS transistor and a small-size inverter are added to the conventional BiNMOS gate to form the BiPNMOS gate. The gate is suitable for 3.3-V supply and achieves 230-ps gate delay for a two-input NAND with full-swing output. Added small-size MOS transistors in the BiPNMOS basic cell can also be used for memory macros effectively. A test chip with four memory macros—a high-speed RAM, a high-density RAM, a ROM, and a CAM macro—was fabricated. The high-speed memory macros utilize bipolar transistors in bipolar middle buffers and in sense amplifiers. The high-speed RAM macro achieves an access time of 2.7 ns at 16-kb capacity. On the other hand, the high-density RAM macro is rather slow but the memory cell occupies only a half of the BiPNMOS basic cell using a proposed single-port memory cell.**

TABLE I
BiCMOS GATE SUITABLE FOR 3.3 V

	CBiCMOS	BiNMOS	BiRNMOS	BiPNMOS
Circuit				
Process	−	++	+	++
Speed	+	+	+	++
Full-swing	+	−	+	++

I. INTRODUCTION

IN ORDER TO ensure high reliability of 0.5-μm gate-length MOSFET's, a power supply voltage of 3.3 V is adopted. Reducing the supply voltage is also necessary for decreasing the power dissipation of highly integrated system LSI's. The low supply voltage, however, makes the conventional totem-pole BiCMOS gate lose its speed advantage over CMOS. In order to maintain the speed advantage over CMOS even at the low supply voltage, a BiNMOS gate [1] and a complementary-BiCMOS gate [2] have been proposed.

Table I shows candidates for the low-supply-voltage BiCMOS gate. In all these gates, improvement is done on the pull-down circuit of an original BiCMOS gate, since the pull-down part is the cause of the low speed in the original BiCMOS gate at low supply voltage. The C-BiCMOS gate requires a p-n-p transistor with a high cutoff frequency, as well as an n-p-n transistor, and hence suffers from an increase in process cost. On the other hand, the BiNMOS gate can be realized with only an n-p-n transistor, but the output does not reach V_{DD}; instead it stays at the $V_{DD}-V_{BE}$ level, where V_{BE} is a base–emitter turn-on voltage. This increases the delay time and leakage current of the next gate, and hence decreases noise margins. A BiRNMOS gate, which has a resistor inserted between the emitter and base of the pull-up bipolar transistor, achieves a full-swing output. However, if the resistance is set small to realize high-speed pull-up, it bypasses the base current and hence degrades the speed. Here, we propose a BiPNMOS gate which is suitable for a low supply voltage. The BiPNMOS gate achieves high speed, low process cost, and full-swing capability. The BiPNMOS gate can maintain a speed advantage over CMOS at 3.3-V supply voltage.

Another problem concerns memory macros in a BiCMOS gate array. High-speed and high-density memory macros are necessary for building a high-performance system on a chip. However, not many kinds of memory macros have been introduced in a BiCMOS gate array, which prevents the user from making highly value-added VLSI's easily. Besides, recent gate arrays tend to use six-transistor CMOS memory cells for a RAM macro [4], [5] but bipolar transistors arranged in BiCMOS basic cells are not utilized effectively. This inefficiency is solved by new circuit technologies, a double bit-line structure [7] with bipolar middle buffer and a BiCMOS sense amplifier with dotted-emitter structure [6], [8]. As for variety of memory macros, several kinds of memory macros are

Manuscript received April 19, 1991; revised July 22, 1991.

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IEEE Log Number 9102947.

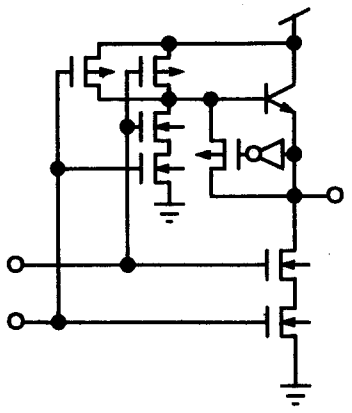


Fig. 1. BiPNMOS gate.

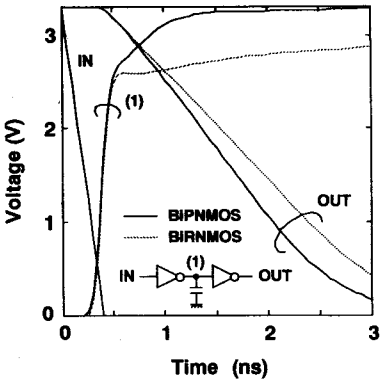


Fig. 2. Output waveforms of BiPNMOS and BiRNMOS gates.

realized including RAM's, a ROM, and a CAM. All these macros use developed BiCMOS circuits.

II. BiPNMOS Gate

Fig. 1 shows a two-input NAND BiPNMOS gate. A small-size PMOS transistor and an inverter are added to the conventional BiNMOS gate. The added PMOS transistor realizes the full swing of the output, while not decreasing the base current of the n-p-n transistor and hence not degrading the speed. When an output terminal is low, the added PMOS is OFF and all current flowing through the PMOS becomes the base current efficiently. When the voltage of the output terminal reaches the threshold voltage of the feedback inverter, the added PMOS turns on and starts pulling up the output to V_{DD}. Even after the bipolar transistor turns off at $V_{DD}-V_{BE}$, the added PMOS keeps ON and realizes a full-swing output. Fig. 2 shows a comparison of the output waveforms of the BiPNMOS gate and the BiRNMOS gate. In this case, the value of the resistor of the BiRNMOS is set to 50 kΩ. As seen from the figure, the full swing of BiRNMOS gate is achieved very slowly. On the other hand, the BiPNMOS gate offers high-speed pull-up to V_{DD}. This reduces the delay and the leakage current of the next gate and increases noise margins.

Fig. 3 shows a layout pattern of a BiPNMOS basic cell. A bipolar transistor and small-size MOS transistors are

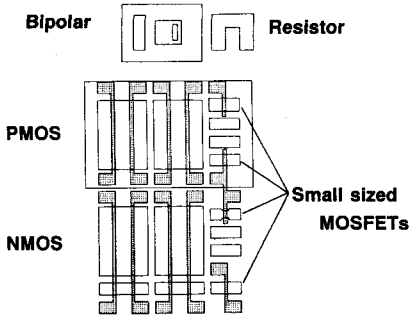


Fig. 3. Basic cell layout of BiPNMOS gate array.

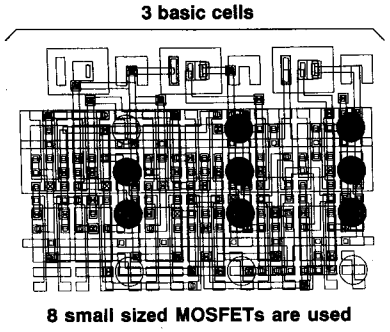


Fig. 4. D-type flip-flop cell layout pattern.

added to the pure CMOS basic cell. These transistors are not only used to construct the basic BiPNMOS gates but also can be used in flip-flops, memory macros, and other cells effectively. Fig. 4 shows an example layout pattern of a D-type flip-flop cell. This D-type flip-flop cell with the BiPNMOS drivers is constructed on three basic cells, and utilizes eight out of 12 small-size MOS transistors.

III. Memory Macros

Recent gate arrays tend to include small MOS transistors in a basic cell to implement a high-density six-transistor CMOS RAM cell. In the present BiPNMOS gate array, small MOS transistors laid out in the BiPNMOS basic cells can be utilized for six-transistor RAM cells. Moreover, the bipolar transistors are utilized for word-line drivers and sense amplifiers efficiently. Four memory macros, namely high-speed RAM, high-density RAM, ROM, and CAM, are designed. A summary of these macros is listed in Table II. One memory cell of the high-speed RAM macro occupies one basic cell. The high-density RAM macro is rather slow but the memory cell occupies half of the basic cell. As for the ROM macro, eight memory cells can be realized in one basic cell and the CAM macro is realized employing one basic cell per bit.

Fig. 5 shows a circuit diagram of the high-speed RAM macro. A RAM cell has a separate write port and a read port and can be used as a two-port RAM cell enabling WRITE and READ operation at the same time. WRITE operation is performed through the DATA line connected to NMOS $N3$, and the dimensions of $N3$ must be selected bigger than $N1$ for stability. High-speed opera-

TABLE II
FEATURES

Chip size	14.0×14.4 mm^2
Internal gate count	237 120 raw gates (CMOS two-input NAND gate)
I/O cell count	1044
Basic cell area	54.4×25.6 μm^2
Supply voltage	3.3 V single
Gate delay	230 ps (typ., BiPNMOS two NAND, fan-out = 7)
Process	1-poly, 3-metal, 0.5-μm BiCMOS process
Bipolar	Poly-Si emitter Emitter size = 0.8×2.8 μm^2
MOS	PMOS = 12.1/0.6 μm NMOS = 12.1/0.5 μm
High-speed RAM	1 memory cell/1 basic cell T_{acc} = 2.7 ns (typ. at 512 word $\times$ 32 b)
High-density RAM	2 memory cells/1 basic cell T_{acc} = 4.0 ns (typ. at 256 word $\times$ 32 b)
ROM	8 memory cells/1 basic cell T_{acc} = 3.2 ns (typ. at 256 word $\times$ 32 b)
CAM	1 memory cell/1 basic cell Data to match = 2.0 ns (typ. at 64 entry $\times$ 32 b)

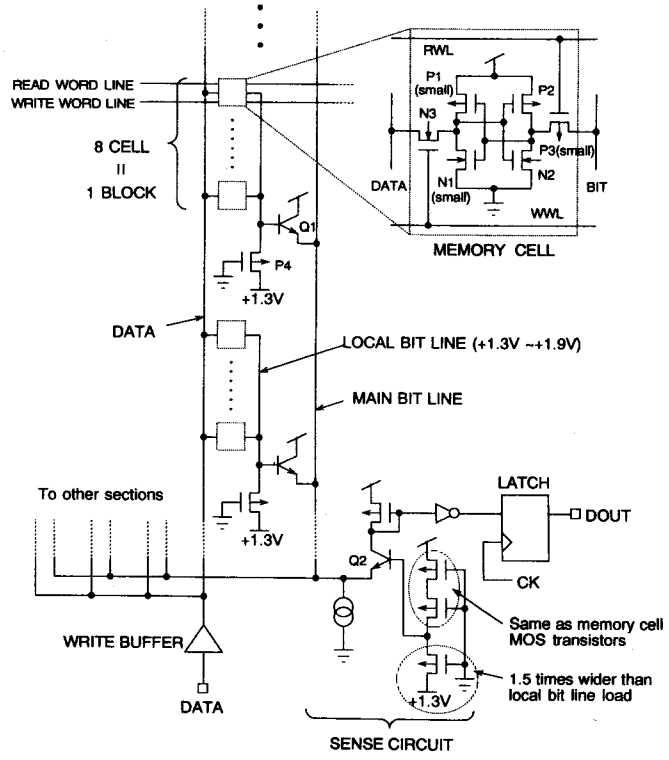


Fig. 5. Circuit diagram of fast RAM macro.

tion in the READ mode is achieved by the following three techniques:

1) double bit lines with bipolar middle buffers,
2) 0.6-V bit-line swing,
3) BiCMOS sense amplifiers with emitter-dotted shared transistors.

Readout operation from a memory cell is carried out through a PMOS ($P3$) connected to the BIT line. A small transistor is used for $P3$ in order to limit the swing of the

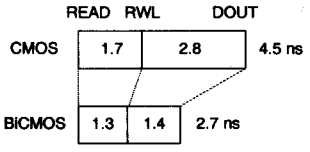


Fig. 6. Simulated access time of BiCMOS RAM macro compared to CMOS RAM.

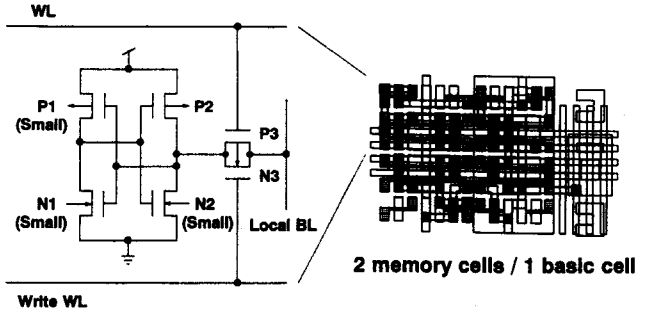


Fig. 7. Circuit diagram and layout pattern of high-density RAM macro.

local bit line. The local bit line is pulled down to the low level of +1.3 V before the readout operation. The local bit-line level is determined by PMOS's $P2$–$P4$ and NMOS $N2$, and only changes to +1.9 V when $P2$ is ON. This 0.6-V swing is transferred to a main bit line through a bipolar middle buffer ($Q1$). The number of memory cells connected to the local bit line is eight (one block). The bipolar middle buffer effectively drives the highly capacitive main bit line. The bipolar middle buffer ($Q1$) is also used as a component of a differential sense amplifier using an emitter dotting technique. The other side of the amplifier is made with the bipolar transistor ($Q2$) whose base is controlled by a self-tracking reference voltage generator. The reference generator uses MOS transistors, which are the same as a memory cell, and 1.5 times wider MOS compared with a local bit-line load to generate a proper reference voltage. The reference generator tracks process, voltage, and temperature variation in a self-tracking way. Fig. 6 shows simulated delay component distributions of the BiCMOS RAM macro and a pure CMOS RAM macro. The delay from READ signal to read word line (RWL) is reduced from 1.7 to 1.3 ns by using BiCMOS drivers. More drastic delay reduction is achieved in the delay from the bit line to the output of the sense amplifier. The current consumption of a sense circuit is 1.3 mA per bit.

In some applications, density is more important than speed. For these applications, a high-density RAM macro, which implements two memory cells in one basic cell, is more suitable. Fig. 7 shows the circuit diagram and the cell layout pattern. The RAM cell realizes high density to adopt a single-port cell and to use the small-size MOS transistors. In READ mode only a PMOS transfer gate turns on to ensure cells stability. In WRITE mode both PMOS and NMOS transfer gates turn on to ensure stable WRITE operation. The sensing scheme is the same as that of the high-speed RAM macro.

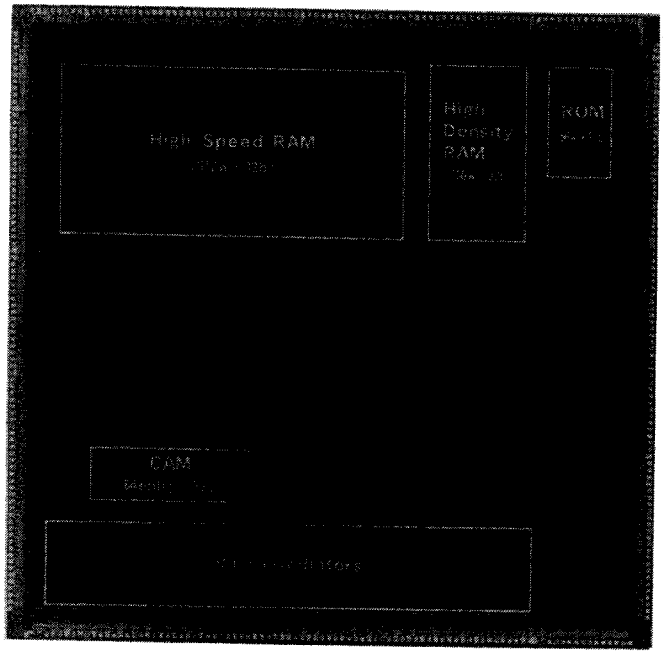
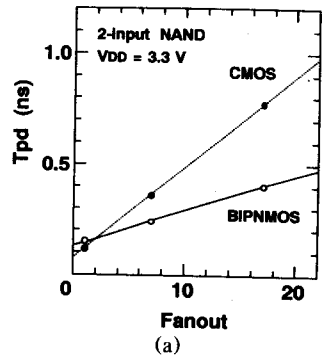


Fig. 8. Microphotograph of evaluation chip.

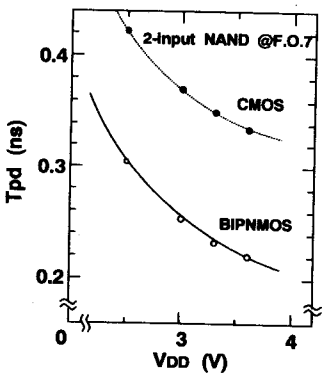
The ROM macro adopts the double bit line and the same sensing scheme as the RAM's. Four PMOS ROM cells and four NMOS ROM cells can be built using one basic cell. The local bit line for the PMOS ROM cell and that for the NMOS ROM cell are separate, because the bit-line levels are different. Content addressable memory (CAM) is another important macro. Small-size MOS transistors are used for the six-transistor memory cells, so a single CAM cell can be constructed with only one basic cell. The CAM macro employs a double match-line architecture and a BiCMOS pull-up circuit to drive the second match line [13]. The key features of the CAM macro are listed in Table II together with a summary of the present chip.

IV. Experimental Result

Fig. 8 shows a microphotograph of the fabricated $14.0 \times 14.4\text{-mm}^2$ chip. The test chip contains ring oscillators to evaluate the speed for the BiPNMOS gate and the CMOS gate, and memory macros. The test chip is fabricated using a 0.5-μm triple-metal BiCMOS process. Although the gate length for the MOSFET's is 0.5 μm, the basic design rule of 0.8 μm is adopted to achieve high speed and high yield at the same time. A poly-Si emitter bipolar transistor with a cutoff frequency of 13 GHz is adopted, and the rapid thermal annealing (RTA) technique is applied to realize a stable poly-single interface. The features of the present chip are shown in Table II, together with the key process parameters of the 0.5-μm BiCMOS technology. Fig. 9(a) shows a speed dependence of the BiPNMOS gate on fan-out. A BiPNMOS two-input NAND gate realizes a propagation delay time of 230 ps with a fan-out of 7 at room temperature. The BiPNMOS gate shows 35% smaller delay than the pure CMOS gate



(a)



(b)

Fig. 9. (a) Propagation delay time versus fan-out. (b) Supply voltage dependence of delay time.

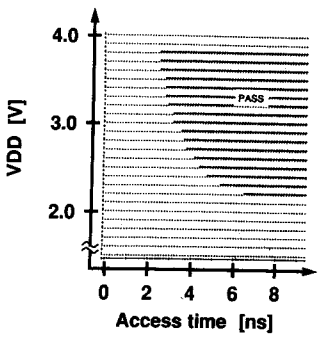


Fig. 10. Schmoo plot of high-speed RAM macro.

even at 3.3 V. Fig. 9(b) shows the speed dependence of the BiPNMOS gate and the pure CMOS gate on V_{DD}. The speed advantage over the CMOS gate is observed down to 2.5 V. Fig. 10 shows a schmoo plot of the high-speed RAM macro and the typical access time of 2.7 ns is seen at 512 word $\times$ 32 b. The speeds of the high-density RAM and ROM macros are 4.0 and 3.2 ns, respectively. These memory macros achieve a high-speed operation using BiCMOS circuit technologies, even in a high-memory-capacity range.

V. Conclusions

A BiPNMOS gate is proposed that assures full-swing and high-speed operation at 3.3 V. The BiPNMOS gate reduces the delay and the leakage current of the next gate and increases noise margins. A two-input NAND gate delay

of 230 ps is observed at a fan-out of 7. Small-size MOS transistors, which are added to construct the BiPNMOS gate, are utilized by flip-flop cells and memory macros effectively.

Four BiCMOS memory macros are presented. A double bit-line structure with bipolar middle buffers and a BiCMOS sense amplifier are introduced for high-speed operation. Small-size MOS transistors and a single-port memory cell are used in a high-density memory macro. The typical access time of the high-speed RAM macro is measured to be 2.7 ns at 16-kb capacity.

Acknowledgment

The authors would like to express their appreciation to Dr. T. Iizuka, K. Maeguchi, and H. Nakatsuka for encouragement throughout the work.

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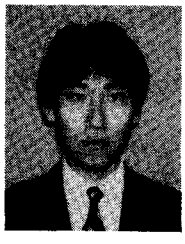

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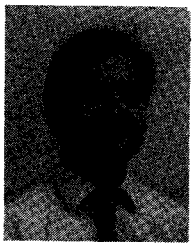
Mr. Hara is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



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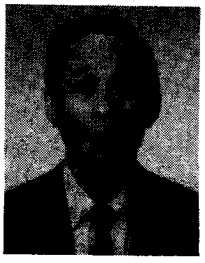

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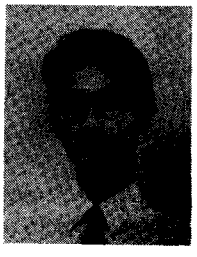
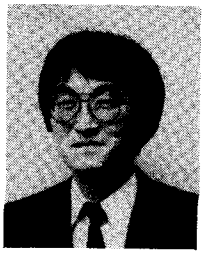


Katsuhiro Seta was born in Tokyo, Japan, on September, **9, 1963. He received** the B.S. and M.S. degrees **in electric** engineering from Science **University of Tokyo**, Japan, in 1987 and 1989, **respectively.**

He joined the Semiconductor Device Engineering **Laboratory**, Toshiba Corporation, **Kawasaki, Japan**, in 1989, where he has been **engaged** in the research and development of **BiCMOS** ASIC and BiCMOS cache **macros.**

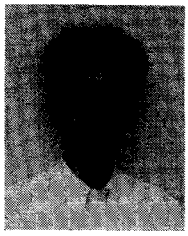
Mr. Seta is a member of the **Institute** of Electronics, Information and Communication Engineers of **Japan.**



Hiroshi Momose (M'91) was born in Matsumoto, Japan, in February 19, 1954. He received the B.S. and M.S. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1977 and 1979, respectively.

In 1979 he joined a newly organized laboratory, the Semiconductor Device Engineering Laboratory (SDEL), Toshiba Corporation, Kawasaki, Japan, where he has been engaged in advanced CMOS/BiCMOS process development, including trench isolation and LDD structure and latch-up analysis. He has also developed EPROM, very-large-scaled CMOS SRAM, and BiCMOS high-speed RAM devices. From 1986 to 1987 he worked for Hewlett-Packard Laboratories, Palo Alto, CA, as a Visiting Engineer, where he studied half-micrometer BiCMOS technology. He is currently responsible for half- and submicrometer BiCMOS device and process technologies for memory and logic VLSI's.

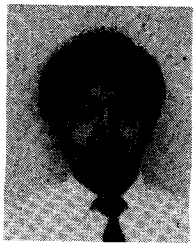
Mr. Momose is a member of the Institute of Electronics and Communication Engineers of Japan.



Youichiro Niitsu was born in Tokyo Japan. He received the B.S. degree in physics in and 1980 and the M.E. degree in applied physics in 1982 from Tohoku University, Sendai, Japan.

He joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan, in 1982. He worked in the area of the high-performance CMOS logic devices. In 1986 he was engaged in the development of BiCMOS logic devices.

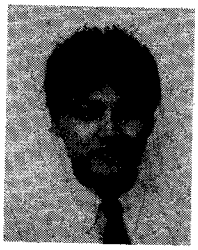
Mr. Niitsu is a member of the Institute of Electronics and Communication Engineers of Japan.



Hiroyuki Miyakawa was born in Gunma, Japan. He received the B.S. degree in electrical engineering in 1982 and the M.S. degree in electrical engineering in 1984 from Hosei University, Tokyo, Japan.

He joined Tamagawa Works, Toshiba Corporation, in 1984. In 1989 he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan, where he was engaged in development of BiCMOS logic devices.

Mr. Miyakawa is a member of the Japan Society of Applied Physics.



Yoshinori Watanabe was born in Mie, Japan, on May 11, 1961. He received the B.S. degree in electronic control engineering from Tokai University, Japan, in 1984.

He joined the Toshiba Microelectronics Corporation, Kawasaki, Japan. He then joined Toshiba's Semiconductor Device Engineering Laboratory, Kawasaki, Japan, where he has been engaged in the research and development of BiCMOS ASIC and BiCMOS memory macros.