Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's

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Abstract—**Controlling *RC* interconnection delay is the key to high-speed VLSI designs [1], [2]. In this paper, a closed-form formula for a waveform of the *RC* line with practical boundary conditions is derived for the first time. Expressions are also derived for a voltage slope and transition time of the *RC* interconnection. Other important issues related to interconnections are capacitive coupling of two lines and crosstalk induced by the capacitive coupling. Expressions are derived for a coupling capacitance and a crosstalk voltage height, which can be used in VLSI designs. Using the expressions, optimum linewidth that minimizes *RC* delay, and the trend of *RC* delay in the scaled-down VLSI's are discussed.**

I. Introduction

INTERCONNECTION delay, coupling, and crosstalk are important in realizing recent high-performance VLSI's and will become increasingly important as the feature size of the lines is miniaturized and line length is increased. The situation is illustrated in Fig. 1. *RC* delay increases because of the thinner and longer interconnections and the coupling capacitance between adjacent lines increases in relation to the total capacitance. The crosstalk problem gets eminent when mixed CMOS/ECL signals are used on a chip.

An aluminum interconnection of 20-mm length and 0.5-mm width will show *RC* delay of 3 ns (0 to 90% rise time), assuming that its sheet resistance is 35 mΩ and that its capacitance is 0.11 fF/μm. This delay is about 40 times longer than an inverter switching time of the same generation and is about 5 times longer than an optimized buffer delay [12] to drive the pure capacitance of the interconnection. In this sense, analyzing *RC* interconnection delay is important [3]. In Section II, a closed-form formula for a waveform of an *RC* line with practical boundary conditions is derived for the first time in order to understand the behavior of an *RC* interconnect. In the section, simple formulas for a voltage slope and a transition time of the *RC* line are also given.

In Section III, a simple formula for the capacitive coupling is proposed and using the formula, the optimum linewidth that minimizes the *RC* delay is discussed. The trend of *RC* delay in the scaled-down VLSI's is also treated in the section. A crosstalk induced by capacitive coupling is analyzed in Section IV and useful expressions are derived for a crosstalk voltage height. Section V is dedicated to conclusions.

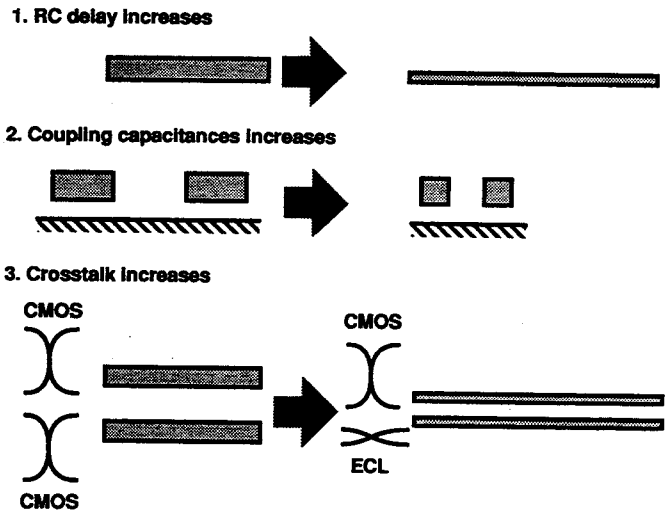

Fig. 1. Three major interconnection problems in scaled-down VLSI's.

II. Voltage Waveform and Delay of an *RC* Interconnection

Consider a distributed *RC* line which is driven by a voltage source with an internal resistor of r_t, and loaded with capacitor of c_t as shown in Fig. 2. This model represents a point-to-point single-layer interconnection driven by a transistor and connected to the next gate, and is widely used in VLSI design theory [1]. Since the characteristic impedance of signal lines in VLSI's is much less than the resistance of the lines whose *RC* delay is of importance, the inductive effects are neglected in this paper [1]. A differential equation for the system can be written as

$$\frac{1}{r}\frac{\partial^2 V}{\partial x^2} = c\frac{\partial V}{\partial t} \tag{1}$$

where $r(c)$ is unit length resistance (capacitance) of the line. The voltage at the far end of the line $V(l, t)$ can be expressed in a series expanded form [2].

$$\frac{V(l,t)}{E} = 1 + \sum_{k=1}^{\infty} K_k e^{-\sigma_k \cdot t/RC} \approx 1 + K_1 e^{-\sigma_1 \cdot t/RC} \tag{2}$$

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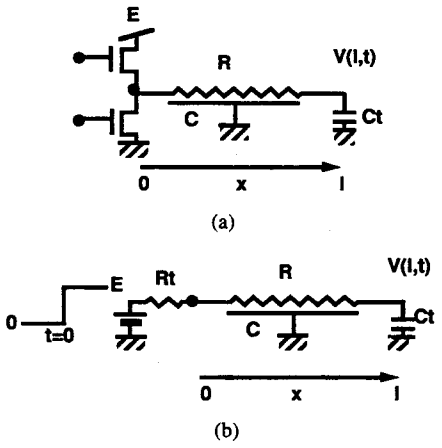


Fig. 2. A model and notation of an interconnection driven by a resistive voltage source and loaded with a capacitor. (a) Circuit and (b) model of an RC interconnection.

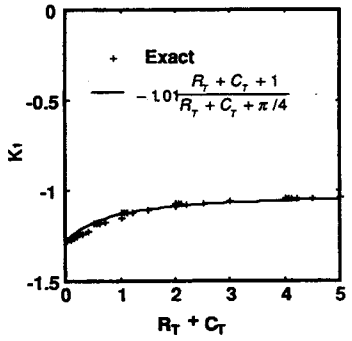


Fig. 3. Comparison between the exact value of K_1 and a simple formula.

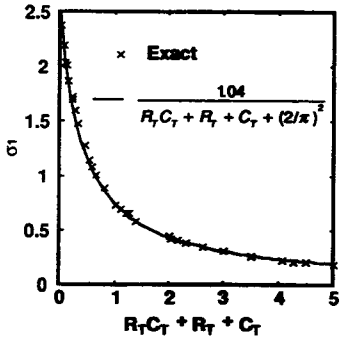


Fig. 4. Comparison between the exact value of σ_1 and a simple formula.

where $R(C)$ is total resistance (capacitance) of the line and calculated as $R = rl(C = cl)$ with l being the length of the line. σ_k's are the roots of the following equation and $(k - \frac{3}{2})\pi < \sqrt{\sigma_k} < (k - \frac{1}{2})\pi$. Since the original paper [2] contains minor errors in the expressions, they are rewritten here. Hereinafter, R_T and C_T denote R_t/R and C_t/C, respectively.

$$\tan \sqrt{\sigma_k} = \frac{1 - R_T C_T \sigma_k}{(R_T + C_T)\sqrt{\sigma_k}}.$$

Once σ_k's are obtained, K_k's are calculated as

$$K_k = (-1)^k \frac{2}{\sqrt{\sigma_k}} \frac{\sqrt{(1 + R_T^2\sigma_k)(1 + C_T^2\sigma_k)}}{(1 + R_T^2\sigma_k)(1 + C_T^2\sigma_k) + (R_T + C_T)(1 + R_TC_T\sigma_k)}.$$

Because the single-exponent approximation in (2) is excellent for $t/RC > 0.1$ [2]. K_1 and σ_1 are the most essential coefficients. However, they have not yet been given in a closed form. The first contribution of this paper is to give approximate formulas for them as follows:

$$K_1 = -1.01 \frac{R_T + C_T + 1}{R_T + C_T + \pi/4} \tag{3}$$

$$\sigma_1 = \frac{1.04}{R_TC_T + R_T + C_T + (2/\pi)^2}. \tag{4}$$

When $R_T = C_T = 0$, the exact value for K_1 is $4/\pi$ and that for σ_1 is $(\pi/2)^2$. When $R_T = C_T >> 1$, the exact asymptotic value for K_1 is -1 and that for σ_1 is $1/\{(R_T + 1)(C_T + 1)\}$. The above expressions correctly reproduce these asymptotic behaviors. The relative errors of the above functions are graphically shown in Figs. 3 and 4 and are less than 3% for K_1 and less than 4% for σ_1 for any R_T and C_T.

The waveform itself can be expressed as follows:

$$\frac{V(l, t)}{E} = v = 1 - \exp\left(-\frac{t/RC - 0.1}{R_TC_T + R_T + C_T + 0.4}\right). \tag{5}$$

An example of the calculation is shown in Fig. 5 together with the exact response. By solving t in terms of v, a delay expression can be obtained. Let us define t_v as the delay from $t = 0$ to the time when the normalized voltage at the end point reaches $v(=V/E)$. t_v is expressed as

$$\frac{t_v}{RC} = 0.1 + \ln\left(\frac{1}{1 - v}\right)(R_TC_T + R_T + C_T + 0.4). \tag{6}$$

The accuracy of the formula is shown in Fig. 6 and the error is less than 3.5% of RC. For special values of v, that is, for $v = 0.9$ and $v = 0.5$, the following formulas can be derived just by calculating (6):

$$t_{09}/RC = 1.02 + 2.3\,(R_TC_T + R_T + C_T)$$

$$t_{05}/RC = 0.377 + 0.693\,(R_TC_T + R_T + C_T).$$

Similar expressions have been derived for the specific values of $v = 0.9$ [2] and $v = 0.5$ [1]. However, compared with these expressions, (6) is more accurate and more general in the sense that it is possible to calculate complex delay, for example 10%–90% rise time and so on.

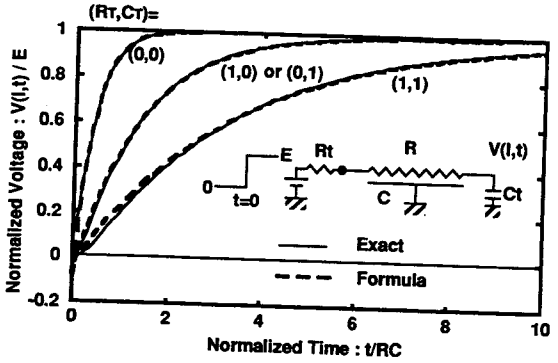


Fig. 5. Voltage waveforms of a distributed RC line.

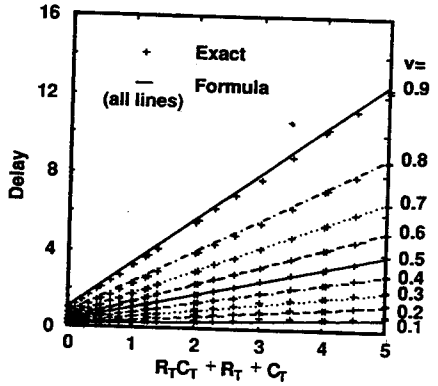


Fig. 6. Comparison of exact delay with a simple formula.

On the other hand, there are widely used Elmore's delay expression [10] and the waveform bounding method [9] to calculate delay in tree-like interconnections. If the waveform bounding method is applied to a distributed RC interconnection with $R_T = C_T = 0$, the relation $0.262 < t_{05}/RC < 0.513$ can be derived. The range is too wide and sometimes not satisfactory in estimating the delay. The accuracy of the waveform bounding method is thus limited while the method can be applied to a more general interconnection system than a simple RC line. The Elmore delay for a distributed RC line is $0.5RC$, which is also not as accurate as (6).

As for a slope of $V(l, t)$ and a transition time t_T, the following expressions can be obtained by just differentiating (2). The transition time is essential in calculating delay of CMOS logic gates [4] and can be calculated from (5) as follows:

$$\left.\frac{dv}{dt}\right|_{v=0.5} = \frac{0.5}{R_T C_T + R_T + C_T + 0.4}$$

$$\frac{t_T}{RC} = 2\,(R_T C_T + R_T + C_T + 0.4).$$

III. Coupling Capacitances and Optimum Linewidth

Simple expressions are derived for coupling capacitances of parallel lines shown in Fig. 7. Formulas for the total capacitances of the same system have been reported

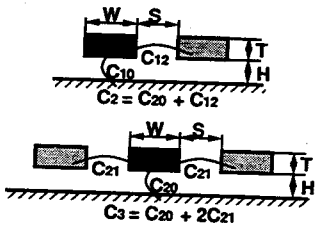


Fig. 7. Notation for coupling capacitances.

in [5] but the coupling capacitance component are not given separately.

$$\frac{C_{21}}{\epsilon_{ox}} = \left[1.93\left(\frac{T}{H}\right)^{1.1} + 1.14\left(\frac{W}{H}\right)^{0.31}\right]\left(\frac{S}{H} + 0.51\right)^{-1.45}$$

(for three lines)

$$\frac{C_{12}}{\epsilon_{ox}} = \left[1.82\left(\frac{T}{H}\right)^{1.08} + \left(\frac{W}{H}\right)^{0.32}\right]\left(\frac{S}{H} + 0.43\right)^{-1.38}$$

(for two lines).

Notation is given in Fig. 7. Relative errors of these formulas are less than 15% for $0.3 \le (T/H), (W/H), (S/H) \le 3.0$. The coefficients are extracted by using the Fast Simulated Diffusion algorithm [6]. The target values for C_{21} and C_{12} are calculated by a numerical method [5], [8].

$$\frac{C_3}{\epsilon_{ox}} = \frac{C_{20} + 2C_{21}}{\epsilon_{ox}} = \frac{C_1}{\epsilon_{ox}} + \left[0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222} + 0.03\left(\frac{W}{H}\right)\right]\left(\frac{S}{H}\right)^{-1.34}$$

(for three lines)

$$\frac{C_2}{\epsilon_{ox}} = \frac{C_{10} + 2C_{12}}{\epsilon_{ox}} = \frac{C_1}{\epsilon_{ox}} + \left[0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222} + 0.03\left(\frac{W}{H}\right)\right]\left(\frac{S}{H}\right)^{-1.34}$$

(for two lines)

$$\frac{C_1}{\epsilon_{ox}} = 2.80\left(\frac{T}{H}\right)^{0.222} + 1.15\left(\frac{W}{H}\right)$$

(for a single line).

Relative errors of the first two formulas are less than 10% for $0.3 < (T/H), (W/H) < 10$, and $0.5 < (S/H) < 10$. The relative error of the single-line formula is less than 6% for $0.3 < (T/H), (W/H) < 30$.

By using these formulas, RC delay is calculated as shown in Fig. 8(a) with a pitch $P(= W + S)$ being fixed. The pitch determines the occupying area, and to fix the pitch corresponds to making the area constant. In order to estimate the worst case delay, it is assumed that three lines are run in parallel and two outer lines are driven by an inverted signal of the center line, that is, the center line feels an effective capacitance of $C_{20} + 4C_{21}$. RC delay in arbitrary units is calculated as $(C_{20} + 4C_{21})/(W/H)$,

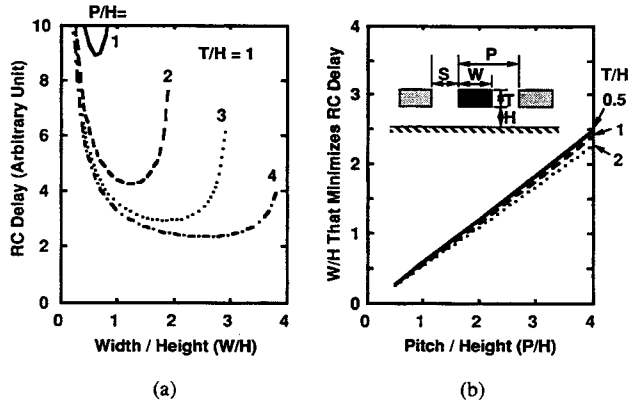


Fig. 8. (a) *RC* delay versus linewidth, and (b) optimum linewidth that minimizes *RC* delay versus pitch of the lines.

where a formula for $C_3 (= C_{20} + 2C_{21})$ is given in [5]. In the calculation, the condition that $R_T = C_T = 0$ is assumed. This represents the case where the *RC* interconnection delay dominates the total delay.

Let us consider here a relationship between the total delay and the *RC* interconnection delay. The total delay D_{TOT} is a sum of buffering delay D_{BUF} and the *RC* interconnection delay t_{05} in (6). It can be assumed that the delay of an inverter depends on a fanout f, e.g., $Af + B$, where A and B are specific to the process technology and, for example, A is 38.1 ps and B is 44.2 ps for a certain 0.5-μm CMOS technology [12]. If the buffer is optimized, the minimized D_{BUF} can be expressed as $(3A + 0.6B) \ln (r_{IN}/r_t)$, where r_t is effective resistance of the driving MOSFET and r_{IN} designates effective MOSFET resistance at the first stage of the buffer [12]. For simplicity, the load capacitance of an *RC* line, c_t, is neglected. Then the following expression holds:

$$D_{TOT} = D_{BUF} + t_{09} = (3A + 0.6B) \ln \left(\frac{r_{IN}}{r_t} \right) + 1.02RC + 2.3r_tC.$$

By minimizing D_{TOT} in terms of r_t, we have

$$D_{TOT} = (3A + 0.6B) \ln \left(\frac{2.3e}{3A + 0.6B} r_{IN}C \right) + 1.02RC.$$

The first term corresponds to the buffering and driving delay and the second term in the *RC* interconnection delay. If typical values for 0.5-μm technology are used, the above expression is reduced to $D_{TOT} = 0.14 \ln (8.01) + 0.0079l^2$, where l is a length of an interconnection measured in millimeters and the delay is measured in nanoseconds.

The specific coefficient values are not important but what is relevant is that the buffering delay is proportional to $\ln (l)$, while the *RC* delay is proportional to l^2. Consequently, for a long interconnection, say longer than 8 mm in 0.5-μm technology, the *RC* interconnection delay surmounts the buffering delay and rapidly becomes dominant for the longer interconnection. Moreover, the inverter delay is decreased as the technology advances. As a result, the *RC* interconnection delay becomes increasingly dominant in the future. This is the reason why only the *RC* delay is considered in the calculation for Fig. 8.

It is seen from Fig. 8(b) that there is an optimum width for a specific pitch in terms of *RC* delay. This is because although resistance decreases linearly as the width increases, capacitance increases rapidly as separation of the lines (S) decreases. Fig. 8(b) shows the optimum linewidth versus pitch for various thicknesses. The optimum width is about half the pitch as long as the pitch is less than 4 times the height.

Fig. 9 shows a trend of *RC* delay in a bus structure. In a bidirectional bus structure, it is difficult to use the repeater technique described in [1]. Again it is assumed that $R_T = C_T = 0$ and it is also assumed that three lines are run in parallel and two outer lines are driven by an inverted signal of the center line, that is, the center line feels an effective capacitance of $C_{20} + 4C_{21}$. In the calculation, H, T, W, and S are assumed to be 1 μm in the year 1990, taking into account the above-mentioned optimum width discussion. The sheet resistance in the year 1990 is assumed to be 30 mΩ. The feature size is scaled exponentially from 1 μm in 1990 to 0.25 μm in the year 2000. The chip side length is increased exponentially from 10 mm in 1990 to 25 mm in 2000.

Four scaling scenarios are considered. One is that all of H, T, W, and S are scaled down in accordance with the feature size. In this scenario, the *RC* delay rapidly increases as the feature size is shrunk. In the other extreme, a totally unscaled case is considered. In this case, if the interconnection length is not increased, the *RC* delay remains constant. Between these two extremes, two other schemes are considered in the figure. In the four scenarios, the unscaled interconnection scheme is by far the most attractive. To realize this scenario, at least one vertically unscaled metal layer is required.

IV. Crosstalk

Crosstalk between two parallel *RC* lines is another important issue in VLSI designs. For example, in BiCMOS VLSI's where both of CMOS large-swing logic signals and ECL small logic signals coexist on a chip, malfunctions may occur if crosstalk induced by the CMOS signal on the ECL signal line is so large that the noise on the ECL signal goes across the logic threshold of ECL gates.

The basic differential equations which govern two capacitively coupled *RC* lines see Fig. 10) are as follows:

$$\begin{cases} \dfrac{1}{r_1} \dfrac{\partial^2 V_1}{\partial x^2} = (c_1 + c_c) \dfrac{\partial V_1}{\partial t} - c_c \dfrac{\partial V_2}{\partial t} \\ \dfrac{1}{r_2} \dfrac{\partial^2 V_2}{\partial x^2} = (c_2 + c_c) \dfrac{\partial V_2}{\partial t} - c_c \dfrac{\partial V_1}{\partial t}. \end{cases}$$

In these equations, $r_1 (r_2)$ and $c_1 (c_2)$ are resistance and capacitance to the ground per unit length of line 1 (2), respectively. c_c signifies coupling capacitance between the two *RC* lines per unit length. $V_1 (V_2)$ designates a voltage

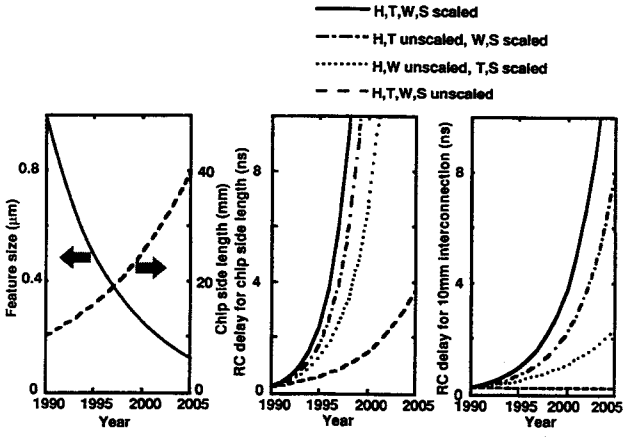


Fig. 9. Future trend of bus RC delay. (a) Trend of the feature size and chip side length. (b) 0%-90% RC delay for chip side long interconnection with various scaling strategies. (c) Trend of 0%-90% delay for 10-mm-long interconnection with various scaling strategies.

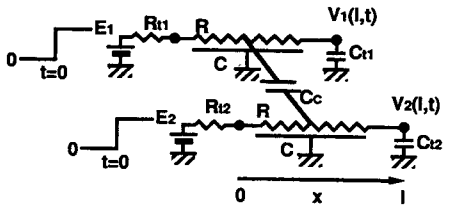


Fig. 10. Notation for capacitively coupled RC lines.

of line 1 (2). For simplicity, it is assumed in this paper that $r_1 = r_2 = r$ and $c_1 = c_2 = c$. The above differential equations are simplified if the following V_+ and V_- are used: $V_+ = (V_1 + V_2)/\sqrt{2}$ and $V_- = (V_1 - V_2)/\sqrt{2}$. The resulted equations using these V_+ and V_- are

$$\begin{cases} \dfrac{\partial^2 V_+}{\partial x^2} = rc \dfrac{\partial V_+}{\partial t} \\ \dfrac{\partial^2 V_-}{\partial x^2} = r(c + 2c_c) \dfrac{\partial V_-}{\partial t}. \end{cases}$$

Since these equations have the same form as (1), the approximate expressions for both V_+ and V_- can be obtained by using the result of Section II. Transforming V_+ and V_- back into V_1 and V_2 yields closed-form expressions for the voltage waveforms as follows:

$$\begin{cases} V_1(l,t) \approx E_1 + \dfrac{K_1}{2}\left[(E_1 + E_2)\exp\left(-\sigma_1 \dfrac{t}{RC}\right) + (E_1 - E_2)\exp\left(-\sigma_1 \dfrac{t}{RC + 2RC_c}\right)\right] \\ V_2(l,t) \approx E_2 + \dfrac{K_1}{2}\left[(E_1 + E_2)\exp\left(-\sigma_1 \dfrac{t}{RC}\right) - (E_1 - E_2)\exp\left(-\sigma_1 \dfrac{t}{RC + 2RC_c}\right)\right]. \end{cases} \quad (7)$$

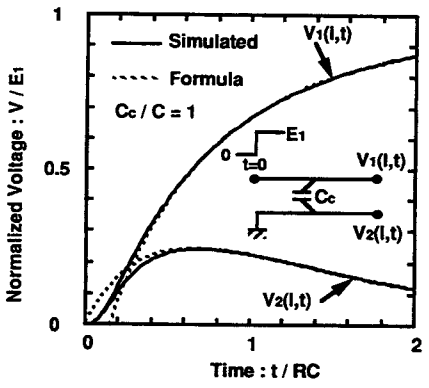


Fig. 11. Simulated and calculated waveforms of capacitively coupled RC lines.

In these expressions, R, C, and C_c denote rl, cl, and $c_c l$, respectively, where l is the length of the lines. In calculating K_1 and σ_1, (3) and (4) are valid with substitutions that $R_T = R_{t1}/R = R_{t2}/R$ and $C_T = C_{t1}/C = C_{t2}/C$. Calculated results of these formulas are compared with simulated waveforms with SPICE [7] in Fig. 11. SPICE simulation is carried out by using 10- step π-ladder circuit to approximate distributed RC lines. In Fig. 11, it is assumed that $E_2 = 0$ and $R_T = C_T = 0$.

It is understood from the expressions that if two lines are driven by in-phase signals ($E_2 = E_1$), the behavior of the lines is just the same as that of a distributed line with capacitance of C. If two lines are driven by off-phase signals ($E_2 = -E_1$), the behavior of the line is the same as that of a distributed line with capacitance $C + 2C_c$. If $E_2 = 0$, line 1 shows a faster response than a distributed line with capacitance $C + 2C_c$.

Suppose that $E_2 = 0$, then a peak value of $V_2(l, t)$, V_P, is a noise height induced by the capacitive crosstalk. If V_P is higher than a logic threshold voltage of an ECL gate, a malfunction may occur in BiCMOS LSI's as mentioned above. V_P can be obtained by differentiating (7).

$$\frac{V_P}{E_1} = K_1 \left(\frac{1}{1 + 2\eta}\right)^{1/2\eta} \left(\frac{\eta}{1 + 2\eta}\right) \approx \frac{1}{2}\frac{\eta}{1 + \eta} \quad (8)$$

where η stands for C_c/C. These formulas are plotted graphically in Fig. 12 for $R_T = C_T = 0$ and can be used in estimating crosstalk noise. The approximate expression $(\eta/2(1 + \eta))$ holds when $R_T = C_T = 0$ and $\eta \leq 2$. It should be noted that the factor $\eta E_1/(1 + \eta)(= CE_1/(C + C_c))$ is a statically pulled up voltage of a middle point of two serially connected capacitors whose capacitances are C_c and C. The dynamic peak noise V_P is about half the height of the statically pulled up voltage.

When R_{t1} is zero and R_{t2} is finite, an expression for V_P becomes as follows:

$$\frac{V_P}{E_1} \approx \frac{\frac{1}{2} + R_{T2}}{1 + R_{T2}} \frac{\eta}{1 + \eta}.$$

This case is important because the value of V_P becomes higher than the value of (8), and hence the system shows

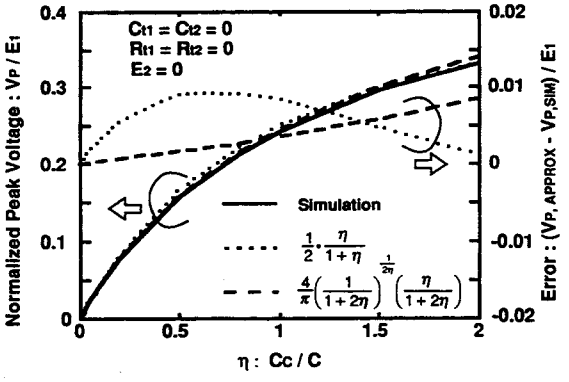
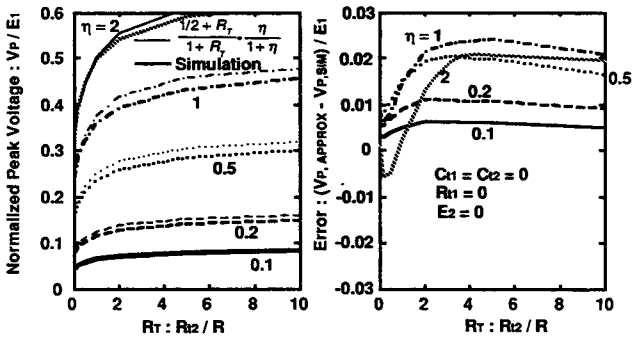


Fig. 12. Peak crosstalk voltage ($R_T = 0$ case) and error of a simple formula.



(a) (b)

Fig. 13. (a) Peak crosstalk voltage ($R_T \neq 0$ case) and (b) error of a simple expression.

worse crosstalk characteristics. The finite R_{t2} means that line 2 is not pinned down so firmly.

A comparison between formula calculation and simulation results is given in Fig. 13(a) together with the approximation error in Fig. 13(b). The maximum error is less than 3% of E_1. The formula holds when $R_{T1} = C_T = 0$ and $\eta \leq 2$ and reproduces the correct asymptotic behavior when $R_{T2} << 1$ and $R_{T2} >> 1$.

V. Conclusions

Simple yet practical expressions are derived for *RC* interconnection delay and voltage waveform. The expressions are more general and accurate than those previously published. Secondly, simple formulas for coupling capacitances are proposed, whose errors are less than 15% for the practical range of parameters. Using the formula, the optimum width to minimize a bus *RC* delay is calculated. The optimum point is shown to be about half of the pitch as long as the pitch is less than 4 times the height. The future trend of *RC* delay is also analyzed and it is shown that some type of unscaled interconnection is effective in reducing the *RC* delay. These formulas are useful in understanding and attacking interconnection-related problems in the future VLSI's.

Finally, crosstalk between adjacent *RC* lines is treated and expressions for waveforms and peak-noise height for the interconnection system are given. In mixed-signal VLSI's, where, for example, ECL and CMOS signals coexist on a chip, the large voltage swing signal causes harmful effects on the small voltage swing signal. The effect is estimated by using the crosstalk formulas presented here.

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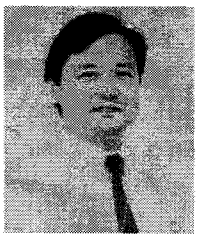

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