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INVITED PAPER *Special Issue on Low-Voltage Low-Power Integrated Circuits*

Overview of Low-Power ULSI Circuit Techniques

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SUMMARY This paper surveys low-power circuit techniques for CMOS ULSIs. For many years a power supply voltage of 5 V was employed. During this period power dissipation of CMOS ICs as a whole increased four-fold every three years. It is predicted that by the year 2000 the power dissipation of high-end ICs will exceed the practical limits of ceramic packages, even if the supply voltage can be feasibly reduced. CMOS ULSIs now face a power dissipation crisis. A new philosophy of circuit design is required. The power dissipation can be minimized by reducing: 1) supply voltage, 2) load capacitance, or 3) switching activity. Reducing the supply voltage brings a quadratic improvement in power dissipation. This simple solution, however, comes at a cost in processing speed. We investigate the proposed methods of compensating for the increased delay at low voltage. Reducing the load capacitance is the principal area of interest because it contributes to the improvement of both power dissipation and circuit speed. Pass-transistor logic is attracting attention as it requires fewer transistors and exhibits less stray capacitance than conventional CMOS static circuits. Variations in its circuit topology as well as a logic synthesis method are presented and studied. A great deal of research effort has been directed towards studying every portion of LSI circuits. The research achievements are categorized in this paper by parameters associated with the source of CMOS power dissipation and power use in a chip.

key words: *LSI, CMOS, low-power, low-voltage, power-delay product, energy-delay product, pass-transistor logic*

1. Introduction

"CMOS circuits dissipate little power by nature." So believed circuit designers. But in reality, CMOS power dissipation as a whole has increased by 4 times every 3 years, which is the same pace as increase in bit density of state-of-the-art DRAMs! Figure 1 plots power dissipation of MPUs and DSPs presented in the ISSCC for the past 15 years. The power dissipation has increased by 1000 times over the 15 years and is exceeding 10 watts. Designers are to be looking at CMOS circuits in a new light.

Why is CMOS power dissipation becoming so large? The reason can be found in scaling principles shown in Table 1. A "constant field scaling" theory formulated by Dennard et al. [1] assumes that device voltages as well as device dimensions are scaled by a scaling factor $\chi(>1)$, resulting in a constant electric field in the device. This brings a desirable effect that, while power density remains constant, circuit performance can be improved in terms of density (χ^2), speed (χ), power ($1/\chi^2$), and the power-delay product ($1/\chi^3$). Almost limitless progress in CMOS ICs is promised with this scaling scenario. But in practice, neither a supply voltage, V_{DD}, nor a threshold voltage of MOSFETs, V_{th}, had long been scaled till 1990. The resultant effect is better explained with a scaling theory called "constant voltage scaling." With the constant voltage scaling, circuit speed is further improved (χ^2), while power density increases very rapidly by χ^3. For more precise analysis in the submicron region [2], the power density increases by $\chi^{\alpha+1}$, where α represents velocity saturation effects and is typically 1.3 for 0.5

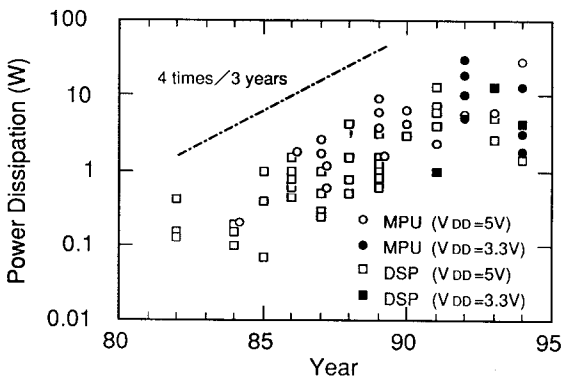

Fig. 1 Power dissipation of MPUs and DSPs presented in the ISSCC for the past 15 years.

Table 1 Influence of scaling on MOS device characteristics.

PARAMETER		SCALING MODEL		
		Constant field	Constant voltage	$\propto 1/\kappa^{0.5}$ voltage
Device size		$1/\kappa$	$1/\kappa$	$1/\kappa$
Gate-oxide thickness	tox	$1/\kappa$	$1/\kappa$	$1/\kappa^{0.5}$
Substrate doping		κ	κ^2	$\kappa^{1.5}$
Supply voltage	V	$1/\kappa$	1	$1/\kappa^{0.5}$
Electric field	E	1	κ	1
Current	I	$1/\kappa$	κ $(\kappa^{\alpha-1})$	$1/\kappa$
Area	A	$1/\kappa^2$	$1/\kappa^2$	$1/\kappa^2$
Capacitance	$C=\varepsilon A/tox$	$1/\kappa$	$1/\kappa$	$1/\kappa^{1.5}$
Gate delay	VC / I	$1/\kappa$	$1/\kappa^2$ $(1/\kappa^{\alpha})$	$1/\kappa$
Power dissipation	VI	$1/\kappa^2$	κ $(\kappa^{\alpha-1})$	$1/\kappa^{1.5}$
Power density	VI / A	1	κ^3 $(\kappa^{\alpha+1})$	$\kappa^{0.5}$
Power-delay product	CV^2	$1/\kappa^3$	$1/\kappa$	$1/\kappa^{2.5}$

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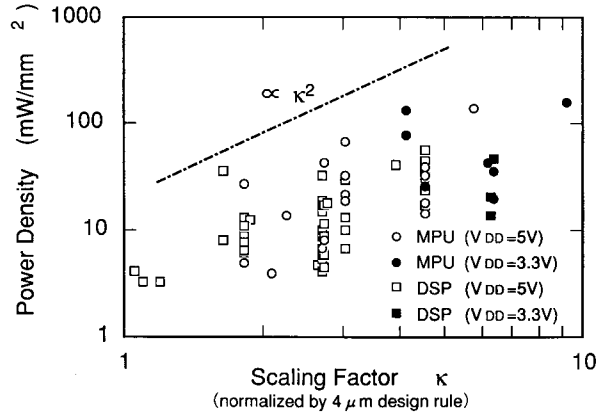

Fig. 2 Power density dependence on scaling factor normalized by 4 μm design rules.

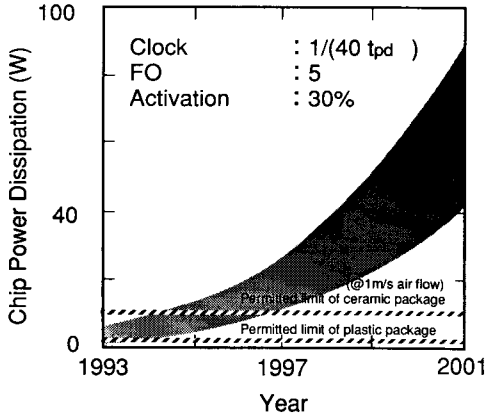

Fig. 3 Prediction of CMOS power dissipation by the year 2001.

μm MOSFETs. This constant voltage scaling causes the rapid increase in CMOS power dissipation. This inference is verified by Fig. 2 where the power density dependence on the scaling factor is plotted using the data in Fig. 1.

A real move to 3.3V or even lower supply voltage is being seen. One of the driving forces is increasing packaging and cooling cost of CMOS LSIs. The permitted limit of chip power dissipation in an inexpensive plastic package is a little over 1 W. Above the criterion, an expensive ceramic package is necessary which cannot meet a tight budget for consumer LSIs at all. Another motivation is emerging battery-operated applications for multimedia that demand intensive computation in portable environments. Furthermore, TTL interface is reaching its speed limit and an alternative is being developed where people don't have to stick to the 5 V supply voltage framework. This is also one of the background reasons. As shown in Fig. 1, the power dissipation is still increasing even under the reduced supply voltage.

How is the CMOS power dissipation changing in future? The $\chi^{\alpha+1}$ increase in power density with the constant voltage scaling cannot be accepted. The constant field scaling is not realistic due to auxiliary factors in MOSFETs such as a subthreshold current slope. Many alternative scaling approaches have been proposed. Scaling V_{DD} by $\chi^{0.5}$ is reported to satisfy both device reliability and circuit performance [3]. The resultant effect is summarized in Table 1. With this scaling approach the increase in power density is held down to $\chi^{0.5}$. In Fig. 3, CMOS power dissipation by the year 2001 is predicted, assuming that the $\chi^{0.5}$ supply voltage scaling is carried out, or assuming that a little bit gradual scaling scenario of $\chi^{0.33}$ is applied. χ is assumed to be 1.26 per year, which is the same scaling factor as has been applied so far. It is predicted that by the year 2000 the power dissipation would exceed that of ECL ICs, even if the supply voltage is appropriately scaled down. CMOS ULSIs are facing a power dissipation crisis. A new philosophy of circuit design is required.

The CMOS power dissipation is analyzed in Sect. 2. The power dissipation can be minimized by reducing: 1) the supply voltage, 2) the load capacitance, 3) switching activity. Reducing the supply voltage is studied in Sect. 3. The capacitance reduction is discussed in Sect. 4. Pass-transistor logic is attracting attention as it comprises fewer transistors and exhibits smaller stray capacitance than conventional CMOS static circuits. Variations in its circuit topology as well as a logic synthesis method are presented and studied in this section. In Sect. 5, an overview of low-power circuit techniques is given as summary.

2. Analysis of CMOS Power Dissipation

CMOS power dissipation is given by

$$P = p_t \cdot (C_L \cdot V_S + \overline{I_{SC}} \cdot \Delta t_{SC}) \cdot V_{DD} \cdot f_{CLK} + (I_{DC} + I_{LEAK}) \cdot V_{DD}. \quad (1)$$

The first term, $p_t \cdot C_L \cdot V_S \cdot V_{DD} \cdot f_{CLK}$, represents dynamic dissipation due to charging and discharging of the load capacitance, where p_t is the switching probability, C_L is the load capacitance, V_S is the voltage swing, and f_{CLK} is the clock frequency. In most cases, V_S is the same as V_{DD}, but in some logic circuits V_S may be smaller than V_{DD} for high-speed and/or low-power operation. The second term, $p_t \cdot \overline{I_{SC}} \cdot \Delta t_{SC} \cdot V_{DD} \cdot f_{CLK}$, is dynamic dissipation due to switching transient current, where $\overline{I_{SC}}$ is the mean value of the switching transient current, and Δt_{SC} is time while the switching transient current draws. This dissipation can be held down by careful design [4]. The third term, $I_{DC} \cdot V_{DD}$, is static dissipation in such a circuit as a current mirror sense amplifier where current is designed to draw continuously from the power supply. The last term, $I_{LEAK} \cdot V_{DD}$, is due to the subthreshold current and the reverse bias leakage between the source-drain diffusions and the

substrate. The dominant term in a well-designed logic circuit is the charging and discharging term, and CMOS power dissipation is given by

$$P \approx p_t \cdot C_L \cdot V_{DD}^2 \cdot f_{CLK}. \quad (2)$$

Reducing the supply voltage brings a quadratic improvement in the power dissipation. This simple solution to low-power designs, however, comes at the cost of a speed penalty. As V_{DD} approaches the sum of the threshold voltages of the devices, the circuit delay increases drastically. Compensation for the increased delay at low voltage is required. Reducing the load capacitance, on the other hand, contributes to the improvement of both power dissipation and circuit speed, and is therefore most principle. The physical capacitance can be minimized through the utilization of certain circuit styles, as well as device miniaturization. Reducing the switching activity has recently been paid attention. A problem to calculate the switching probability of a series connected logic circuits is found to be very time consuming (i.e. NP-Complete). A fast power estimation tool is expected for low-power LSI design. Power loss by glitching is reported to amount to 15% to 20% of the total power dissipation [5]. Optimum logic structures to reduce hazards should be investigated. This paper focuses the discussion associated with voltage and capacitance reduction in the following sections.

3. Voltage Scaling

Lowering the supply voltage is the most attractive choice due to the quadratic dependence. However, as the supply voltage becomes lower, the circuit delay increases and the LSI throughput degrades. There are three means to maintain the throughput: 1) reduce V_{th} to improve circuit speed, 2) introduce parallel and pipelined architecture while using slower device speeds, 3) prepare multiple supply voltages and for each cluster of circuits choose the lowest supply voltage that satisfies the speed requirements.

The second approach is discussed in [6] in detail. The idea here is to utilize the increasing transistor density to provide additional circuits to parallelize the computation, and trade off silicon area against power consumption. This idea is basically based on almost "limitless" number of transistors, which has not yet been obtained. In reality, chip sizes are still increasing even though the transistor density is increasing by 60% per year. It should also be pointed out that the algorithm that is being implemented may be sequential in nature and/or have feedback, which will limit the degree of parallelism.

The problem in the third approach is the necessity of level conversion every time signals interface the circuit clusters in different supply voltages. A good level converter should be developed which exhibits small delay, consumes little power, and occupies small pattern area. How efficiently can circuits be clustered with the minimum number of the interface is another discussion issue. In this section, lowering both V_{DD} and V_{th} is investigated.

3.1 Optimizing V_{DD} and V_{th}

The I_D-V_{GS} characteristic of short-channel MOSFETs has an α-law dependence (typically α is 1.3 for 0.5 μm MOSFETs) [7] due to velocity saturation effects:

$$I_{DS} = \beta \cdot (V_{GS} - V_{th})^{\alpha}. \quad (3)$$

The circuit delay D is then approximated as

$$D = \gamma \cdot \frac{Q}{I_{DSO}} = \frac{\gamma \cdot C_L \cdot V_{DD}}{\beta \cdot (V_{DD} - V_{th})^{\alpha}}. \quad (4)$$

Taking the charging and discharging current and the leak current into account, the CMOS power dissipation is given by

$$P = p_t \cdot C_L \cdot V_{DD}^2 \cdot f_{CLK} + I_{LEAK} \cdot V_{DD}, \quad (5)$$

where

$$f_{CLK} = \frac{1}{nD},$$

$$I_{LEAK} = \lambda \cdot W \cdot \exp\left\{\frac{-V_{th}}{S}\right\},$$

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_D}{C_{ox}}\right). \quad (6)$$

n is the logic depth, k is Boltzmann's constant, T is temperature, C_D is the depletion-layer capacitance, and C_{ox} is the gate capacitance. For with $W_P = 10$ μm, $W_n = 5$ μm, $p_t = 0.3$, $n = 30$, fanout $= 2$, and other parameters for a 0.4 μm CMOS device, the power dissipation and the circuit delay are calculated in various V_{DD} and V_{th}, and the results are plotted in Figs. 4(a) and (b), respectively. Figure 4(b) indicates that the increasing delay with low V_{DD} can be compensated by lowering V_{th}. The delay contour lines are provided on the $V_{DD} - V_{th}$ plane in Fig. 4(b).

The power-delay (PD) product is calculated and plotted in Fig. 4(c). The PD product can be interpreted as the amount of energy expended in each switching event. The dimension is joule (watt$\times$second), or watt/MIPS. By ignoring the subthreshold leak current in (5), the PD product is given by

$$P \cdot D = \frac{p_t}{n} \cdot C_L \cdot V_{DD}^2. \quad (7)$$

This suggests that the energy expended in every circuit transition is independent of the circuit speed (and V_{th} when $V_{th} \geqq 0.1$ V). In order to save the energy, it is desirable to operate a circuit at the slowest possible speed with the lowest possible supply voltage. The PD product is considered to be a good index for those who

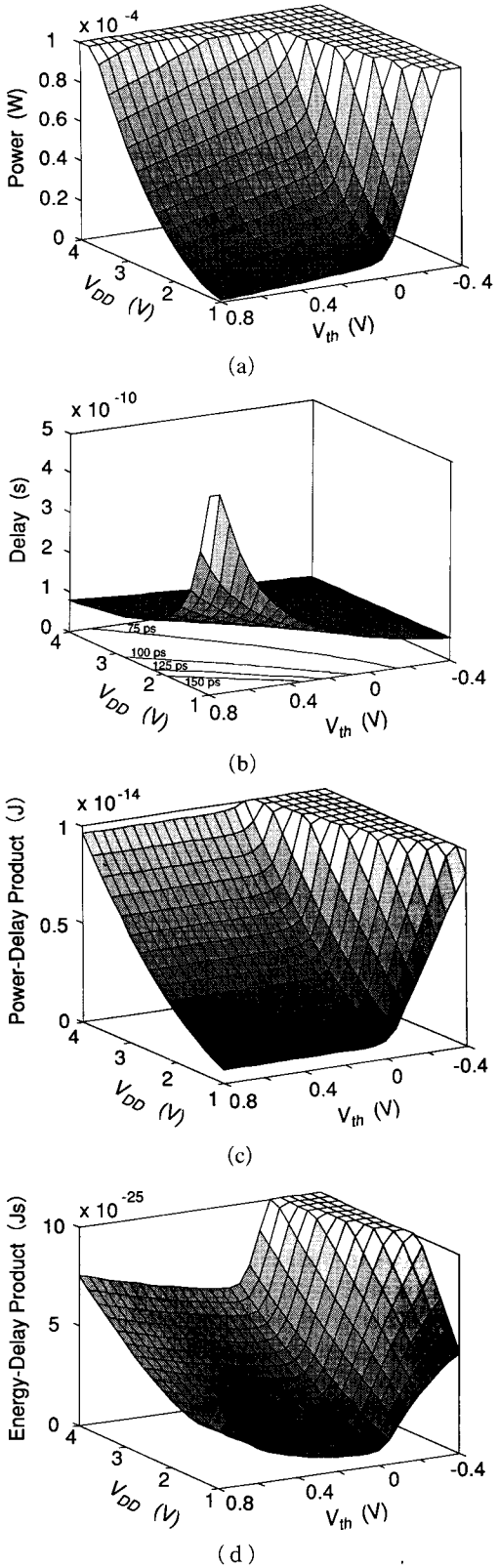

Fig. 4 Simulated (a) power dissipation, (b) circuit delay, (c) power-delay product, (d) energy-delay product, dependence on supply voltage and threshold voltage. Assumption: $W_p=10$ μm, $W_n=5$ μm, $V_{thp}=V_{thn}$, $p_t=0.3$, fanout=2, logic depth=30 stages, and other parameters for a 0.4 μm CMOS.

care mostly about battery consumption. However, most of the applications of today requires near-peak performance throughput. The PD product gives no information about the trade-off between energy and speed.

In discussing the trade-off between energy and speed, the energy-delay space is explored to find the most energy saving solution under a given speed constraint. The energy-delay (ED) product, that is PD^2, can be an important index for those who care about speed as much as energy. Figure 4(d) shows the calculation results which suggest V_{th} be lowered to about 0.1 V to minimize the ED product. For example, if V_{DD} is reduced from 3.3 V to 1.0 V, the delay of CMOS circuit in $V_{th}=0.7$ V is increased by a factor of 5. However, if V_{th} is reduced to 0.1 V, the delay increase is held down to only 20%. Consequently, the power dissipation can be reduced to below 1/10, while almost maintaining the circuit speed.

3.2 Controlling V_{th} Fluctuation

V_{th} fluctuation due to process variation is presently around ± 0.15 V, but this value should be scaled down in the low voltage operation. Figure 5 shows how much the V_{th} fluctuation affects the circuit delay in various V_{DD}. It is seen from the figure that the V_{th} fluctuation of ± 0.15 V gives less than 5% speed variation in 5 V V_{DD}, while the same amount of the V_{th} fluctuation doubles the delay in 1 V V_{DD}. For example, if it is specified that 0.4 V is the minimum V_{th} to keep a total leakage current of a VLSI within a specification, the center value of V_{th} should be set 0.55 V. The worst chips then show the V_{th} of 0.7 V. The V_{th} distribution of this case is illustrated by a shaded region in Fig. 5. If the V_{th} fluctuation can be reduced to ± 0.05 V, the worst V_{th} becomes 0.5 V. This case is indicated by another shaded region in the figure. The worst case speed difference between the two V_{th} fluctuation cases is a factor of 1.3 for 1.5 V V_{DD} and a factor of 3 for 1 V V_{DD}.

A new circuit technique was developed to reduce

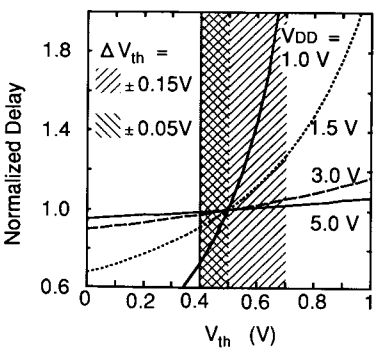

Fig. 5 Calculated circuit delay dependence on V_{th} in various V_{DD}.

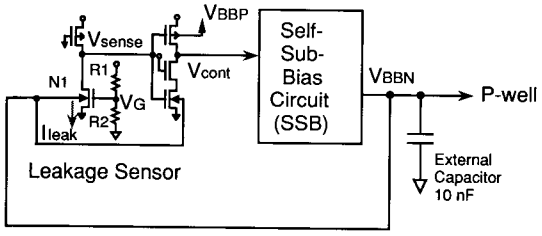

Fig. 6 Circuit diagram of self-adjusting V_{th} scheme.

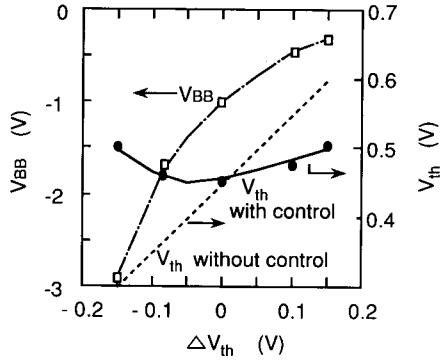

Fig. 7 Measured V_{th} controllability dependence on process fluctuation ΔV_{th}.

the V_{th} fluctuation by using self-substrate-biasing [8]. Figure 6 shows a circuit diagram. A leakage sensor senses leakage current of a representative MOSFET, N1, amplifies it by a load pMOS, and outputs a control signal, Vcont, to a Self-Substrate-Bias (SSB) circuit. The leakage current can vary by a factor of 10 when V_{th} is changed by 0.1 V. V_G is set around 0.2 V to enhance the leakage current. Vcont is controlled such that it triggers the SSB only when the leakage is higher than a certain level. In an nMOS case, the SSB, when triggered, draws charge from P-wells, and lowers a substrate voltage. V_{th} is then increased to reduce the leakage currents. Thus, the substrate bias is controlled such that leakage current of the MOSFETs is adjusted constant. Figure 7 shows a measured V_{th} static controllability which is found to be less than ± 0.025 V. The delay of the sensor introduces dynamic controllability. The overall V_{th} controllability including static and dynamic effects is ± 0.05 V.

4. Capacitance Reduction

Total load capacitance is the sum of gate capacitance, diffusion capacitance, and routing capacitance. The ratio is case-by-case, but may often be almost even. Using small number of transistors or small size of transistors contributes to the reduction in the gate capacitance and the diffusion capacitance. Pass-transistor logic may have this advantage because it comprises fewer transistors and exhibits smaller stray capacitance than conventional CMOS static logic. As

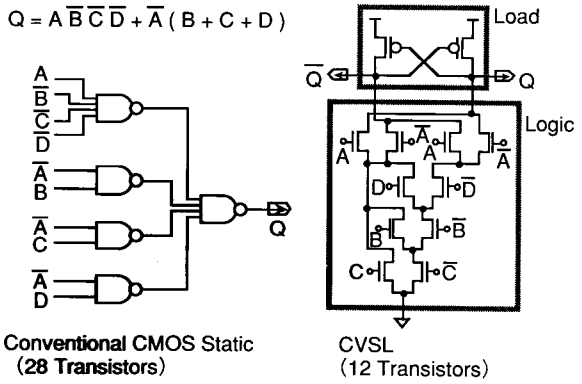

Fig. 8 CVSL.

for the transistor size, there is a study [9] reporting that through a size optimization, the total size of one million transistors in a gate array design was reduced to 1/8 of original design while maintaining the circuit speed. The total load capacitance was therefore reduced to 1/3 and 55% of the power dissipation was saved on average. It is often seen that bigger transistors are used in macrocells in a cell library so that they can drive even a long wire within an acceptable delay time. As device size is miniaturized, the routing capacitance places weight. Layout tools should take power dissipation of long wires into account as well as speed and pattern density.

In this way, the whole design system including a cell library and CAD environments should be reexamined. In this section, pass-transistor logic is studied which is expected as a post CMOS logic for low power design.

4. 1 Pass-Transistor Logic

Historically speaking, pass-transistor logic was derived from a Cascade Voltage Switch Logic (CVSL) [10] which was developed in 1984. CVSL is constructed of stacked nMOS differential pairs which are connected to a pair of cross-coupled pMOS loads for pull-up. No dc current draws in static. Differential pairs stacked in N-level can implement a logic with a maximum of $2^N - 1$ inputs. Therefore, complicated logic which may require several gates in conventional CMOS can be implemented in a single stage gate in CVSL. For example, as shown in Fig. 8, a logic $Q = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot (B + C + C)$ can be implemented with 28 transistors in conventional CMOS. With including inverter gates for generating the complement inputs, the total number of transistors becomes 36. On the other hand, in CVSL 12 transistors make the logic; hence stray capacitance in gate and drain of MOSFETs can be reduced to 1/3.

In 1985 further refinement lead to a Differential Split-Level Logic (DSL) [11] depicted in Fig. 9. In DSL the "H" level of the nMOS logic is clamped by the n-transistors whose gates are biased to $(V_{DD}/2)$

reduces the signal swing to half in the circuits to gain speed.

and DSL were closely examined in [12]. results of full adders in CMOS, CVSL and summarized in Table 2. Contrary to the ation, CVSL is slower than CMOS. This is e during the switching action, the nMOS pull-down trees have to "fight" the cross-coupled pMOS loads which are holding the previous data. Reducing the size of the cross-coupled pMOS transistors helps to gain the switching speed at the cost of degradation in drive capability. Both CVSL and DSL consume almost twice as big dynamic power as CMOS. Different current paths through the nMOS stacked trees for the compliment inputs can cause signal skew on the output. If the two compliment outputs in the nMOS pull-down trees become "L" simultaneously, the cross-coupled pMOS loads don't flip and draw large current. DSL is fast, but consumes larger static power. This is because the clamped "H" level of $V_{DD}/2$ yields leak current through one of the pMOS loads which should be turned off. The PD product and the ED product indicate that neither CVSL nor DSL outperforms CMOS in spite of the reduced stray capacitance.

The nMOS logic circuits in CVSL and DSL can drive only "L" level, and therefore the cross-coupled pMOS loads are necessary for driving "H" level. Pass-transistor circuits, on the other hand, can drive both "H" and "L" levels so that they don't need the cross-coupled pMOS loads. Modifications and derivations of pass-transistor logic have been proposed such as CPL, DPL, DCVSPG, SRPL, and SAPL. Their

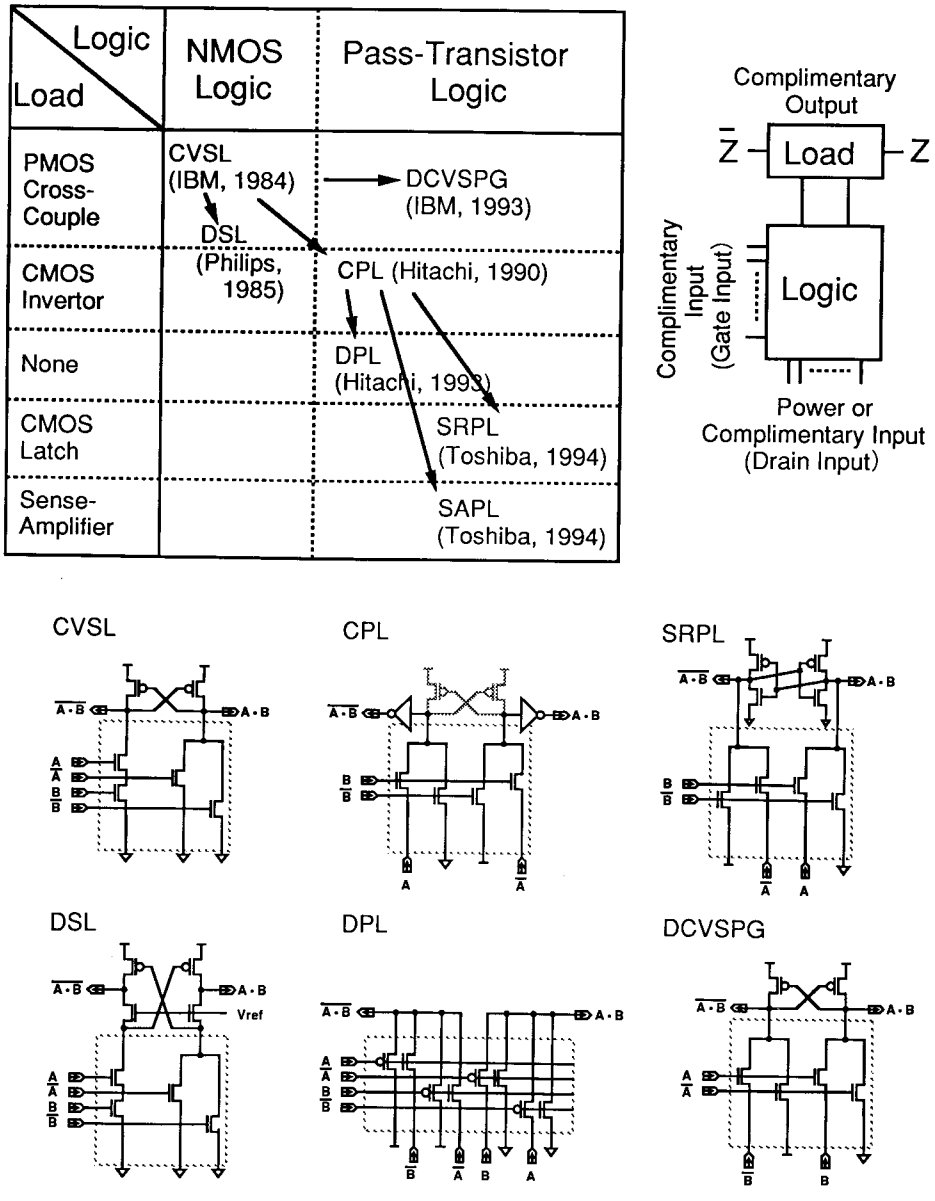

Fig. 9 Various pass-transistor logic structures.

Table 2 Simulated performance comparison of full adder in various pass-transistor structures.

3 μm Device (Full Adder)

Performance / Circuit	Tr. Number	Speed (ns)	Power (mW/25MHz)	P·D (normalized)	E·D (normalized)
CMOS	40	20	0.29	1.00	1.00
CVSL	22	22	0.61	2.31	2.55
DSL	26	14	0.48	1.15	0.80

0.4 μm Device (Full Adder)

Performance / Circuit	Tr. Number	Speed (ns)	Power (mW/100MHz)	P·D (normalized)	E·D (normalized)
CMOS	40	0.82	0.52	1.00	1.00
CPL	28	0.44	0.42	0.43	0.23
DPL	48	0.63	0.58	0.86	0.66
DCVSPG	24	0.53	0.30	0.37	0.24
SRPL	28	0.48	0.19	0.21	0.13

circuit diagrams are depicted in Fig. 9 together with an illustration which explains a history of their development. Their performance was studied in [16] and summarized in Table 2.

A Complementary Pass-transistor Logic (CPL) [13] uses nMOS pass-transistor circuits where "H" level drops by V_{thn}. CMOS inverters are provided in the output stage to compensate for the dropped signal level as well as to increase output drive capability. However, the lowered "H" level increases leak current in the CMOS inverters. So the cross-coupled pMOS loads can be added to recover the "H" level and enlarge operation margin of the CMOS inverters in low V_{DD}. In this case, the cross-coupled pMOS loads are used only for the level correction and don't require large drive capability. Therefore, small pMOS can be used in order not to degrade the switching speed.

A Differential Cascade Voltage Switch with the Pass-Gate (DCVSPG) [14] also uses nMOS pass-transistor logic with the cross-coupled pMOS load. A Double Pass-transistor Logic (DPL) [15] uses both nMOS and pMOS in the pass-transistor logic. No signal drop is taken place and therefore the circuit has big operation margin in low V_{DD}. However, since twice the number of transistors are used, the stray capacitance doesn't become small.

A Swing Restored Pass-transistor Logic (SRPL) [16] uses nMOS pass-transistor logic with a CMOS latch. Since the CMOS latch flips in a push-pull manner, it exhibits larger operation margin, less static current, and faster speed, compared to the cross-coupled pMOS loads. SRPL is suitable for circuits with light load capacitance. Figure 10 illustrates a full adder in SRPL. Figure 11 illustrates the full adder's delay dependence on the transistor sizes in the pass-transistor logic and the CMOS latch. The figure shows substantial design margin in SRPL which means that SRPL circuits are quite robust against process variations. As shown in Table 2, CPL is the fastest while SRPL is the most power saving. SRPL exhibits the smallest PD product and the smallest ED product in

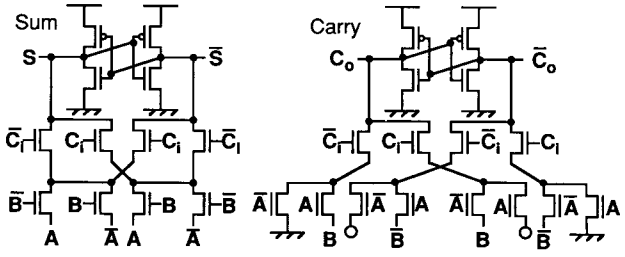

Fig. 10 Full adder circuit in SRPL.

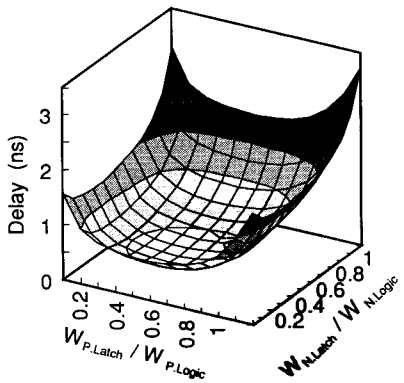

Fig. 11 Delay dependence on transistor width in SRPL.

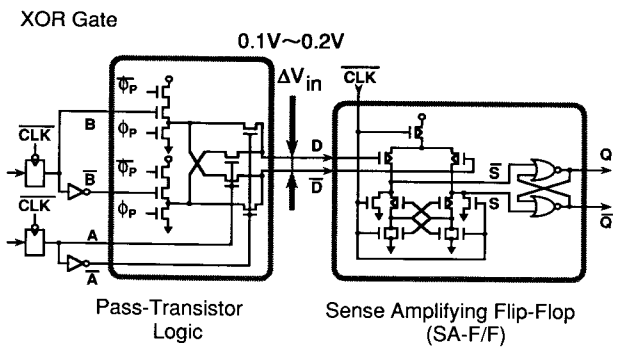

Fig. 12 SAPL.

this comparison. The push-pull action of the CMOS latch and the small stray capacitance bring this result.

A Sense-Amplifying Pass-transistor Logic (SAPL) [17] is a dynamic pass-transistor logic. In SAPL a reduced output signal of nMOS pass-transistor logic is amplified by a current latch sense-amplifier to gain speed and save power dissipation. Figure 12 depicts the circuit diagram. All the nodes in the pass-transistor logic are first discharged to the GND level and then evaluated by inputs. The pass-transistor logic generates complement outputs with small signals of around 100 mV just above the GND level. The small signals are sensed by the sense-amplifier in about 1.6 ns. Since the signal swings are small just above the GND level, the circuit runs very fast with small power dissipation, even when the load capacitance is large. SAPL therefore is suitable for circuits with large load

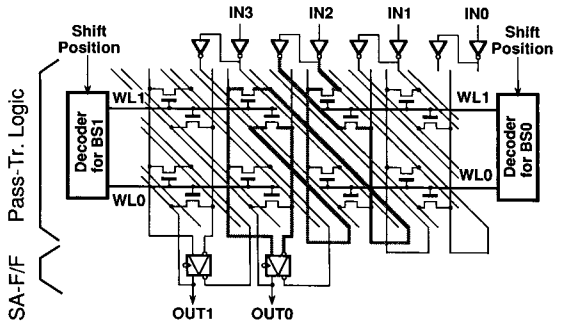

Fig. 13 4-to-2 barrel shifter in SAPL.

capacitance. By adding a cross-coupled NOR latch, the sensed data can be latched so that the SAPL circuit can be used as a pipeline register. An application example is a barrel shifter shown in Fig. 13 where multi-stage logic can be constructed just by concatenating the pass-transistors without inserting an amplification stage.

It should also be noted that test patterns can be generated automatically by using D-algorithm [18] for pass-transistor logic as well as for conventional CMOS static logic.

4. 2 Pass-Transistor Logic Synthesis

A synthesis method of pass-transistor network is described in [19]. It is based on Binary Decision Diagram (BDD) [20]. The synthesis begins by generating logic binary trees for separate logic functions which are then merged and reduced to a smaller graph. Lastly the graph is mapped to transistor circuits.

Let's consider a carry generation function in an adder. The function is expressed as $f = abc + a\bar{b}\,\bar{c} + \bar{a}\,b\,\bar{c} + \bar{a}\bar{b}c$. The logic binary trees are instantly generated as shown in Fig. 14 from a truth table of the function f. For example, the path from the source node (f) through edges "$\bar{c}$," "$\bar{b}$," and "a" to the sink node (1) corresponds to the case when $f=1$ with $c=b=0$ and $a=1$.

The trees can be reduced by applying in sequence two operations illustrated in Fig. 15 from the sink node. Operation 1 merges two nodes whose corresponding outgoing complement edges reach the same node. Operation 2 removes from the graph a node with two outgoing complement edges to the same node. In this particular example, a case where the second operation can be applied is not found. Figure 16 illustrates the reduction procedure of the logic binary trees in Fig. 15. The reduced graph is mapped to transistor circuits as shown in Fig. 17. All the edges are replaced with n-transistors whose gates are provided with the variables marked on the edges. The sink nodes (0) and (1) are replaced with V_{SS} and V_{DD}. If a edge "x" reaches the sink node (1) and the compliment edge "$\bar{x}$" reaches the sink node (0), "x" can be fed to the

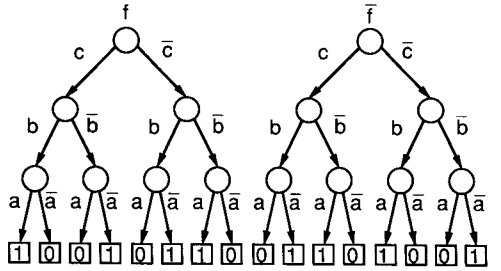

Fig. 14 Logic binary trees of function $f = abc + a\bar{b}\bar{c} + \bar{a}\,b\,\bar{c} + \bar{a}\bar{b}c$.

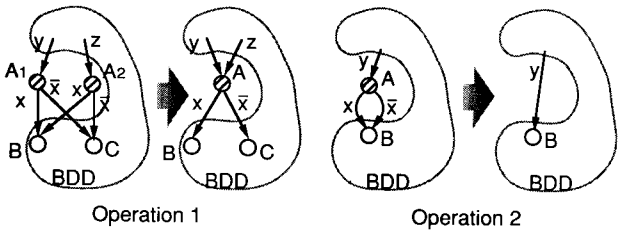

Fig. 15 Two operations to reduce logic binary trees.

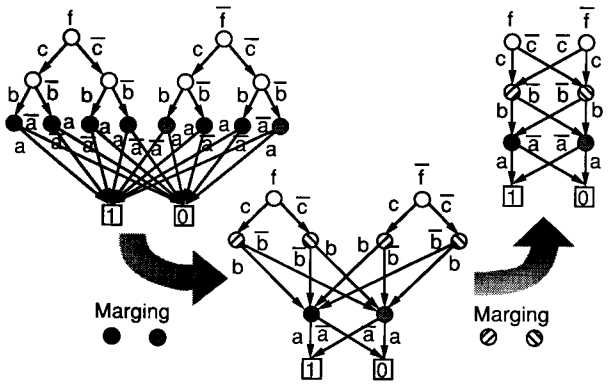

Fig. 16 Logic binary tree reduction.

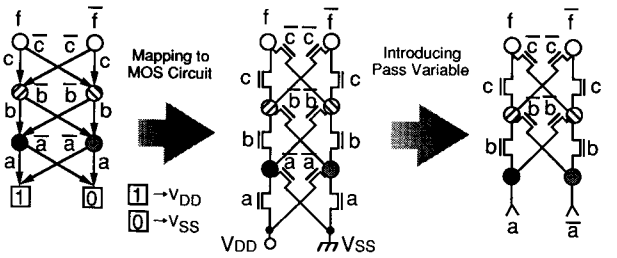

Fig. 17 Transistor mapping.

node as a pass variable. In this example two transistors are reduced by this rule. Lastly, appropriate buffer circuits should be connected to the output nodes (f) and ($\bar{f}$).

It is always guaranteed that a correct logic circuit can be synthesized in this method. Detail discussion can be found in [19].

Table 3 Low-power CMOS LSI circuit techniques.

	p_t	C_L	V_S	V_{DD}	f_{CLK}	I_{SC}	I_{DC}	I_{LEAK}
General		• device scaling	*Small Signal*	*Low V_{DD}* • DC-DC converter [22] • 0.25V QuadRail [23]		*Careful Design* • design verification by CAD		• control V_{th} fluctuation by SSB [8]
Clock	• gated clock	• floorplan to reduce wire length • F/F sizing *Charge Recycling* • C stacking [24]	• 1/2 swing [24]					
Bus	*Glitch Suppress* • 3-state-buffer activated after data fix [25]	• C stacking [26] • exclusive bus	• 1/2 swing [26]					
Data Path	• latch insertion to deskew data-in [27]	*Tr. Reduction* • pass-transistor (CPL [13], SRPL [16], SAPL [17], DPL [15], DCVSPG [14])	• pass-transistor (SAPL [17])		• parallelism [6]			
Random Logic	*CAD* • permutation of series-connected transistor order [28]	• library & CAD for pass-tr. logic [29] • tr. sizing [9][30]	• current switch logic (MCML [31])					*Sleep Mode* • 2 type V_{th} (MT-CMOS [32])
Memory		• hierarchy	• reduced swing WL, BL				*Cut Current* • latch S/A [33]	• switched-source-impedance [34]
I / O		• MCM [35] • area pad [35]	• reduced swing I/O (GTL [36], LVDS)		• phase modulation [37]		• dynamic termination [38]	

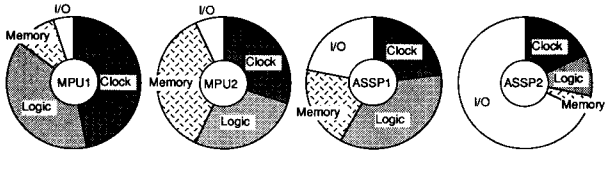

Fig. 18 Power use in logic CMOS LSIs.

5. Conclusions

The source of CMOS power dissipation was discussed in Sect. 2 and the parameters associated with the power dissipation were studied. Another concern is power use in a chip. Figure 18 shows some examples. Reflecting the versatility of logic CMOS LSIs, the power use is different from chip to chip. This suggests that all kinds of efforts in reducing the power parameters in every portion of LSI circuits should be paid to reduce the total power dissipation of a chip.

Many research efforts have been reported which are categorized in Table 3 by the power parameters and the power use. Brief explanations of the research achievements are given in [21]. Even though most of the research fields seem to have been explored, the low-power research has just come to the most interesting stage. In order to achieve power reduction by three figures, various techniques are required in each design domain from architectural level to algorithmic, logical, circuit, layout, and device levels. Wide spread of research activities will be expected involving many researchers working on system design, circuit design, CAD tools, and device design.

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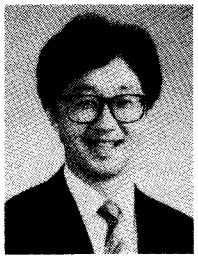

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