Editorial

THIS issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a selection of the best presentations at the 1996 Symposium on VLSI Circuits held at the Hilton Hawaiian Village in Honolulu, HI, USA, from June 13–15. In this issue you will find full-length papers describing the authors works in a more extensive format than possible in the Symposium Digest. These invited papers were subject to the normal JOURNAL review and referee process.

The Symposium on VLSI Circuits was founded in 1987 and is sponsored jointly by the Japan Society of Applied Physics and the IEEE Solid-State Circuits Council in cooperation with the Institute of Electronics, Information and Communications Engineers, Japan. The Symposium has been held in conjunction with the Symposium on VLSI Technology since 1988 and has attracted many papers presenting timely and important new developments in the field of VLSI and ULSI circuit design, from theoretical and novel circuits work to complete VLSI chips.

1996 marked the tenth year the VLSI Symposium had been held. To open the VLSI Symposium this year, we asked Dr. Minoru Nagata, the very first Symposium Technical Program Chairman, to recount the events that lead to the Symposium beginning. We have included a copy of his speech describing the VLSI Symposium's beginnings after this editorial.

This year's Symposium Program committee reviewed a record of 232 papers submitted from 24 countries around the world. The committee selected 72 papers to be presented along with four invited papers. From these presentations, and based in part on session ratings, we have selected 17 papers to include in this special issue of the JOURNAL. They are loosely grouped into four categories: memory, high speed I/O, analog, and RF communications.

In the memory circuits area we have seven papers. The first is one of the Symposium's invited papers. Itoh *et al*. investigate the topic of the limitations and challenges in designing multigigabit DRAM chips in terms of density, performance, and low-power/low-voltage. This is followed by a paper by Watanabe *et al*. describing a modular DRAM architecture for integrated DRAM and logic chips where data transfer rates of 6 to 12 Gbyte/s are achievable. An 8-Mb DRAM and four pixel processors were implemented in a CMOS DRAM process with 0.4-μm design rule. The third paper is our last DRAM paper, and it describes two low-voltage, high-speed circuit design techniques by Lee *et al*. for the gigabit DRAM's. An experimental 16-Mb DRAM using a 0.18-μm CMOS process achieved an access time for RAS (tRAC) of 28 ns at $V_{cc} = 1.5$ V and $T = 25°$C.

Next we have two memory papers focusing on the area of nonvolatile ferroelectric technology. A one-transistor and one-capacitor per bit ferroelectric cell architecture is described by Hirano *et al*. with which an access time of 100 ns is achieved at 2.0 V. Also trying to achieve high-speed and low-power ferroelectric nonvolatile memories, Fujisawa *et al*. describe a charge-share modified precharge-level architecture for selective subdataline activation. These techniques and circuits are evaluated for a simulated 16-Mb ferroelectric memory reducing access time by 20 ns to 51 ns compared with a conventional architecture.

Finishing out the memory papers we have two Flash memory design papers. A compact on-chip error correcting circuit for low cost Flash memories is described by Tanzawa *et al*. The error correcting circuit requires only 2% additional chip area, including all associated cells, sense amplifiers, logic, and interconnect lines. A 120-mm^2 64-Mb NAND Flash memory achieving 180 ns/Byte effective programming speed and 40 MByte/s read throughput is described by Kim *et al*. The chip was fabricated using a 0.4-μm single-metal CMOS flash process resulting in an effective cell size of 1.1 μm^2.

In the area of high speed I/O we have two papers. The first by Sidiropoulos *et al*. describes how current integrating receivers with a 1 V signal swing can realize a 740 Mb/s/pin CMOS signaling interface in a 0.8-μm CMOS technology with a bit error rate less than 10^{-14}. This circuit utilizes a delay-locked loop (DLL) for data sampling clock signal generation. The second paper in this area is by Kim *et al*. and describes a 960 Mb/s/pin interface which eliminates setup and hold time margins by using 3X oversampling and data recovery. Two experimental chips with a 4-pin interface were fabricated in a 0.6-μm CMOS technology.

In the area of analog we have two papers. First Redman-White describes a new rail-to-rail CMOS input architecture that implements an input stage with transconductance and slew-rate that are both nearly independent of input common-mode voltage level. The circuit operation is applicable even in deep submicron technology. The second analog paper describes a mixed-signal RAM decision-feedback equalizer for disk drives by Rothenberg *et al*. In the analog domain, this circuit subtracts intersymbol interference caused by the past four outputs based upon an error look-up table stored in a RAM. The equalizer operates at 90 Mb/s in a 1.0-μm CMOS process using a 5.0 V supply voltage.

Indicating the high level of circuit activity in the area of RF communications, six papers have been selected describing various RF circuit components. Chang *et al*. first describe a highly selective CMOS linear switched-capacitor channel-select filter for a direct-conversion wireless receiver. This receiver, when fabricated in a 1.0-μm CMOS process, operates in the 902–928 MHz band in which

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the filter selects a 230-kHz wide channel while providing attenuation by more than 50 dB from 320 kHz to 57 MHz.

The next paper by Razavi decribes the design of a 2-GHz, 1.6-mW phase-locked loop fabricated in an 18-GHz, 0.6-μm BiCMOS process. The circuit employs cross-coupled delay elements and inductive peaking to merge the oscillator and the mixer into one stage to reduce power dissipation. The third RF communications paper is a completely integrated 1.8-GHz low phase-noise CMOS voltage controlled oscillator by Craninckx and Steyaert. The authors implemented this circuit using optimized hollow spiral inductors with only two metal layers in a standard silicon digital CMOS process. In the fourth RF communications paper, Shaeffer and Lee present a 1.5-V, 1.5-GHz CMOS low noise amplifier implemented in a standard 0.6-μm CMOS process, and it is intended for use in a global positioning system. In addition to the low noise amplifier architecture, the effects of induced gate noise in MOSFET devices are discussed in the paper.

The fifth RF communications paper is by Lee *et al*. who present a fully integrated low noise 1-GHz frequency synthesizer design for mobile communications applications. The PLL-based frequency synthesizer realized in a 0.8-μm CMOS process has a center frequency of 800 MHz and tuning range of $\pm$25%, with $-$80 dBc/Hz phase noise at a 100 kHz carrier offset. The last of our papers in this special issue is an RF communications paper by Nakagawa and Nosaka. They describe a direct digital synthesizer without a ROM that still produces square waves with low spurious signals. This is achieved through the use of analog circuits and interpolation of the analog-converted accumulator contents with timing extracted from the interpolated signal.

This special issue required a great amount of effort from both the authors and reviewers. We would like to give them all our thanks in appreciation of their effort. Special thanks are due to the Symposium Chairman, K. J. O'Connor, and Co-Chairman T. Masuhara, and all the members of the Technical Program Committee of the Symposium on VLSI Circuits for making it a success. We also appreciate the IEEE Transactions and Journals staff, especially Ms. R. Shaw and Ms. L. Tucker, for their outstanding effort to publish this issue.

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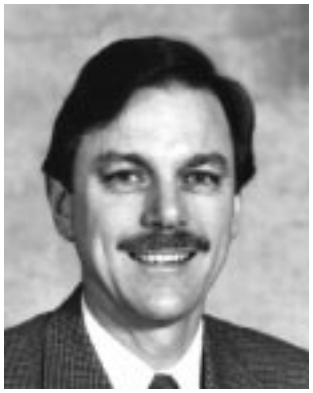

Ian Young (S'73–M'78) was born in Melbourne, Australia. He received the B.E. and M. Eng. Sci. degrees in electrical engineering from the University of Melbourne in 1972 and 1975, respectively. He received the Ph.D degree in electrical engineering from the University of California, Berkeley, in 1978.

He was a consultant to American Microsystems, Inc. from 1976 to 1978, developing switched-capacitor circuits for telecommunications. He taught the Analog Integrated Circuit Design course at the EECS Department of the University of California, Berkeley, in 1977. From 1978 to 1981 he worked for Mostek Corporation, designing MOS integrated circuits for telecommunications' applications. From 1981 to 1983 he worked as an Industrial Consultant designing analog/digital MOS integrated circuits. In 1983 he joined the Portland Technology Development group at Intel Corporation in Hillsboro, OR, where he is currently an Intel Fellow and Director of Advanced Circuit and Technology Integration. He is responsible for defining and developing future circuit directions and optimizing the manufacturing process technology for high-performance microprocessor products. At Intel he has been involved with the development of DRAM's and high-speed SRAM's, CMOS and BiCMOS digital circuit design techniques for microprocessors, phase-locked loop clock generation and distribution for microprocessors, interconnect capacitance and device modeling, and also analysis of circuit design considerations in the development of process technology for five generations (1.0 μm through 0.25 μm) of advanced microprocessors. He holds 20 patents.

Dr. Young has received three Intel Achievement Awards; in 1990 for phase-locked loop clock generator design, in 1992 for defining and implementing BiCMOS process technology and BiCMOS logic circuit techniques, and in 1996 for development of the high performance transistors for the 0.25-μm technology. In 1994 he served on the Semiconductor Industry Association 1995–2010 National Roadmap Defining Technical Working Group. In 1994 he also served also on the first Sematech TCAD project planning committee. In each of these activities he represented circuit design and interconnect issues. He has been a member of the Program Committee for the Symposium on VLSI Circuits since 1991. During 1995 and 1996 he was Co-Chairman and Chairman of this Symposium's Program Committee, and in 1997 he is the Symposium's Co-Chairman. Since 1992 he has been a member of the International Solid-State Circuits Conference Program Committee, serving as the Digital Subcommittee Chairman since 1996. He has been a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS for the December 1994, April 1996, and April 1997 special issues.

Takayasu Sakurai (S'77–M'78) received the B.S., M.S., and Ph.D. degrees in electronic engineering from University of Tokyo, Tokyo, Japan, in 1976, 1978, and 1981, respectively.

In 1981 he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Japan, where he was engaged in the research and development of CMOS dynamic RAM and 64 Kb, 256 Kb SRAM, 1 Mb virtual SRAM, cache memories, and BiCMOS ASIC's. During the development, he also worked on the modeling of interconnect capacitance and delay, new memory architectures, hot-carrier resistant circuits, arbiter optimization, gate-level delay modeling, alpha/nth power MOS model and transistor network synthesis. From 1988 through 1990, he was a Visiting Scholar at University of California, Berkeley, doing research in the field of VLSI CAD. From 1990, back in Toshiba, he managed multimedia LSI development including media processors and video compression/decompression LSI's. Since 1996, he has been a Professor at the Institute of Industrial Science, University of Tokyo, working on low-power and high-performance LSI designs.

Dr. Sakurai is and has been serving as a program committee member for CICC, DAC, ICCAD, ICVC, ISPLED, ASP-DAC, TAU, CSW, VLSI, and FPGA Workshop. He is a technical committee chairperson for the VLSI Circuits Symposium. He is a member of the IEICEJ and the Japan Society of Applied Physics.