Foreword

THIS issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a selection of the best presentations at the 1997 Symposium on VLSI Circuits held at the Rhiga Royal Hotel in Kyoto, Japan, from June 13–15. This issue contains full-length papers describing the authors' works in a more extensive format than possible in the *Symposium Digest*. These papers were selected from all the offerings at the symposium and were subject to the normal journal reviews and referee processes. This issue is a joint publication with the *IEICE Transactions on Electronics*.

The symposium was founded in 1987 and is sponsored jointly with the Japan Society of Applied Physics and the IEEE Solid-State Circuits Council, in cooperation with the Institute of Electronics, Information and Communications Engineers, Japan. The symposium has been held in conjunction with the Symposium on VLSI Technology since 1988 and has attracted many papers presenting timely and important new developments in the field of transistor-level VLSI circuit design, from theoretical work to complete VLSI chips.

In the high-performance logic circuit area, we have included two microprocessor papers. The first was an invited talk at the symposium and chronicles the design history of a family of high-performance microprocessors. The second paper describes the logic and circuits, comprising 141 000 transistors, used to implement a 20-entry instruction queue which scoreboards 80 registers and issues four instructions per cycle at 600 MHz.

In the low-power arena, we selected a total of six papers. These include a video signal processing A/D with a low-power consumption of 4.3 μW per MS/s per comparator and ±4 mV differential nonlinearity by canceling threshold voltage fluctuation. A second paper describes a complimentary metal–oxide-semiconductor (CMOS) adiabatic circuit block together with a four-phase clock generator fabricated and measured to show a factor of 3.5 improvement in power over the conventional circuit. Two other papers describe a flip-flop which accommodates a small swing clock to considerably reduce system power and another low-power flip-flop scheme based on the data dependent operation of a D flip-flop, fabricated using 0.25 μm SOI CMOS. For use in the medical field, the fifth paper reports on a variable rate sigma–delta analog-to-digital converter (ADC) capable of measuring charge pulses down to 360 electrons at 100 000 events/s. The low-power area is rounded out by a demonstration of the feasibility of operating a 500 kHz digital system from power generated by vibrations in its environment.

The wireless area continues to make great strides, and we have included four papers in this area. One paper describes integrated inductors utilizing a patterned ground shield to increase the quality factor by 25% and reduce substrate coupling. There is a demodulator using analog-sampled data signal processing to achieve a 128 MS/s processing rate and a 54 dB input dynamic range consuming 75 mW. A third paper describes a low-voltage bipolar mixer suitable for portable wireless systems based on two-cell battery operation. A final paper reports on a second-order integrated LC band-pass delta–sigma modulator employing active Q enhancement to achieve a signal-to-noise ratio of 56 dB over a 200 kHz bandwidth at 950 MHz.

We selected two papers on high speed chip-to-chip interconnections. The first covers 4 Gb/s serial links using a 0.5 μm MOSIS process, which demonstrated a bit error rate of $<10^{-14}$ with a 3.3 V supply. The second paper describes skew-insensitive data recovery up to 1.04 Gbd using a digital phase-locked loop and small swing signals applicable to an XGA flat panel system.

In the memory area, we selected five papers. Two SDRAM papers describe a 7 ns 1 Gb, 570 mm^2 SDRAM using 0.16 μm CMOS and techniques to achieve a 200 MHz $\times$ 32 b synchronous DRAM which enables a 1.6 GB/s data rate operation. A third paper describes the out-of-order execution of the DRAM accesses to provide high data throughput for random access of embedded DRAM. Compensating Vth mismatch with a charge transfer sense amplifier is described in another paper. This reduces power dissipation of a 2 k $\times$ 16 b SRAM to 5 mW at 1 V and 50 MHz. A paper on ferroelectric RAM reports a 37% chip area reduction by serially connecting the MOSFET's and ferroelectric capacitors.

WILLIAM BIDERMANN, *Guest Editor*
Chromatic Research, Inc.
Sunnyvale, CA 94089 USA

TAKAYASU SAKURAI, *Guest Editor*
Institute of Industrial Science
University of Tokyo
Tokyo, Japan

William Bidermann (M'89) received the B.S. and M.S. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 1978. As part of his research, he worked jointly with Texas Instruments on low-power CCD's.

From 1978 to 1981, he was with Hewlett Packard, Palo Alto, CA, developing 16 and 64 k DRAM's, MNOS, and floating-gate EEPROM's. From 1981 to 1984, he was a Consultant for Digital Equipment Corporation, VLSI Technology, RCA, and Lockheed Missile and Space Division. He worked from 1984 until 1994 as a Group Hardware Engineering Manager responsible for the Advanced Development Group at Digital's Hudson, MA, facility, where he was responsible for embedded memory design, low-temperature CMOS technology, and the first Alpha development. In 1994, he became Vice President of Engineering at HaL Computer Systems, Campbell, CA, and developed the first SPARC V9 microprocessor. Currently, he is the Vice President of Advanced Development for Chromatic Research, Sunnyvale, CA, developing next-generation media processors.

Mr. Bidermann holds two patents. He has been a member of the Program Committee for the VLSI Symposium on Circuits and the International Solid State Circuits Conference. He is currently the Chairman of the Technical Program Committee for the Symposium on VLSI Circuits.

Takayasu Sakurai (S'77–M'78) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1976, 1978, and 1981, respectively. His Ph.D. work was on electronic structures of the Si–SiO$_2$ interface.

In 1981, he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Japan, where he was engaged in the research and development of CMOS dynamic RAM and 64 kb, 256 kb SRAM, 1 Mb virtual SRAM, cache memories, and BiCMOS ASIC's. During this time, he also worked on the modeling of interconnect capacitance and delay, new memory architectures, hot-carrier resistant circuits, arbiter optimization, gate-level delay modeling, alpha/nth power MOS models, and transistor network synthesis. Among them, the 2-D capacitance model and alpha power law MOSFET model are widely used in timing designs. From 1988 through 1990, he was a Visiting Scholar at the University of California, Berkeley, doing research in the field of VLSI CAD. From 1990, again at Toshiba, he managed multimedia LSI development including media processors and video compression/decompression LSI's. Since 1996, he has been a Professor at the Institute of Industrial Science, University of Tokyo, working on low-power and high-performance LSI designs.

Dr. Sakurai has served and currently is serving as a program committee member for the CICC, DAC, ICCAD, ICVC, ISPLED, ASP-DAC, TAU, CSW, VLSI design, and the FPGA Workshop. He is a Technical Committee Chairperson for the VLSI Circuits Symposium and is a member of the Institute of Electronics Information and Communication Engineers of Japan and the Japan Society of Applied Physics.