Integrated Current Sensing Device for Micro IDDQ Test

Kouichi Nose and Takayasu Sakurai
Institute of Industrial Science, University of Tokyo, Tokyo, Japan
7-22-1 Roppongi, Minato-ku, Tokyo, 106-8558 Japan
nose@iis.u-tokyo.ac.jp

Abstract

A current sensing device, namely Hall Effect MOSFET (HEMOS) is proposed. It is experimentally shown that the HEMOS enables a non-contacting, and non-disturbing current measurement, which can be used for IDDQ testing of internal circuit blocks. The HEMOS can be manufactured and integrated in a VLSI with the conventional CMOS process. The HEMOS is also helpful to establish the low standby current by identifying the locations of large standby power consumption (possibly a design fault) using only a few pads.

1. Introduction

Recently, the number of transistors in VLSI's is increasing rapidly, which makes it difficult to find out the locations of design errors and/or the locations of small margins in VLSI's. In order to pin-point these problematic locations, it is effective if the location of an abnormal current path can be identified. The IDDQ test tries to measure the abnormal current by measuring the power supply line current in a stand-by mode. In the conventional IDDQ test, however, these locations of problems can not be identified, since only the current of several power supply line systems that are separated internally and have separate external pins can be checked. Because each power supply line connects to too many transistors, it is just impossible to nail down the error locations. It is possible to identify the location of error if the current of thousands of internal power supply lines can be checked.

In this paper, a current sensing device, namely Hall Effect MOSFET (HEMOS), which consists of twin-drain MOSFET is proposed to achieve this goal. The HEMOS enables a non-contacting, and non-disturbing current measurement by using the Hall effect. It is shown for the first time that the current density of the order of 50μA/μm can be measured using the proposed HEMOS. This is sufficient to pick up the abnormal standby current. By introducing the HEMOS, it is possible to check the quiescent current of thousands of macros on a chip, which we call a micro IDDQ test.

One more feature that is necessary in recent VLSI's is to achieve low standby power. The proposed HEMOS also helps establish the low standby current by identifying the locations of large standby power consumption.

2. The structure of HEMOS

2.1 Basic concept of HEMOS

Figure 1 shows the structure of the HEMOS. A power supply line for a circuit block under test is placed on top of the HEMOS. When an abnormally high leakage current flows through the power supply line, a magnetic field, B, is generated around the line. The relation between B and I_P is shown as

$$\mu I_P = \oint \boldsymbol{B} d\boldsymbol{s} \cong B(2W_P + 2T), \qquad (1)$$

where W_P is width of a power supply line and T is the space between a power supply line and an channel of the HEMOS. This equation shows that the magnetic field is in proportion to the current of the power supply line, I_P, and inversely proportion to W_P if W_P is much larger than T. Then, electrons which flow in the channel of the HEMOS are deflected by the vertical element of the magnetic field through the Hall effect. The number of electrons which flow into the Drain1 in Fig.1 is different from the number of electrons which reaches the Drain2.

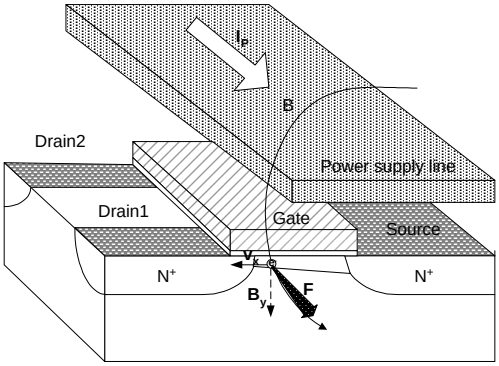

Figure 1. The structure of HEMOS

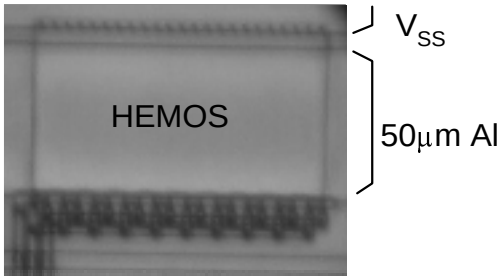

Figure 3. Microphotograph of HEMOS

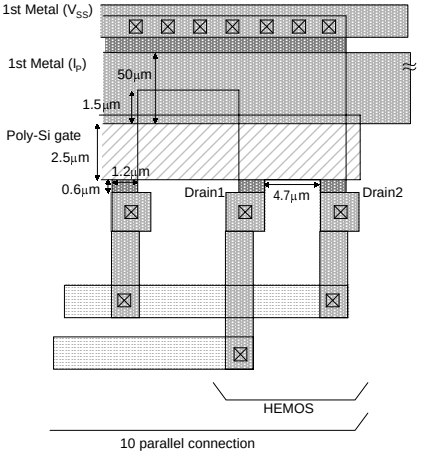

Figure 2. Layout of HEMOS

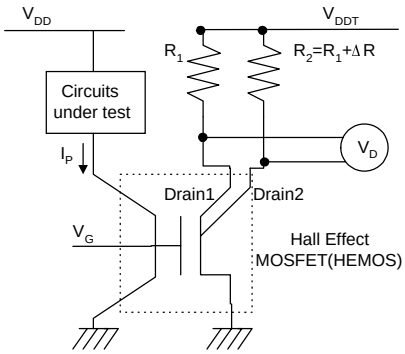

Figure 4. Test circuit to measure the current of power supply line using HEMOS

2.2 HEMOS design

Figure 2 shows the layout of HEMOS. In this study, the HEMOS has ten parallel connections in order to suppress the variation of transistors and to obtain as large current as possible. The channel length of HEMOS is designed as long as possible in order to intensify the Hall effect. In this study, the width of the power supply line is chosen to be 50μm($=W_P>>T$).

Figure 3 shows a microphotograph of a fabricated HEMOS using the conventional 0.5μm double metal CMOS technology, which is used to conduct measurements in this paper.

Figure 4 shows a test circuit to measure the difference between the Drain1 current and Drain2 current. The circuit consists of the HEMOS and two external resistors in order to convert the current difference into voltage. These resistors are not identical with each other. Therefore The difference between R_1 and R_2, denoted as ΔR, is taken into account.

The voltage difference between Drain 1 and Drain2, V_D, can be measured more accurately than the output current difference between I_1 and I_2. V_D is calculated as

$$V_D = I\Delta R + R_1(\Delta I_2 - \Delta I_1) + \Delta R\Delta I_2 , \qquad (2)$$

where

$$I_1 = I + \Delta I_1 , \quad I_2 = I + \Delta I_2 , \quad \Delta R = R_2 - R_1 ,$$

where I is the drain1 and drain2 current when I_P=0. In this expression, the term, $I\Delta R$, corresponds to V_D when I_P=0 ($V_D(I_P=0)$).

Now, let's introduce a quantity, ΔV_D, which signifies the increment of V_D from when I_P is not zero. In the measurement, a resistor whose relative error is less than 1% can be easily employed (in other words, $\Delta R/R_1 < 0.01$). Then, ΔV_D can be appropriated as

$$\Delta V_D \cong R_1(\Delta I_2 - \Delta I_1) \qquad (3)$$

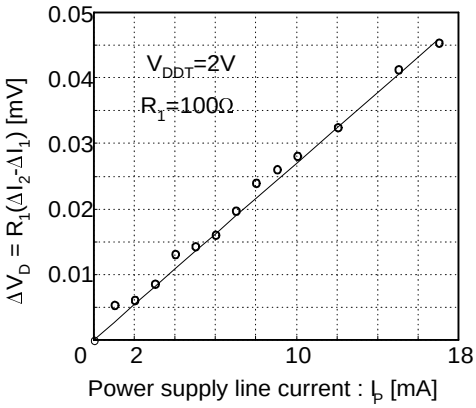

Figure 5. Measured results for ΔV_D dependence on the current under test, I_P.

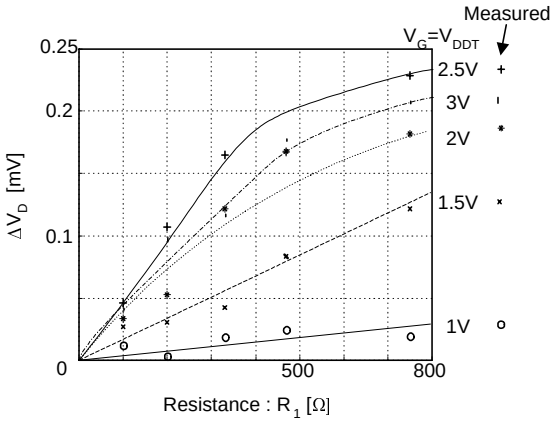

Figure 6. Measured results for ΔV_D dependence on R

From eq.(3), ΔV_D is proportional to the difference between I_1 and I_2.

3. Measurement results

Figure 5 shows that the measured results of ΔV_D dependence on the power supply line current, I_P. It is clearly shown that ΔV_D is proportional to the current of the power supply lines, I_P, and it is possible to measure I_P in a non-contacting and non-disturbing way. In this paper, the width of the power supply line is 50μm. When the width is narrower than 50μm, ΔV_D is larger than this in an inversely proportional way (see Fig.1). It is also confirmed that ΔV_D degreases proportionally when I_P is lower than zero.

Figures 6 and 7 are measured ΔV_D dependence on the resistance of an external resistor, R, and the testing voltage, V_{DDT}, respectively. In this paper, the current of power supply line, I_P, is chosen to be 10mA. It is seen that there is a good bias point that makes ΔV_D the largest to improve the sensitivity of the IDDQ measurement. It is suggested that ΔV_D is proportional to an external resistance when we see Eq.(3), in the measurement ΔV_D is not proportional to R_1 when V_G and R_1 are large (V_G>2V and R>500Ω). The reason for this is considered that HEMOS is affected by the voltage degradation of the external resistance. The drain current of HEMOS flows mA order when gate voltage is larger than 2V. In this condition, the voltage degradation of external resistance is 100mV order. Hence, the voltage degradation can not ignored when R is large. From this effect, when an internal resister instead of external resister, like a gate-drain tied MOSFET, it is necessary to take care of the voltage degradation of the resister.

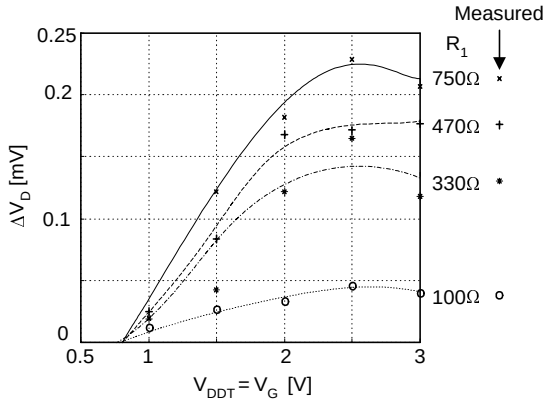

Figure 7. Measured result of ΔV_D dependence on V_{DDT}.

4. Micro IDDQ test circuit using HEMOS

Next, a way to implement the micro IDDQ test in a VLSI chip should be discussed. A difficult part is that only a few pads are allowed for a testing purpose, since a pad, a pin and bonding area are precious and expensive. Fortunately, it is possible to share pads among thousands of HEMOS's, since the off current of the HEMOS whose gate is biased low is measured to be much smaller by the order of 10^6 than the on current of the HEMOS whose gate is biased high. Now, there are a couple of approaches to measure the thousands of power supply current using the HEMOS by sharing pads. One of the solutions is depicted in Fig.8. By using shift registers, only one of the HEMOS's is turned on by applying '1' to the gate of the HEMOS,

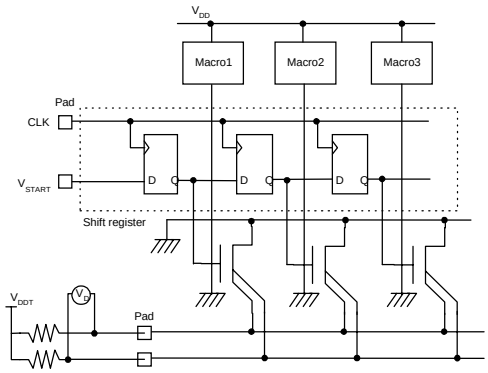

Figure 8. Circuit diagram for the micro IDDQ test by sharing pads among HEMOS's

while other HEMOS's are kept off by applying '0' to the gates.

From the standboint of the variation in each chip, this micro IDDQ structure using the HEMOS is effective. First, it prepares the reference HEMOS which can flow I_P directly. Then, it measures the characteristics like fig.1 using this reference HEMOS. From this characteristic, it is able to measure I_P of each macro considering the variation of the chip.

5. Conclusion

In conclusion, it is experimentally shown that the proposed HEMOS with the power supply line on top of it is a promising candidate for conducting an IDDQ test on thousands of small circuit blocks on a chip to pick up an abnormal leakage current and hence to identify the point of design errors and small margins. The HEMOS can be manufactured and integrated in a VLSI with the conventional CMOS process.

Acknowledgement

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by NTT Electronics Corporation and Dai Nippon Printing Corporation.

The work has been supported by a grant from Toshiba Corporation.