LSI design toward 2010 and low-power technology

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Biography

Takayasu Sakurai received the B.S., M.S. and Ph.D degrees in EE from University of Tokyo, Japan, in 1976, 1978, and 1981, respectively. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM and BiCMOS ASIC's. He also worked on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at Univ. of Calif., Berkeley, doing research in the field of VLSI CAD. From 1990 back in Toshiba, he managed RISCs, media processors and MPEG2 LSI designs. From 1996, he is a professor at the Institute of Industrial Science, University of Tokyo, working on low-power and high-performance system LSI designs. Prof. Sakurai served as a conference chair for Symposium on VLSI Cirucits, a vice chair for ASPDAC and a program committee member for ISSCC, CICC, DAC, ICCAD, FPGA workshop, ISLPED, TAU, and other international conferences. He is also consulting to US startup companies.

Summary:

If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI's of the year 2010: namely power crisis, interconnection crisis, and complexity crisis.

As for power crisis, there are activities to lower the power consumption from device level, circuit level to system level. Lowering supply voltage (V_{DD}) is very effective in reducing the power but the threshold voltage (V_{TH}) should be reduced at the same time for high-speed operation. The low V_{TH}, however, increases the leakage current. To overcome this situation, V_{TH} and V_{DD} control through the use of multiple V_{TH}, variable V_{TH}, multiple V_{DD} and variable V_{DD} are intensively pursued and some have been productized. At the system level, a system LSI approach is promising for realizing low power. The new trend is to exploit cooperation of software and hardware. In the sub 1-volt design, watch out for the abnormal temperature dependence of drain current.

The interconnection will be determining cost, delay, power, reliability and turn-around time of the future LSI's rather than MOSFET's. RC delay problem can be solved through LSI architecture realizing "the further, the less communication" with the help of local memories.

It is just impossible to design LSI's with 100 million transistors from scratch. The complexity issue can only be solved by the sharing and re-use of design data. So-called IP-based design will be preferable. The virtual components are put together on a silicon to build billion transistor LSI's, which can be compared to the present system implementation with pre-manufactured LSI components.

In the year 2012, sensors / actutors can be integrated on a chip with 0.06μm 2G Si FET's with V_{TH} & V_{DD} control. Globally asynchronous LSI's with locally synchronous 10GHz clock will be implemented.

LSI Design Toward 2010 and Low-Power Technology

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1 Scaling and three crises
2 Power crisis
3 Interconnection crisis
4 Complexity crisis

Fig.1 Title

Scaling Law

Transistor		Numbers are exponent to k (k^n)
Voltage	[V]	-1
Tr. size	[x]	-1
Oxide thickness	[t]	-1
Current	[I~V$^{1.3}$/t]	- 0.3
Tr. capacitance	[Cg~x^2/t]	-1
Tr. delay	[Tτ~CεV/I]	-1.7
Tr. power	**[Pg~CgV^2/Tg]**	**-1.3**
Tr. power density	**[p~Pg/x^2]**	**0.7**
Tr. desity	**[n~ 1/x^2]**	**2**

Interconnection		Local	Middle	Global	VDD/VSS
Length	[L]	-1	- 0.5	0	0
Width	[W]	-1	- 0.5	0	1
Thickness	[T]	-1	- 0.5	0	1
Height	[H]	-1	- 0.5	0	0
Resistance	[Rm~LW/T]	1	0.5	0	-1
Capacitance	[Cm~LW/H]	-1	- 0.5	0	1
Delay/T. delay	**[Tm~RmCm/Tg]**	**1.85**	**1.85**	**1.85**	**-**
Current density	**[J~pLW/V/W/T]**	**-**	**-**	**-**	**0.85**
Dc Noise	**[SN dc~JWLR m/V]**	**-**	**-**	**-**	**1.35**

K=2

$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{T}{L}\right)\frac{(V_{gs}-V_t)^{\alpha}}{2} \sim [V^{\alpha}/t]$$

$\alpha = 1.3$

T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no,2, pp.584-594, Apr. 1990.

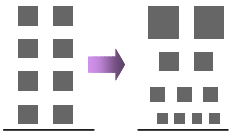

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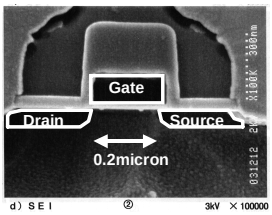
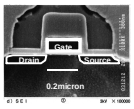
Fig.2 Scaling law

Scaling Law



Size 1/2



Favorable effects	
Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x2
Cost	x1/4

Unfavorable effects	
Power	x1.6
RC delay	x3.6
Current density	x1.8
Voltage noise	x2.5
Design complexity	x4

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Fig. 4 Scaling law

Three crises in VLSI designs

- **Power crisis**
- **Interconnection crisis**
- **Complexity crisis**

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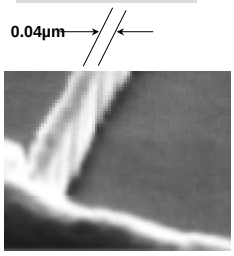
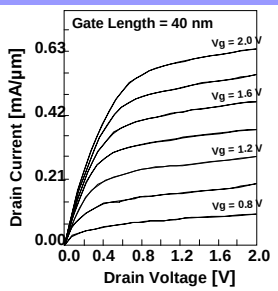
Fig.5 Three crises in VLSI designs

Limit of Miniturization

0.04μm MOSFET





Conventional I-V curve at 0.04μm (Even down to 0.014μm)

M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50nm gate Length N-MOSFETs with 10 nm Phosphorus Source and Drain Junctions", IEDM Technical Digest, pp. 119 - 122, 1993.
H. Kawaura, T. Sakamoto, Y. Ochiai, J. Fujita, and T. Baba, "Fabrication and Characterization of 14-nm-Gate-Length EJ-MOSFETs", Extended Abstracts of SSDM, pp.572-573, 1997.

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Fig.3 Limit of miniturization

Ever Increasing VLSI Power

(Power consumption of processors published in ISSCC)

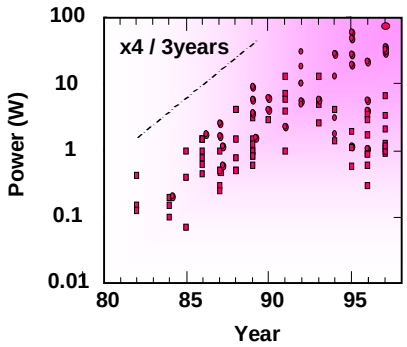

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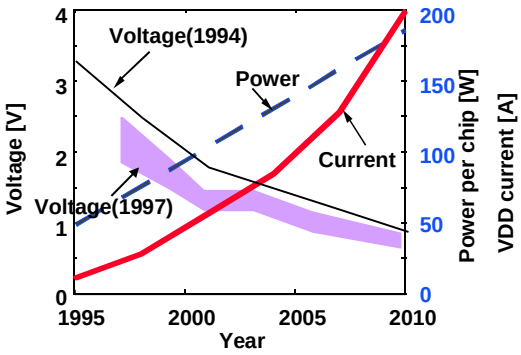
Fig.6 Ever incresing VLSI power

VDD, Power and Current Trend



Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

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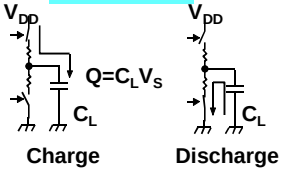
Fig.7 VDD, power and current trend

Expression for CMOS Power

$P = \alpha \cdot C_L \cdot V_S \cdot V_{DD} \cdot f_{CLK}$ Charging & discharging
$+ \alpha \cdot I_{SC} \cdot \Delta t_{SC} \cdot V_{DD} \cdot f_{CLK}$ Crowbar current
$+ I_{DC} \cdot V_{DD}$ Static current
$+ I_{LEAK} \cdot V_{DD}$ Subthreshold leak current



Charge Discharge

$C_L \cdot V_S$ amount of charge loses V_{DD} of potential
-> $C_L \cdot V_{DD} \cdot V_S$ energy consumption per cycle

α : Switching probability
C_L : Load capacitance
V_S : Signal swing
V_{DD} : Supply voltage
I_{SC} : Mean crowbar current
Δt_{SC} : Crowbar current duration
f_{CLK} : Clock frequency
I_{DC} : DC current
I_{LEAK} : Subthreshold leak current

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Fig.10 Expression for CMOS power

Necessity for Low-Power Design

Power range	Concerns	Typical applications (All need high-perf.)
< 0.1W	· Battery life	Portable · PDA · Communications
~ 1W	· Inexpensive package limit · System heat (10W / box)	Consumer · Set-Top-Box · Audio-Visual
> 10W	· Ceramic package limit · IR drop of power lines	Processor · High-end MPU's · Multimedia DSP's

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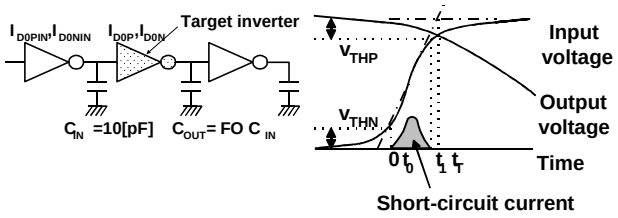
Fig.8 Necessity of low-power design

Voltage waveform of CMOS inverter



$$C_{OUT}\frac{dV_{OUT}}{dt} \cong -I_{DN} = -I_{DON}\left(\frac{V_{GSN}-V_{THN}}{V_{DD}-V_{THN}}\right)^{\alpha_N}$$

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Fig.11 Voltage waveform of CMOS inverter

What sets the technology trend?

- NMOS ⇒ CMOS
  Cost up
- Bipolar ⇒ CMOS
  Speed down
- **Not cost nor speed but power set the technology trend.**
- **Integration can achieve low cost and high speed as a system.**

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Fig.9 What sets the technology trend?

Short-circuit power dissipation formula

$$P_S = \frac{k(v_{D0P})\, fo_P^2 C_{IN} V_{DD}^{\ 2}}{\frac{v_{D0P} g(v_T,\alpha)}{2k(v_{D0P})} FO\beta_r + h(v_T,\alpha)\, fo_P}$$

$$g(v_T,\alpha) = \frac{\alpha_N+1}{f(\alpha)} \frac{(1-v_{TN})^{\alpha_N}(1-v_{TP})^{\alpha_P/2}}{(1-v_{TN}-v_{TP})^{\alpha_P/2+\alpha_N+2}}$$

$$h(v_T,\alpha) = 2^{\alpha_P}(\alpha_P+1)\frac{(1-v_{TP})^{\alpha_P}}{(1-v_{TN}-v_{TP})^{\alpha_P+1}}$$

$$k(v_{D0P}) = \frac{0.9}{0.8} + \frac{v_{D0P}}{0.8}\ln\frac{10 v_{D0P}}{e}$$

$$FO = \frac{C_{OUT}}{C_{IN}}$$ (Fanout)

$$fo_P = \frac{I_{D0P}}{I_{D0PIN}} \quad \beta_r = \frac{I_{D0P}}{I_{D0N}}$$

K. Nose and T. Sakurai, "Closed-Form Expressions for Short-Circuit Power of Short-Channel CMOS Gates and Its Scaling Characteristics," ITC-CSCC (Korea), July 1998.

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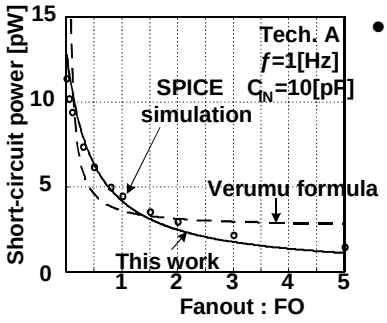
Fig.12 Short-circuit power dissipation formula

Comparison between proposed formula and other formula



- Verumu et al's formula deviates from SPICE simulation
  - fanout > 3
  - fanout is small (diverge to infinity)

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Fig.13 Comparison between proposed formula and other formulas

The change of the short-circuit power dissipation with scaling

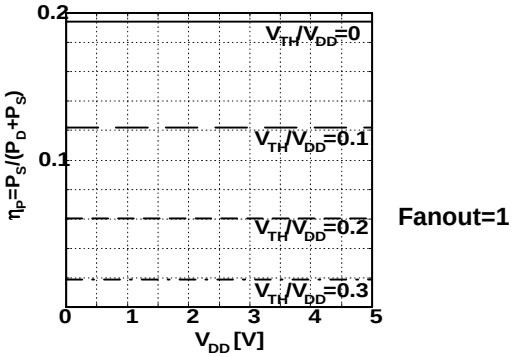

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Fig.14 The change of the short-circuit power dissipation with scaling

Voltage dependent gate cap. effect

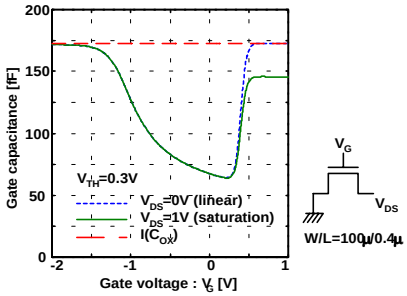

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Fig.15 Voltage dependent gate capacitance effect

Voltage dependent gate cap. effect

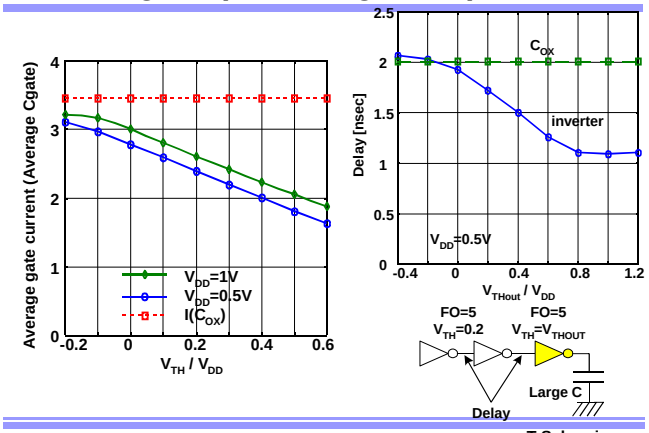

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Fig.16 Voltage dependent gate capacitance effect

Solving power issues

$P = \alpha f C V_s V_{DD}$ + leakage(sub-Vth,gate,D/S)

<u>Low-voltage</u>

- Variable-V_{TH}, multi-V_{TH}
  (Super-Cut-off CMOS, dynamic leakage cut-off SRAM, positive temp. coeff., d-type CMOS, optimum voltages)
- Variable-V_{DD}, multi-V_{DD}
  (Software control)

<u>Low-swing</u>

- Bus, clock, interconnection
  (Reduced Clock Swing F/F, bus with sense-amp. F/F, low-power repeater insertion)

<u>Others</u>

- Easy library generation for early adoption of new tech.
- Micro IDDQ test

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Fig. 17 Solving power issues

Power and delay

Power : $P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{th}}{S}} \cdot V_{DD}$ Delay = $\frac{k \cdot Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^{\alpha}}$ (α=1.3)

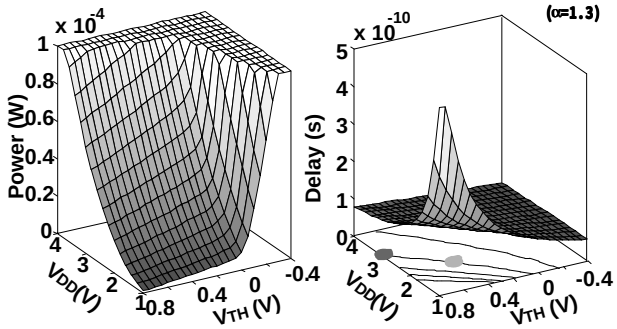

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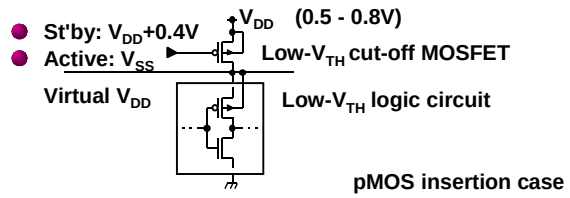
Fig. 18 Power and delay

Concept of Super Cut-off CMOS (SCCMOS)



H.Kawaguchi and K.Nose, T.Sakurai, "A CMOS Scheme for 0.5V Supply Voltage with pico-Ampere Standby Current," 1998 ISSCC, Digest of Tech. Papers, pp.192-193, Feb. 1998.

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Fig.19 Concept of super cut-off CMOS

Losing information in standby

- System level solution: →Using scan-path flip-flops
- Circuit level solution:

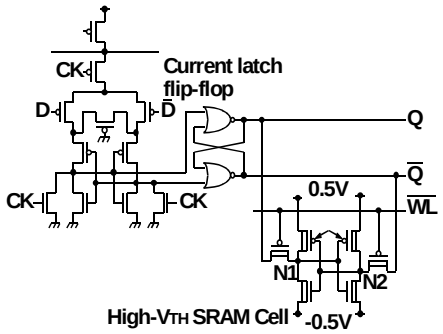

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Fig.22 Losing information in standby

Super Cut-off CMOS Scheme (SCCMOS)

0.3μm, triple-metal CMOS process
V_{TH}=0.2V

100x100μm² pumping freq=10kHz 0.1μA (@V_{DD}=0.5V)

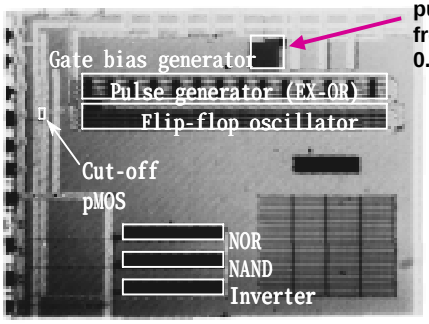

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Fig.20 Super cut-off CMOS scheme

Dynamic Leakage Cut-off

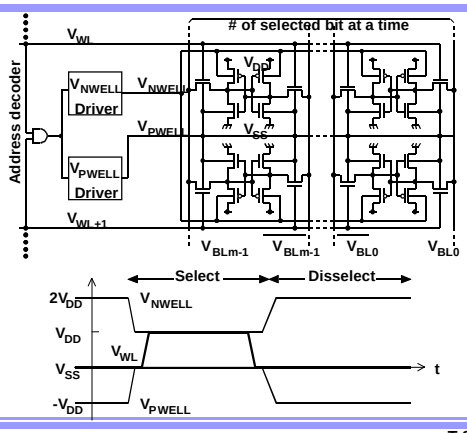

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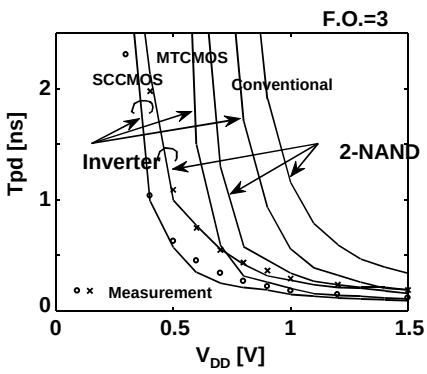
Fig.23 Dynamic leakage cut-off SRAM

Delay characteristics (inverter & NAND)



SCCMOS
0.2V V_{TH} circuit with 0.2V V_{TH} cut-off MOSFET

MTCMOS
0.2V V_{TH} circuit with 0.6V V_{TH} cut-off MOSFET

Conventional
All 0.6V circuit No cut-off MOSFET

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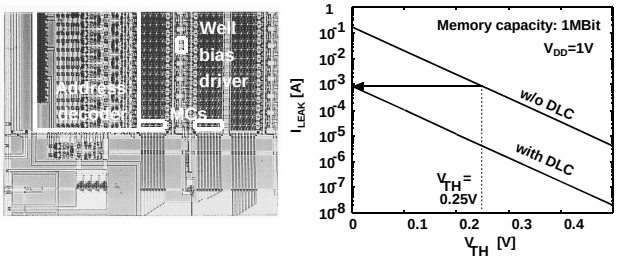
Fig.21 Delay characteristics of SCCMOS

Leakage Reduction of DLC SRAM



Total subthreshold leak of 1Mbit SRAM. At 1V VDD, VTH of the dormant cell is 0.25V while that of the active cell is 0V, keeping the total leakage power at 0.9mW.

H.Kawaguchi and T.Sakurai, "A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction," IEEE J. of Solid-State Circuits, pp.807-811, May 1998.

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Fig.24 Leakage reduction of DLC SRAM

Power Distribution in CMOS LSI's

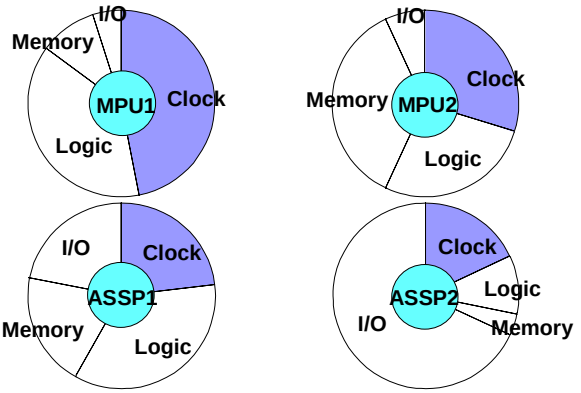

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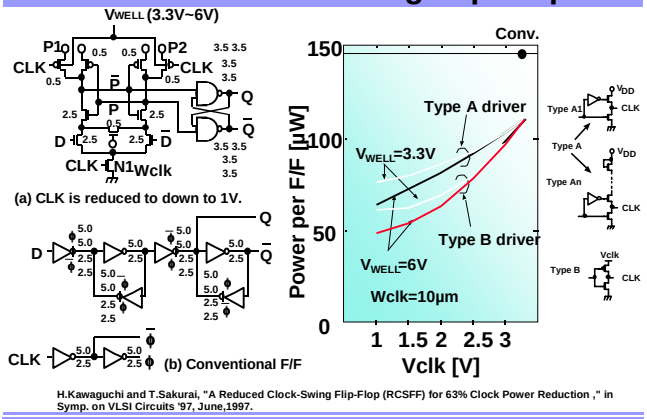
Fig.25 Power distribution in CMOS LSI's

Reduced Clock Swing Flip-Flop



H.Kawaguchi and T.Sakurai, "A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Clock Power Reduction ," in Symp. on VLSI Circuits '97, June,1997.

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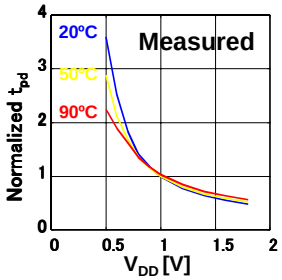
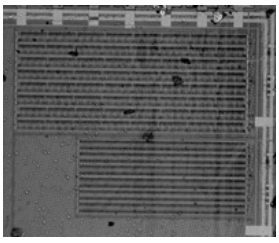
Fig.26 Reduced clock swing flip-flop

Positive temp. coeff. in low-voltage





Photograph of 32bit Adder
0.3μm CMOS

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Fig.27 Positive temperature coefficient in low-voltage region

Cause of positive temp. dependence of I_{DS}

- α-power law model (T = Temp. μ= Mobility)

$I_{DS} \propto \mu(T)\,(V_{DD} - V_{TH}(T))^{\alpha}$

	T ↗	T ↘
$\mu(T) = \mu(T_0)(T / T_0)^{-m}$	↘	↗
$V_{TH}(T) = V_{TH}(T_0) - \kappa(T - T_0)$	↘	↗

Typical Value : α=1.5, m=1.5, κ=2.5[mV/T]

Effects of V_{TH} and μ on I_{DS} when temp. goes up 100[K]

	V_{TH} effect	μ effect
V_{DD}=2.5V, V_{TH}=0.5V	10% ↗	35% ↘
V_{DD}=1.0V, V_{TH}=0.2V	55% ↗	35% ↘

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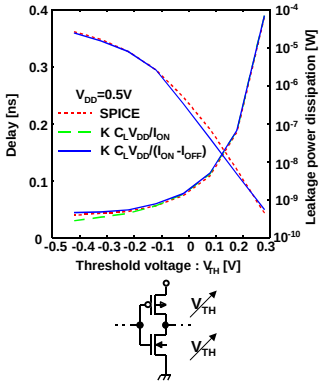
Fig.28 Cause of positive temperature dependence of I_{DS}

D-type CMOS



$$t_{LH} = K\frac{C_L V_{DD}}{(I_{PON} - I_{NOFF})} = K\frac{C_L V_{DD}}{(I_{P0} - I_{NLEAK})}$$

$$t_{HL} = K\frac{C_L V_{DD}}{(I_{NON} - I_{POFF})} = K\frac{C_L V_{DD}}{(I_{N0} - I_{PLEAK})}$$

$$t_d = \frac{t_{LH} + t_{HL}}{2}$$

K~1 (K=0.91 in this case)

D-type leakage can not be neglected in the range V_{TH}<-0.2V.

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Fig.29 D-Type CMOS

SOI Processors in ISSCC'99

Paper#	WP25.1	WP25.3	WP25.7	WP25.4
Company	IBM (East Fishkill)	IBM (Essex & Austin)	IBM (Rochester)	Samsung
Target	PowerPC 604e	PowerPC 750	PowerPC	Alpha
	32b	for Apple	64b	64b
PD/FD	PD	PD (SIMOX)	PD (SIMOX)	FD (SIMOX/Unibond no dep.)
Rule	0.25um		0.2um (Leff=0.12um)	0.25um
Interconnect	5 Al + Wlocal	Cu	6 Cu	4 Al
Area	49mm2		139mm2	209mm2
# of Tr's	6.5M		34M	9.7M
Freq.	500MHz	580MHz@85C, fast proc.	550MHz	600MHz
VDD	1.7V	2V	1.8V	1.5V (2V I/O)
Power		5.1W@2V,400MHz	24W	40W
Speed gain o	25-30%	20%	20%	30%@1.2V, 20%@1.5V SRAM
	22% Ctotal reduction	12% by Cj	15-20% simple gates	
	10-15% more Ids	15-25% by less body-bias	25-40% complex gates	

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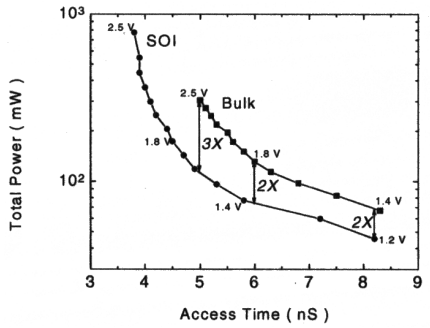
Fig.30 SOI processors in ISSCC'99

Hi-Speed is Low-Power



From URL: www.erniefernandez.com/html/soi.html

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Fig.31 Approach to low-power LSI

Approach to low-power LSI

Example of MPEG2 decoding

High flexibility

Low-power

- Processor (software)
  ~25W
- DSP
  ~4W
- Dedicated sytem LSI (SW/HW)
  ~0.7W

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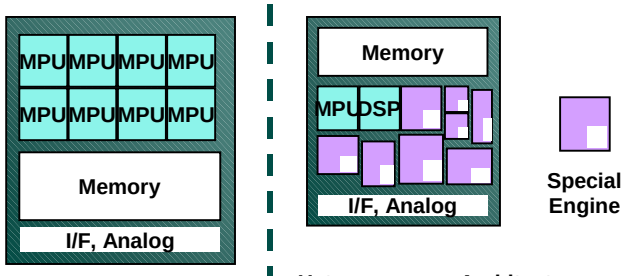
Fig.32 Approach to low-power LSI

Homogeneous vs. Heterogeneous



Homogeneous Architecture

(High flexibility)

Heterogeneous Architecture (System LSI)

(Low-power, more efficient)

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Fig.33 Homogeneous vs heterogeneous

Energy of various operation

Integration (system LSI) is the key to low-power

Operation	Energy/Op (pJ)
Add	7
3-2 Add	2
Multiply	40
Latch	1.8
Internal read	36
Internal write	71
I/O	80
External memory	16000

B.M.Gordon, E.Tsern, T.Meng,"Design of a Low Power Video Decompression Chip Set for Portable Applications," J. of VLSI Signal Processing Systems 13, pp.125-142, 1996

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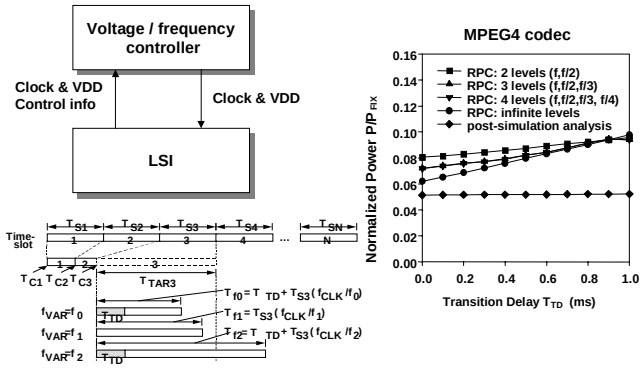
Fig.34 Energy of various operation

Software feedback loop for low-power



Seongsoo Lee, T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications," submitted ASPDAC'00.

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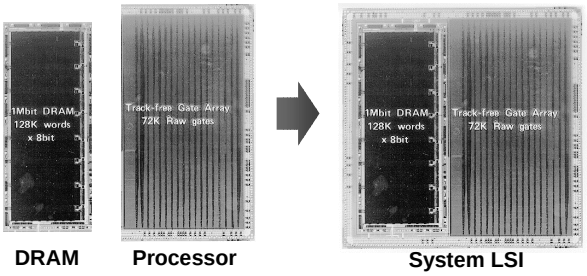
Fig.35 Software / hardware cooperation for low-power

DRAM Embedding



DRAM Processor System LSI

K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- Two orders of magnitude improvement in bandwidth and power

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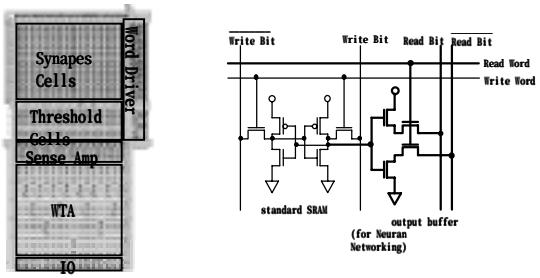
Fig.36 DRAM embedding

Neural chip



3 orders of magnitude smaller power consumption for recognition compared to software implementation
S.Takeuchi &T.Sakurai, ICCD'98, Oct.1998.

Fig.37 Neural chip

Interconnect determines cost & perf.

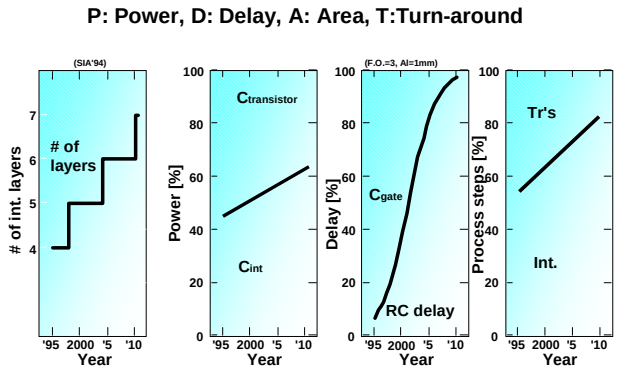
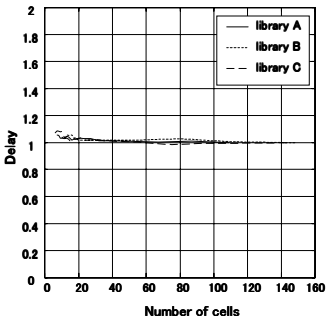


Fig.40 Interconnect determines cost & performance

Compact yet High-Performance (CyHP) Library for Low-Power Technologies



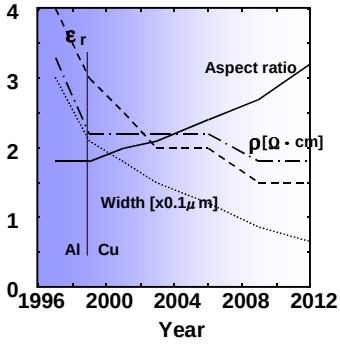
11-CELL CyHP LIBRARY

Flip-flops	D-FF x1, D-FF x2
Inverters	INV x1, INV x2, INV x4
Primitive gates	2-NAND x2 2-NOR x2 2-XNOR x1
Compound gates	2-InvNAND x2 2-InvNOR x2
Multiplexers	2-MUXInv x1

N.Duc, T.Sakurai, "Compact yet High-Performance (CyHP) Library for Short Time-to-Market with New Technologies," submitted ASPDAC'00.

Fig.38 Compact cell library for quick TAT

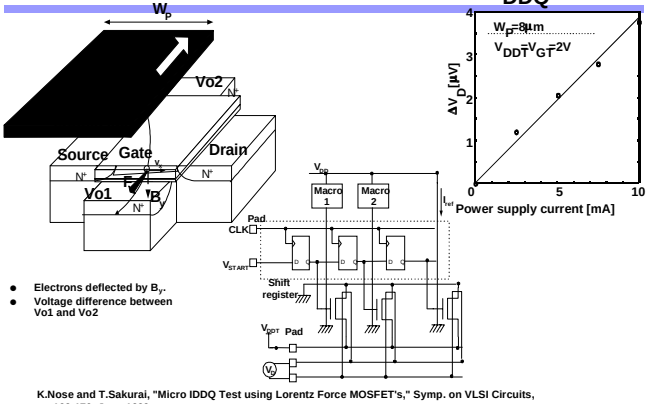
Interconnect parameters trend



Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

Fig.41 Interconnect parameters trend

Lorentz Force MOS for micro I_{DDQ} test



- Electrons deflected by B_y.
- Voltage difference between Vo1 and Vo2

K.Nose and T.Sakurai, "Micro IDDQ Test using Lorentz Force MOSFET's," Symp. on VLSI Circuits, pp.169-170, June 1999.

Fig.39 Lorentz force MOS for micro IDDQ test

RC delay and gate delay

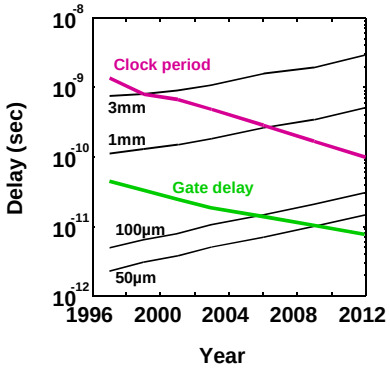
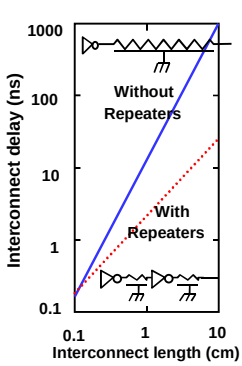
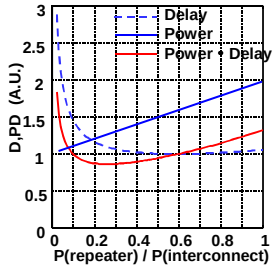


Fig.42 RC delay and gate delay

Delay and Power Optimization for Repeaters





Delay optimized
→P: P(repeater)=0.60 P(interconnect)
Power•Delay optimized
→D: 1.09 Dopt
→P: P(repeater)=0.26 P(interconnect)
→PD: 0.86 of Dopt case

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Fig.43 Delay and power optimization fro repeaters

The further, the less

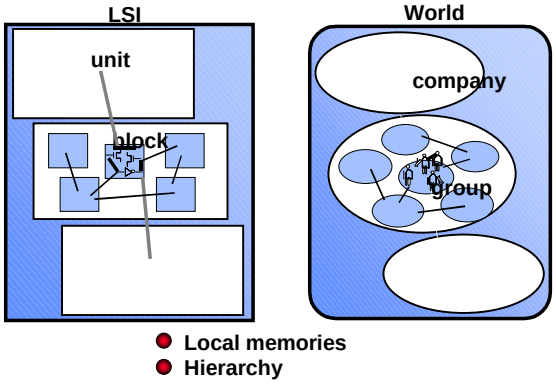

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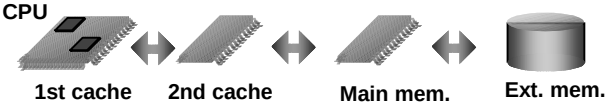
Fig.44 The further, the less

Locality in space & time

Use of local memories



Latency				
	3ns	20ns	100ns	10ms
Throughput				
	3ns	10ns	30ns	100ns

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Fig.45 Locality in space and time

Capacitive Coupling Noise

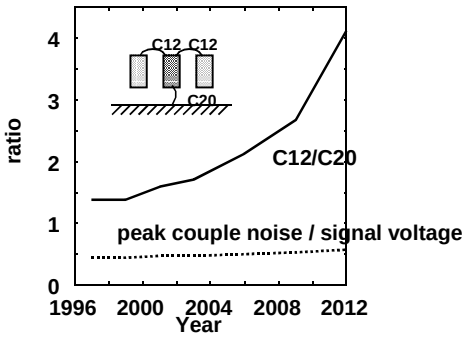

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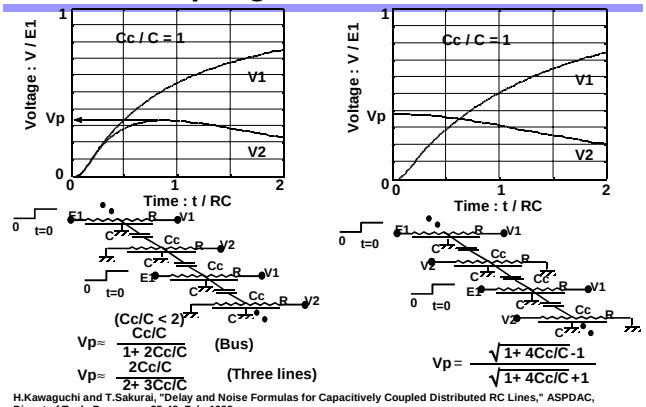
Fig.46 Capacitive coupling noise

Coupling noise in RC bus



H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

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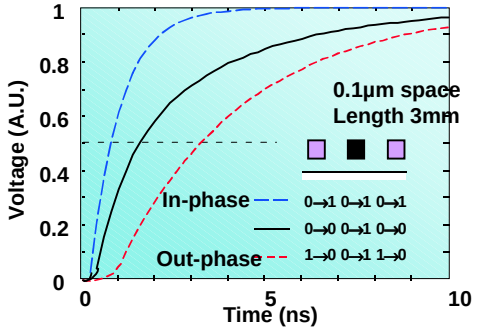
Fig.47 Coupling noise in RC bus

Coupling among Interconnection



Difficulty in checking setup and hold time.

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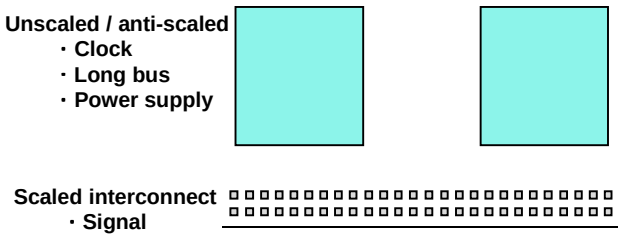
Fig.48 Coupling among interconnections

Interconnect Cross-Section and Noise



1V 15W -> 15A current
5% noise -> 0.05V noise -> 3mΩ sheet R -> 10μm thick Al
Area pad + package, or thick layer on board is needed.

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Fig.49 Interconnect sross-section and noise

Skin Effects for Signal Lines

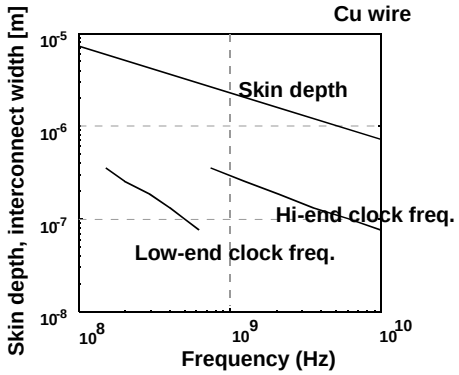

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Fig.50 Skin effects fro signal lines

Inductive Effects

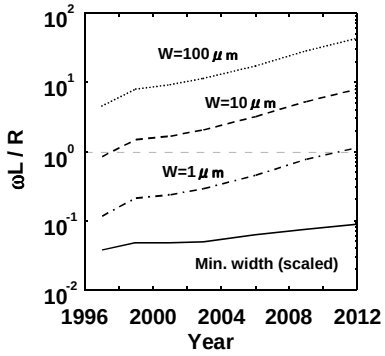

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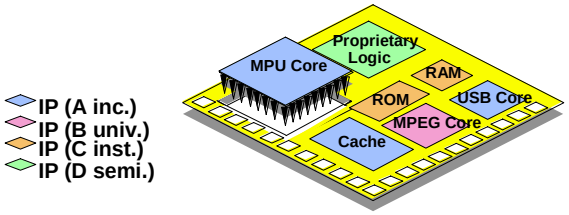
Fig.51 Inductive effects

Overcome complexity crisis

System LSI: Re-use and sharing



IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

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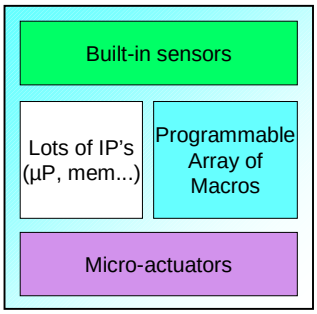
Fig.52 Overcome complexity crisis

Chip in 2012



- Sensors/actutors on chip
- 0.06μm 1G Si FET's with V_{TH} & V_{DD} control
- Locally synchronous 10GHz clock, globally asynchronous

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Fig. 53 Chip in 2012

Summary

- Scaling law indicates power, interconnection and complexity crises.
- Low-voltage + threshold control and less-waste design for low-power
- Process, design guidelines and local memory for interconnection issues
- Design reuse and sharing + software programmability for complexity

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Fig.54 Conclusions