Brief Papers

A Super Cut-Off CMOS (SCCMOS) Scheme for 0.5-V Supply Voltage with Picoampere Stand-By Current

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***Abstract*—A super cut-off CMOS (SCCMOS) scheme is proposed and demonstrated by measurement to achieve high-speed and low stand-by current CMOS VLSIs in sub-1-V supply voltage regime. By overdriving the gate of a cut-off MOSFET, the SCCMOS suppresses leakage current below 1 pA per logic gate in a stand-by mode while high-speed operation in an active mode is possible with low-threshold voltage of 0.1–0.2 V. The SCCMOS pushes the low-voltage operation limit 0.2 V further down compared with conventional schemes while maintaining the same stand-by current level.**

***Index Terms*—DTMOS, leakage current, low power, low voltage, MTCMOS, stand-by current, VTCMOS.**

I. Introduction

RECENTLY, low-power and high-performance features are pursued extensively in CMOS VLSI design to meet the increasing needs for portable multimedia application and overcome heat crisis in high-end processors. Low-voltage logic circuits have been exploited extensively because power consumption of the CMOS logic circuits quadratically depends on supply voltage $V_{\rm DD}$. If the logic circuits are operated in sub-1-V $V_{\rm DD}$ regime, for instance, in 0.5–0.8-V $V_{\rm DD}$ range, threshold voltage $V_{\rm TH}$ of MOSFETs in the logic circuits should be well below 0.5 V. This is because delay of the logic circuits increases if $V_{\rm TH}$ is not lowered. In order to obtain nanosecond-order delay, $V_{\rm TH}$ should be 0.1–0.2 V. This low $V_{\rm TH}$, however, causes 10-nA-order leakage current per logic gate in a stand-by mode, which leads to 10-mA-order for 1 million logic gate VLSIs. This prevents the VLSIs from being applied to portable equipment powered by a small battery such as a solar battery. In this paper, a super cut-off CMOS (SCCMOS) scheme is proposed which overcomes this problem. With the SCCMOS, sub-1-V $V_{\rm DD}$ operation is possible with 0.1–0.2-V $V_{\rm TH}$, at the same time realizing picoampere-order stand-by current per logic gate.

II. Concept of SCCMOS

Fig. 1 shows a concept of the SCCMOS for a pMOS insertion case. The pMOS insertion case is explained and verified by experiments in this paper. This is because a p-type substrate is widely used and suitable for the pMOS insertion case, as is explained below. With the p-type substrate, the well voltage of pMOSs in logic circuits and the cut-off pMOS can be different because both the wells can be electrically isolated. Therefore, the bodies of the pMOSs in the logic circuits may be connected with virtual $V_{\rm DD}$, $V_{\rm DDV}$, line, which does not require other lines for the pMOS body bias. This means that the $V_{\rm DD}$ line in existing cell libraries can be used as the $V_{\rm DDV}$ line and layout modification to the cell libraries can be minimized. The pMOSs in the logic circuits can also share the well with the cut-off pMOS. In this case, however, an extra virtual $V_{\rm DD}$ line must be added to the cell libraries. Likewise, an nMOS insertion case is also possible with an extra virtual ground line to the cell libraries.

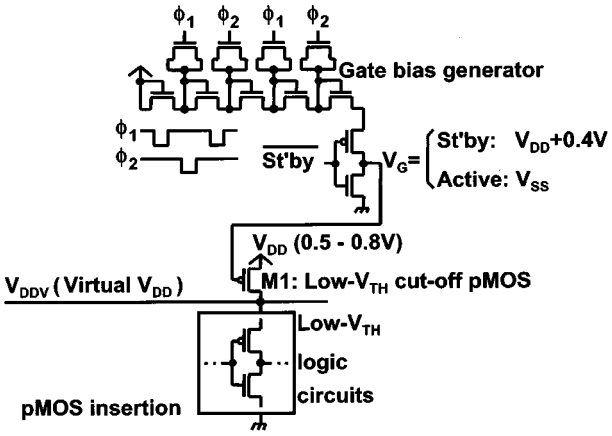

Fig. 1. Concept of SCCMOS.

In Fig. 1, the low-$V_{\rm TH}$ cut-off pMOS, M1, whose $V_{\rm TH}$ is 0.1–0.2 V, is inserted in series to the logic circuits consisting of low-$V_{\rm TH}$ MOSFETs. The low $V_{\rm TH}$ assures high-speed operation of the logic circuits. The gate voltage of M1, V_G is grounded in an active mode to turn M1 on. When the logic circuits enter stand-by operation, V_G is overdriven to $V_{\rm DD}+0.4$ V to completely cut off the leakage current. This is because the low $V_{\rm TH}$ of 0.1–0.2 V is lower by 0.4 V than conventional high $V_{\rm TH}$ (0.5–0.6 V), and thus this overdriven mechanism can sustain the stand-by current level. If $V_{\rm TH}$ is lower than 0.1–0.2 V or negative, V_G should be also lowered as long as there is no problem of gate-oxide reliability or gate-induced drain leakage (GIDL) [1]. On the other hand, in the nMOS insertion case, $V_{\rm DD}$ is applied to the gate of the cut-off nMOS in the active mode and overdriven to -0.4 V in the stand-by mode.

The gate bias generator for V_G can be made relatively easy without any feedback, as is shown in Fig. 1, because precise control of V_G is not needed unless the gate-oxide reliability or the GIDL becomes an issue. V_G can be driven slowly because high

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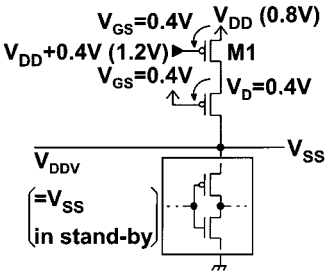

Fig. 2. Gate-oxide reliability problem in SCCMOS.

speed is not needed when the logic circuits enters the stand-by operation. Therefore, the pumping frequency can be low.

Fig. 2 shows a technique to reduce voltage across the gate oxide when the gate-oxide reliability is an issue, as it is in the case of future scaled-down devices. In the stand-by mode, $V_{\rm DDV}$ drops to ground, $V_{\rm SS}$, due to large leakage current of the low-$V_{\rm TH}$ MOSFETs. This may cause the gate-oxide reliability problem of the cut-off pMOS when thin gate oxide is used. For instance, 1.2 V is applied across the gate oxide of the cut-off pMOS in the stand-by mode at 0.8-V $V_{\rm DD}$. In order to prevent the gate oxide from breaking down, connecting two pMOSs in series as the cut-off pMOSs is effective. In this case, both the pMOSs work in a subthreshold region where drain current strongly depends on $V_{\rm GS}$, not $V_{\rm DS}$. The drain voltage of M1, V_D, becomes 0.4 V to draw the same amount of current through them if their gate widths are the same. This combination can reduce maximum voltage across the gate oxide from 1.2 to 0.8 V.

III. Comparison With Other Schemes

There are other schemes that have been reported that realize high speed in low voltage and at the same time reduce leakage current in a stand-by mode.

A. MTCMOS

Multithreshold CMOS (MTCMOS) uses high $V_{\rm TH}$ as a cut-off MOSFET in series with low-$V_{\rm TH}$ logic circuits to cut off leakage current in a stand-by mode [2]. MTCMOS does not work below 0.6-V $V_{\rm DD}$ because the high-$V_{\rm TH}$ MOSFET does not turn on. Therefore, the MTCMOS cannot be used in sub-1-V $V_{\rm DD}$.

B. VTCMOS

Another scheme called variable-threshold CMOS (VTCMOS) applies back-gate bias to cut off leakage current in a stand-by mode by exploiting body effect [3], [4]. This scheme cannot be applied to fully depleted SOI process technology. It is also difficult to apply to partially depleted SOI process technology due to the overhead required to connect the body of each MOSFET with interconnection for applying the body bias. Another drawback is that the VTCMOS requires modification to cell libraries to separate back-gate bias lines from $V_{\rm DD}$ and $V_{\rm SS}$ lines.

C. DTMOS

Dynamic-threshold MOS (DTMOS) ties the gate and body of a SOI MOSFET together and thus changes $V_{\rm TH}$ of the MOSFET so that $V_{\rm TH}$ is high in an off-state and is low in an on-state. The DTMOS, however, suffers from 10-mA-order leakage current in 0.5–0.7-V $V_{\rm DD}$ for 1 million logic gate VLSIs, because of inherent forward-bias current of the p-n-junction associated with the source–body junction of the MOSFET [5]. By combining the SCCMOS and the DTMOS, the leakage current in a stand-by mode can be reduced while the DTMOS remains at high speed in an active mode. For this purpose, the VTCMOS cannot be used with the DTMOS where the body is always fixed to the gate.

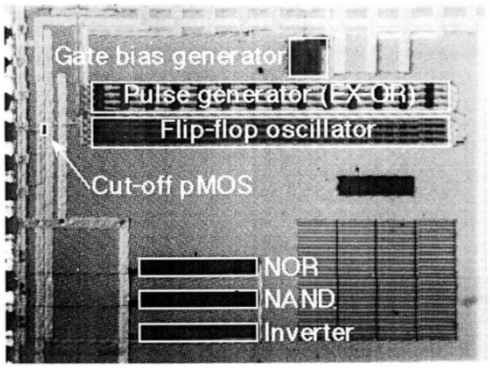

Fig. 3. Microphotograph of fabricated SCCMOS test chip.

IV. Measurement Results

A test chip is fabricated with 0.3-μm triple-metal CMOS process technology whose $V_{\rm TH}$ is 0.2 V for both pMOSs and nMOSs to demonstrate the effectiveness of the SCCMOS. A microphotograph of the test chip is shown in Fig. 3. The area of the gate bias generator is $100 \times 100\ \mu{\rm m}^2$. Current consumption for the gate bias generator is 0.1 μA at 0.5-V $V_{\rm DD}$. Pumping frequency of the gate bias generator is set to be 10 kHz. Delay and stand-by current of inverters, 2-NANDs, flip-flops, and pass-transistor logic gates are measured by means of ring oscillators that have 101 logic gate stages.

A. Inverters and 2-NANDs

Measured speed characteristics of the inverters and the 2-NANDs with a fan-out of three are shown in Fig. 4, with circles and crosses respectively. Simulated delay characteristics are shown with lines. Gate widths in the logic gates are all 2.4 μm so that total logic gate width is 484.8 μm for the inverters and 969.4 μm for the 2-NANDs. On the other hand, the gate width of the cut-off MOSFET is 10 μm. The SCCMOS pushes low-voltage operation limit of the logic gates further than the MTCMOS. In addition, the SCCMOS operates almost at the same speed of the "no cut-off MOSFET" case. That is, 10-μm width is sufficiently large as the cut-off MOSFET. Measured stand-by current is below 1 pA per logic gate. Active energy consumption of the 2-NAND with a fan-out of three is 8 fJ per switching.

Fig. 5 shows simulated speed dependency on the gate width of the cut-off MOSFET(s) in cases of both single and serial connections, as is shown in Fig. 2. Speed degradation is 4.6% for the inverters and 8.6% for the 2-NANDs in the single cut-off MOSFET case. On the other hand, double width is needed for the serial connection to achieve the same speed of the single

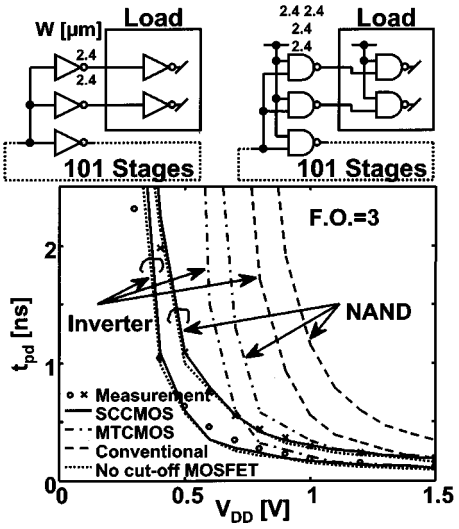

Fig. 4. Measured speed of inverters and 2-NANDs with SCCMOS.

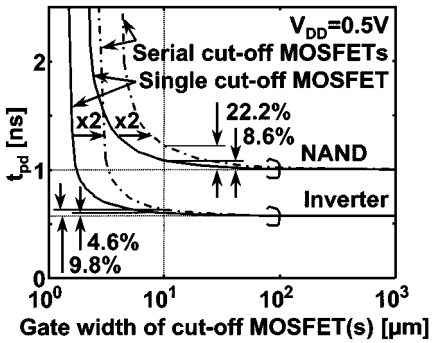

Fig. 5. Simulated speed dependency on gate width of cut-off MOSFET(s) in SCCMOS.

cut-off MOSFET case, which means that the area overhead is four times as large as the single connection case.

B. Keeping Information in Stand-By Mode

When logic circuits are in a stand-by mode and a cut-off MOSFET turned off, $V_{\rm DDV}$ drops almost to $V_{\rm SS}$ due to large leakage current of low-$V_{\rm TH}$ logic circuits. Then, flip-flops in the low-$V_{\rm TH}$ logic circuits lose stored information in the stand-by mode. This is fatal in certain applications. One way to solve the problem at the system level is to send all information stored in the flip-flops to external memories before entering the stand-by operation and to restore the information back to the flip-flops at wake-up with scan-path flip-flops.

When this solution at the system level is not preferable, the flip-flop in Fig. 6 can be used. The current-latch flip-flop in the figure is a low-power flip-flop and extensively used in industrial design. The flip-flop is made of the low-$V_{\rm TH}$ MOSFETs for high speed with a cut-off MOSFET, and an SRAM cell that is composed of high-$V_{\rm TH}$ MOSFETs is added to the flip-flop to suppress leakage current in the stand-by mode. Source voltage of the SRAM cell is -0.5 V to obtain strong drive at wake-up. Therefore, the substantial supply voltage is equivalent to 1 V. If the driving capability of the SRAM cell is low, the SRAM cell cannot write the stored information back into the output nodes of cross-coupled 2-NORs, Q and $\overline{Q}$, and the stored information

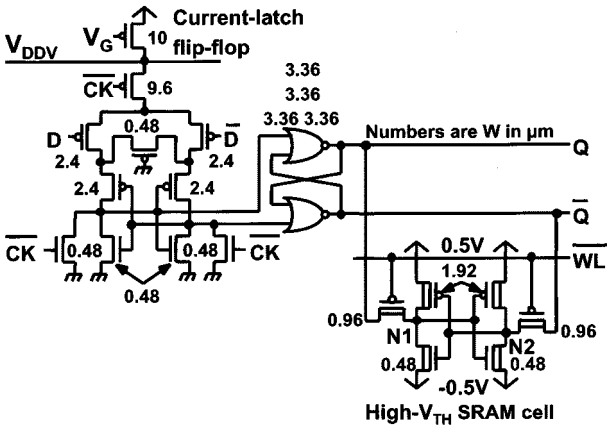

Fig. 6. Flip-flop with SCCMOS.

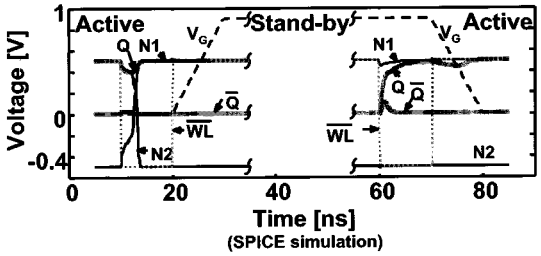

Fig. 7. Operation waveforms of flip-flop with SCCMOS.

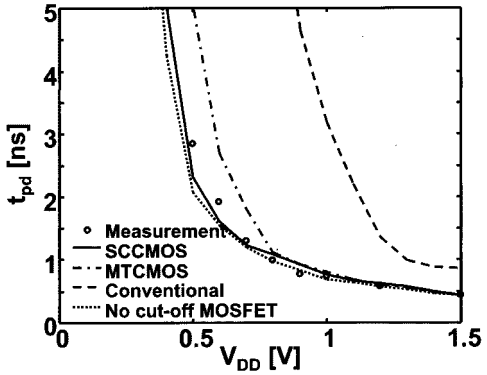

Fig. 8. Measured speed of flip-flops with SCCMOS.

of the SRAM cell is overwritten. Waveforms of the flip-flop are shown in Fig. 7. Before entering the stand-by operation, at first, $\overline{WL}$ is asserted and Q and $\overline{Q}$ is stored in N1 and N2. In the stand-by mode, Q and $\overline{Q}$ become almost $V_{\rm SS}$ due to the large leakage current of the low-$V_{\rm TH}$ logic circuits. N1 and N2, however, keep the right information. In the wake-up process, $\overline{WL}$ is asserted again, and the stored information is written back into Q and $\overline{Q}$.

C. Flip-Flops

Fig. 8 shows measured speed characteristics of the flip-flops. In order to measure the flip-flop delay, flip-flops with an edge-trigger pulse generator shown in Fig. 9 is used. At first, the delay of the flip-flops with the edge-trigger pulse generators is measured, and then the delay of only edge-trigger pulse generators is subtracted from the delay of the flip-flops with the edge-trigger pulse generators to obtain the genuine flip-flop delay. -0.5 V

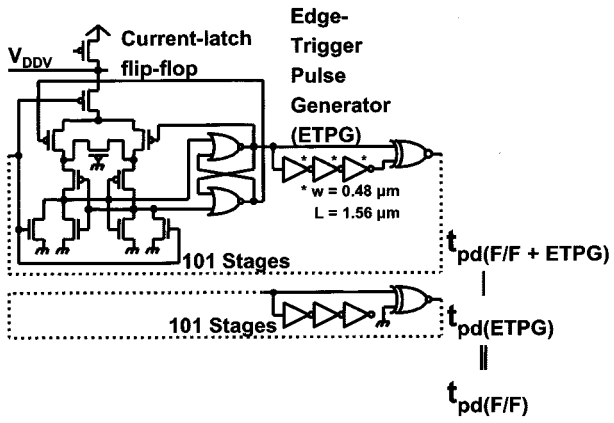

Fig. 9. Method of measuring speed of flip-flops with SCCMOS.

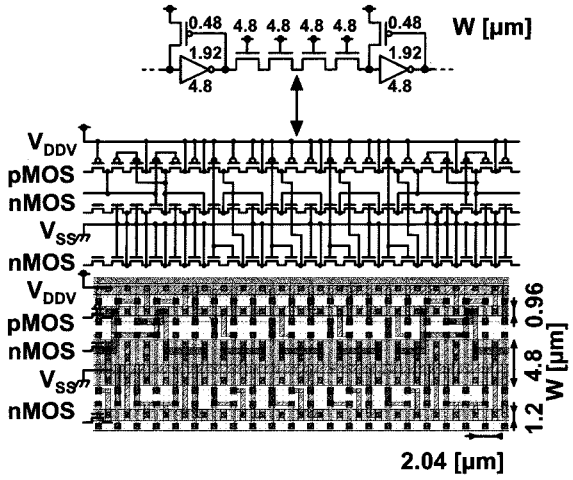

Fig. 10. PTL gate array with SCCMOS.

is applied to the p-type substrate to prevent the p-n-junction from being forward-biased in the SRAM cells only in this measurement. The -0.5-V back-gate bias of the p-type substrate increases $V_{\rm TH}$ of all nMOSs to 0.3 V from 0.2 V because the process is not a triple-well technology. This is the reason the flip-flops are slow in this experiment. With the triple-well technology, the flip-flop delay decreases to about three times the inverter delay with fan-out of three.

D. Pass-Transistor Logic Gate

The test circuit of pass-transistor logic (PTL) gates that can achieve high area efficiency is fabricated with the gate-array structure shown in Fig. 10. A schematic is also shown in the figure. The PTL gate-array structure is optimized for single-rail and is simpler than the previously published basic gate-array structure [6]. One basic cell is composed of a pMOS and two nMOSs. The gate width of the pMOS is 0.96 μm and those of nMOSs are 4.8 and 1.2 μm that are optimized sizes also as an SRAM cell. Thus, the SRAM cell can also be mapped onto this gate-array with two basic cells. Swing restoring structure to obtain full swing made of a small feedback pMOS restores $V_{\rm TH}$ drop due to a series of nMOS transfer gates. Fig. 11 shows measured delay characteristics of the single-rail PTL gates with the

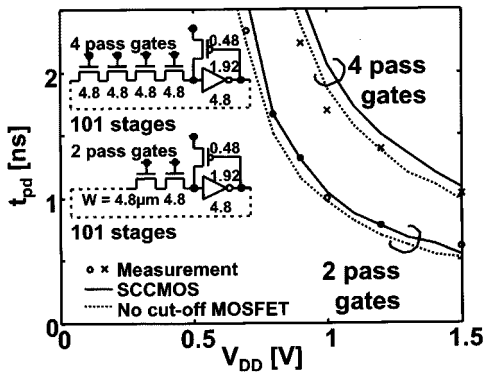

Fig. 11. Measured speed of PTL gates with SCCMOS.

SCCMOS. Operation at 1-V $V_{\rm DD}$ is verified but 0.5-V operation is questionable with the PTL gates because of an inherent $V_{\rm TH}$ voltage drop. However, it can be said that the SCCMOS does not degrade the speed of the CMOS logic gates and the PTL gates.

V. Summary

The SCCMOS is proposed to realize CMOS logic circuits working below 0.5-V $V_{\rm DD}$ while maintaining 1-pA-order stand-by current per logic gate. It is experimentally demonstrated that $V_{\rm DD}$ can be decreased to 0.5 V and $V_{\rm TH}$ can also be decreased to less than 0.2 V without speed and stand-by current degradation. The SCCMOS can be effectively combined with SOI, DTMOS, and/or PTL gates and is promising for future CMOS VLSIs that are optimized for low-power operation.

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