Abstract - If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI’s for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis. This paper describes these crises and possible solutions to cope with the problems.

Summary

If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI’s for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis.

As for power crisis, there are activities to lower the power consumption from device level, circuit level to system level. Lowering supply voltage (VDD) is very effective in reducing the power but the threshold voltage (VTH) should be reduced at the same time for high-speed operation. The low VTH, however, increases the leakage current. To overcome this situation, VTH and VDD control through the use of multiple VTH, variable VTH, multiple VDD and variable VDD are intensively pursued and some have been productized. At the system level, system LSI approach is promising for realizing low power and the new trend is to exploit cooperation of software and hardware. In the sub 1-volt design, watch out for the abnormal temperature dependence of drain current.

The interconnection will be determining cost, delay, power, reliability and turn-around time of the future LSI’s rather than MOSFET’s. RC delay problem can be solved through LSI architecture realizing “the further, the less communication” with the help of local memories.

It is just impossible to design LSI’s with 100 million transistors from scratch. The complexity issue can only be solved by the sharing and re-use of design data. So-called IP-based design will be preferable. The virtual components are put together on a silicon to build billion transistor LSI’s, which can be compared to the present system implementation with pre-manufactured LSI components.

References


Fig. 4 VDD, Power and Current Trend (From SIA)

<table>
<thead>
<tr>
<th>Year</th>
<th>Voltage [V]</th>
<th>Power per chip [W]</th>
<th>VDD current [A]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1998</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>2002</td>
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<td>2010</td>
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<td>2014</td>
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</tbody>
</table>

Fig. 5 Necessity for Low-Power Design

- **NMOS** → CMOS: Cost up
- **Bipolar** → CMOS: Speed down
- Not cost nor speed but power set the technology trend.
- Integration can achieve low cost and high speed as a system.

Fig. 6 What sets the technology trend?

\[
P = \alpha \cdot C_L \cdot \Delta V_s \cdot V_{DD} + \text{leakage (sub-Vth, gate, D/S)}
\]

- Charging & discharging: $C_L \cdot \Delta V_s \cdot V_{DD}$
- Crowbar current: $I_{SC}$
- Static current: $I_{DC}$
- Subthreshold leak current: $I_{LEAK}$

Fig. 7 Expression for CMOS Power

\[
V_{DD} = \sqrt{\frac{P}{\alpha \cdot C_L \cdot \Delta V_s}}
\]

Fig. 8 Voltage waveform of CMOS inverter

Fig. 9 Short-circuit power dissipation formula

\[
P = \frac{k(v_{DHP})}{V_{DD}^2} \cdot \frac{2(f_{MAX})}{h(v_{T}, \alpha) \cdot f_{P}} + \frac{C_P}{C_W}
\]

Fig. 10 The change of the short-circuit power dissipation with scaling

Fig. 11 VDD, VTH, Power and Current Trend

\[
P = \alpha \cdot f \cdot C \cdot V_s \cdot V_{DD} + \text{leakage (sub-Vth, gate, D/S)}
\]

**Low-voltage**
- Variable-V_{DD}, multi-V_{TH}
  - (Super-Cut-off CMOS, dynamic leakage cut-off SRAM, positive temp. coeff., d-type CMOS, optimum voltages)
- Variable-V_{TH}, multi-V_{DD}
  - (Software control)

**Low-swing**
- Bus, clock, interconnection
  - (Reduced Clock Swing F/F, bus with sense-amp. F/F, low-power repeater insertion)

**Others**
- Easy library generation for early adoption of new tech.

Fig. 12 Solving power issues
**Fig. 13** Power and delay

- In standby mode and in IDDQ test, substrate bias is applied to increase VTH, which reduces leakage.
- In active mode, substrate bias is not applied to lower VTH, which ensures high speed.

**Fig. 14** Standby Power Reduction (SPR) Circuit

- In active mode, low VTH MOSFET’s achieve high speed.
- In standby when standby signal is high, high VTH MOSFET’s in series to normal logic circuits cut off leakage current.

**Fig. 15** Self-Adjusting Threshold-voltage Scheme

**Fig. 16** Measured I_{leak} in SAT+SPR

**Fig. 17** Multi-Threshold CMOS Circuit

**Fig. 18** Super Cut-off CMOS (SCCMOS). H. Kawaguchi and K. Nose, T. Sakurai, "A CMOS Scheme for 0.5V Supply Voltage with pico-Ampere Standby Current," ISSCC, pp. 192-193, Feb. 1998.

**Fig. 19** Super Cut-off CMOS Scheme (SCCMOS)

- System level solution: Using scan-path flip-flops
- Quick bistable solution

**Fig. 20** Delay characteristics (inverter & NAND)

**Fig. 21** Losing information in standby

**Fig. 22** Dynamic Leakage Cut-off
**Fig. 23** Power Distribution in CMOS LSI's

**Fig. 24** Reduced Clock Swing Flip-Flop

**Fig. 25** Positive temp. coeff. in low-voltage

- $i_{DD} = \mu(T) (V_{DD} + V_{TH}(T))^n$

<table>
<thead>
<tr>
<th>Typical Value</th>
<th>$n=1.5$, $m=1.5$, $p=2.5$</th>
<th>$T=100[K]$</th>
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</thead>
<tbody>
<tr>
<td>$V_{DD} = 2.5V$, $V_{TH} = 0.5V$</td>
<td>$i_{DD} = 10%$, $p_{DD} = 35%$</td>
<td>$i_{DD} = 10%$, $p_{DD} = 35%$</td>
</tr>
<tr>
<td>$V_{DD} = 1.0V$, $V_{TH} = 0.3V$</td>
<td>$i_{DD} = 55%$, $p_{DD} = 35%$</td>
<td>$i_{DD} = 55%$, $p_{DD} = 35%$</td>
</tr>
</tbody>
</table>

**Fig. 26** Cause of positive temp. dependence of $I_{DS}$

**Fig. 27** SOI Processors in ISSCC '99

**Fig. 28** Hi-Speed is Low-Power.

- Processor (software) $\approx 25W$
- DSP $\approx 4W$
- Dedicated sysytem LSI (5W/4W) $\approx 0.7W$

**Fig. 29** Approach to low-power LSI

- Homogeneous Architecture (High flexibility)
- Heterogeneous Architecture (System LSI) (Low-power, more efficient)

**Fig. 30** Homogeneous vs. Heterogeneous

**Fig. 31** Software feedback loop for low-power

**Fig. 32** DRAM Embedding
Fig. 33: Compact yet High-Performance (CyHP) Library for Low-Power Technologies

P: Power, D: Delay, A: Area, T: Turn-around

Fig. 34: Interconnect determines cost & perf.

Fig. 35: Interconnect parameters trends

Fig. 36: RC delay and gate delay

Fig. 37: RC delay of global interconnections

Fig. 38: Delay and Power Optimization for Repeaters

Fig. 39: The further, the less

Fig. 40: Locality in space & time

Fig. 41: Capacitive Coupling Noise
Fig.42 Coupling noise in RC bus

Fig.43 Coupling among Interconnection

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply

Scaled interconnect
- Signal

1V 15W \rightarrow 15A current
5% noise \rightarrow 0.05V noise \rightarrow 3\mu m sheet R \rightarrow 10\mu m thick Al
Area pad + package, or thick layer on board is needed.

Fig.44 Interconnect Cross-Section and Noise

Fig.45 Skin Effects for Signal Lines

Fig.46 Inductive Effects

Fig.47 System LSI design complexity increases faster than productivity. (http://notes.sematech.org/97melec.htm)

Fig.48. Overcome complexity crisis

Fig.49. LSI in 2014

Fig.50 Chip in 2014