

Low Power Design of Digital Circuits

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Abstract

This paper will cover several of the schemes including multi- V_{TH} , variable V_{TH} , multi- V_{DD} and variable V_{DD} , to achieve low-power systems. Circuit level ideas to software related research are described.

1. Introduction

Power consumption of the VLSI's has been ever increasing (Fig.1) and a VLSI processor dissipating more than 100W has been introduced. A roadmap is suggesting even more power increase in the future with the supply voltage less than 0.5V (Fig.2). Thus, low-power and low-voltage designs are and will continue to be important for further progress of VLSI's.

2. Power consumption of CMOS VLSI's

The expression for power consumption is shown in Fig.3. The crowbar current component (or short-circuit current component) is less than 10% of total active power at present and will be decreasing in the future when V_{TH}/V_{DD} is increased (Fig.4-7). Consequently, the charging and discharging current component is dominant in an active mode and in a standby mode, leakage current component dominates. In the leakage components, subthreshold current is dominant now but gate tunneling current and gate induced drain leakage should be considered in the future. In calculating the dynamic current component, the voltage dependent gate capacitance should be watched out for (Fig. 8, 9).

Using typical values, power and delay are calculated for various V_{DD} and V_{TH} in Figs. 10 and 11. In order to reduce the power, it is preferable to decrease V_{DD} but decreasing V_{DD} leads to the decrease of performance. When we reduce V_{DD} , if we reduce V_{TH} at the same time, it is possible to maintain the speed of circuits. Then, the issue is the increase of the subthreshold leakage in the low- V_{TH} region. This is the reason why some V_{DD} - V_{TH} control is needed to achieve low-power yet high-speed circuits.

3. Multi- V_{TH} , Variable V_{TH} , Multi- V_{DD} and Variable V_{DD}

Using two V_{TH} 's (MTCMOS) is one idea to take the trade-off between the speed in an active mode and the leakage in a standby mode. The other idea is to vary the V_{TH} dynamically using substrate bias effect, namely VTCMOS, which has been also pursued and productized [8, 9]. MTCMOS is definitely one way but does not operate properly when V_{DD} decreases below

0.5V. To overcome this shortcoming, Super Cut-off CMOS (SCCMOS) is proposed (Fig.12-15). By over-driving the MOS gate in a standby mode, it is possible to completely cut off the leakage current of low- V_{TH} MOSFET's. The original MTCMOS and VTCMOS are applicable to logic part of the design but are not applicable to low-voltage SRAM's. If MTCMOS is applied to an SRAM, the stored information is lost in a standby. On the other hand, if VTCMOS is applied to an SRAM with low- V_{TH} memory cells for high-speed purpose, the leakage current in an active mode is enormous. A possible solution to this problem is row-wise selective biasing as is shown in Fig.16.

In a multiple-voltage scheme known as Dual-VS scheme, critical paths are driven with higher V_{DD} , while non-critical gates are operated under low V_{DD} . An example of variable V_{DD} approach called software feedback loop is shown in Figs.17-18. Making use of data dependency, an order of magnitude reduction of power is possible with the scheme. This is a hardware-software cooperative approach for low power.

When using sub-0.5V V_{DD} and low- V_{TH} , watch out for the positive temperature dependence of speed (Fig.19-21). Thermal instability may occur when improper package is used (Fig.22). In introducing new circuit concept, layout modification of standard cell library is needed sometimes. It has been shown, however, small number of cells are sufficient in a library to achieve high performance (Fig.33, Table I, II).

4. Other low-power approaches

Power consumption of a clock system in a digital VLSI is comparable to the power consumed in other logic gates (Fig.24). In order to reduce the power for clocking, reduced swing clock scheme with special flip-flops has been proposed (Fig.25). In the buffer insertion process in interconnection system optimization, if the delay is considered as a target function, the power increase by the buffer insertion amounts up to 60%, while if PD product is considered as an object function, the power increase is 26% (Fig.26). Verifying the standby power is another important issue. By using a special current sensing device, it is possible to measure the standby current (Fig.27-28). In an architectural level, a system LSI approach shows lower power than a general processor approach at the sacrifice of generality and historically low-power has set the technology trend (Fig.29-31).

References

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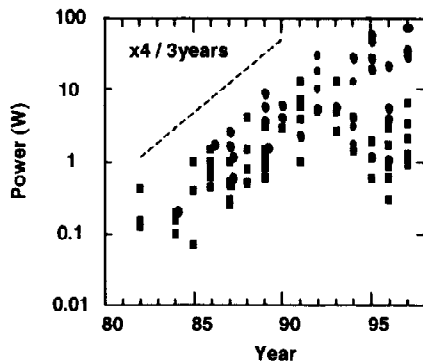


Fig.1 Trend in processor power (from ISSCC)

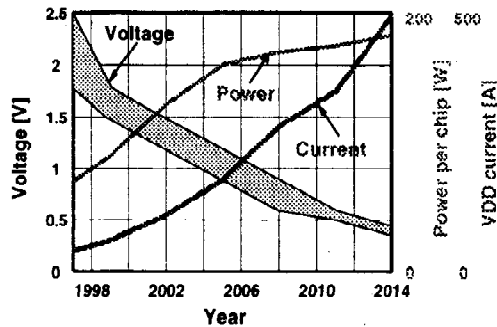


Fig.2 Trend in voltage and power (from SIA)

$$P = \alpha \cdot C_L \cdot V_s \cdot V_{DD} \cdot f_{CLK} + \alpha \cdot I_{SC} \cdot \Delta t_{SC} \cdot V_{DD} \cdot f_{CLK} + I_{DC} \cdot V_{DD} + I_{LEAK} \cdot V_{DD}$$

Charging & discharging
Crowbar current
Static current
Subthreshold leak current

α : Switching probability
 C_L : Load capacitance
 V_s : Signal swing
 V_{DD} : Supply voltage
 I_{SC} : Mean crowbar current
 Δt_{SC} : Crowbar current duration
 f_{CLK} : Clock frequency
 I_{DC} : DC current
 I_{LEAK} : Subthreshold leak current

Charge: $Q = C_L \cdot V_s$
Discharge: $Q = C_L \cdot V_s$
 $C_L \cdot V_s$ amount of charge
loses V_{DD} of potential
 $\rightarrow C_L \cdot V_{DD} \cdot V_s$ energy
consumption per cycle

Fig.3 Expression for CMOS power

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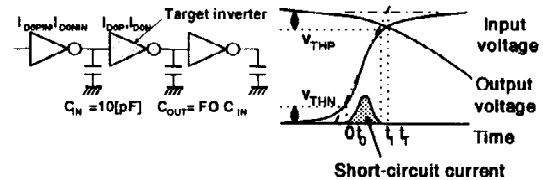


Fig.4 Short-circuit current (crowbar current)

$$P_S = \frac{k(v_{DDP})f\phi_r^2 C_{IN} V_{DD}^2}{\frac{v_{DDP} g(v_T, \alpha)}{2k(v_{DDP})} FO \beta_r + h(v_T, \alpha) f\phi_r}$$

$$g(v_T, \alpha) = \frac{\alpha + 1}{f(\alpha)} \frac{(1 - v_{TN})^{\alpha+1} (1 - v_{TP})^{\alpha+1}}{(1 - v_{TN} - v_{TP})^{\alpha+1}}$$

$$F.O. = \frac{C_{OUT}}{C_{IN}} \text{ (Fanout)}$$

$$h(v_T, \alpha) = 2^{\alpha+1} \frac{(1 - v_{TN})^{\alpha+1}}{(1 - v_{TN} - v_{TP})^{\alpha+1}}$$

$$k(v_{DDP}) = \frac{0.9}{0.8} \cdot \frac{v_{DDP}}{0.8} \ln \frac{10 v_{DDP}}{e}$$

$$f\phi_r = \frac{I_{DDP}}{I_{DDPN}} \quad \beta_r = \frac{I_{DDP}}{I_{DDN}}$$

Fig.5 Expression for short-circuit power (Ref.1)

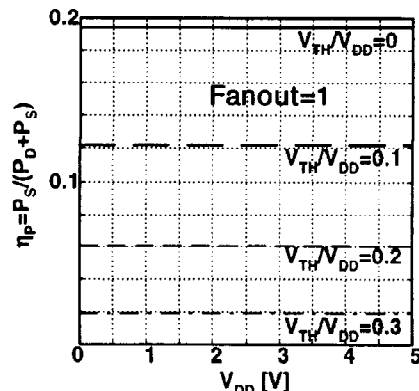


Fig.6 Ratio of short-circuit power (P_S) vs total active power ($P_S + P_n$)

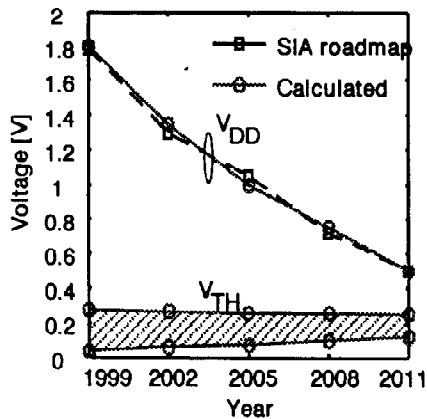


Fig. 7 Optimum V_{DD} and V_{TH} (Ref.2)

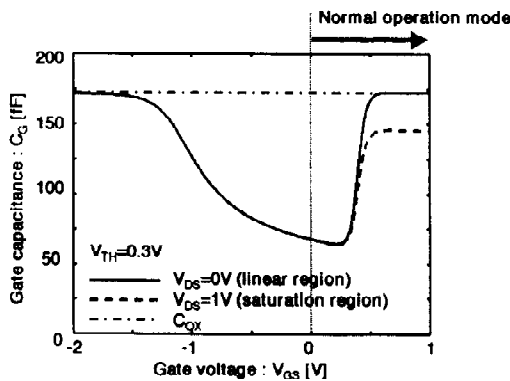


Fig. 8 Voltage dependent gate capacitance (Ref.7)

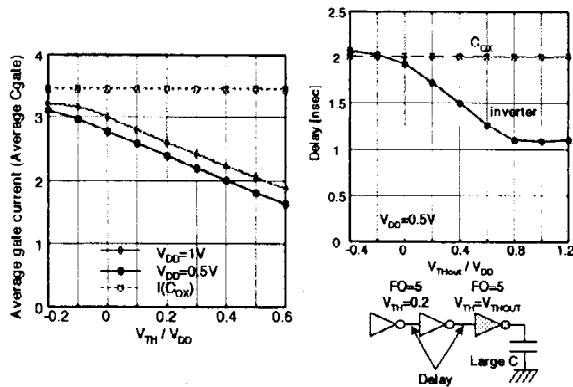


Fig. 9 Effect of voltage dependent gate capacitance

$$\text{Power : } P = p_i \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-5} \cdot \frac{V_{DD}}{s} \cdot V_{DD}$$

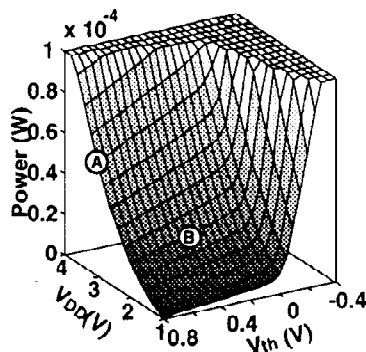


Fig. 10 Power dependence on V_{DD} & V_{TH}

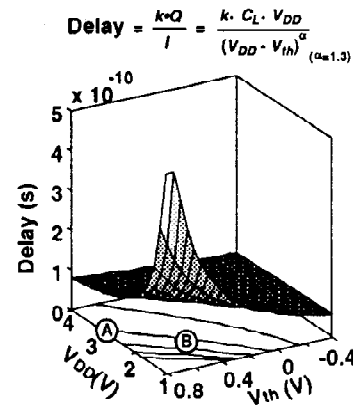


Fig. 11 Delay dependence on V_{DD} & V_{TH}

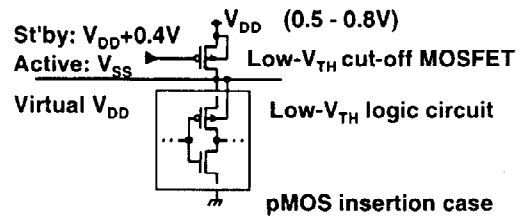


Fig. 12 Concept of Super Cut-off CMOS (SCCMOS) (Ref.4)

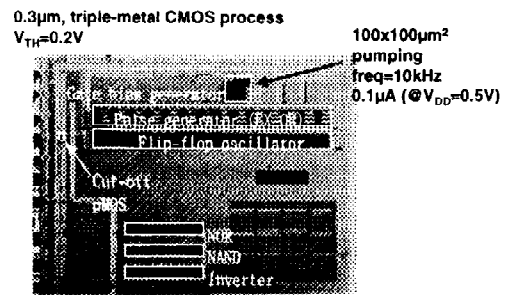


Fig. 13 Super Cut-off CMOS Scheme (SCCMOS)

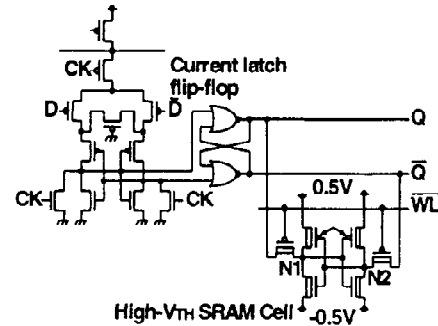


Fig. 14 Maintaining information in standby

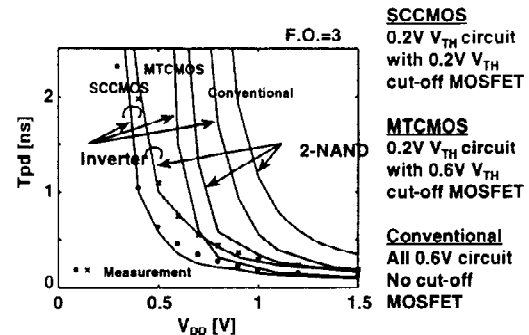


Fig. 15 Delay characteristics (inverter & NAND) of SCCMOS. SCCMOS can push the limit of low-voltage operation down to 0.5V.

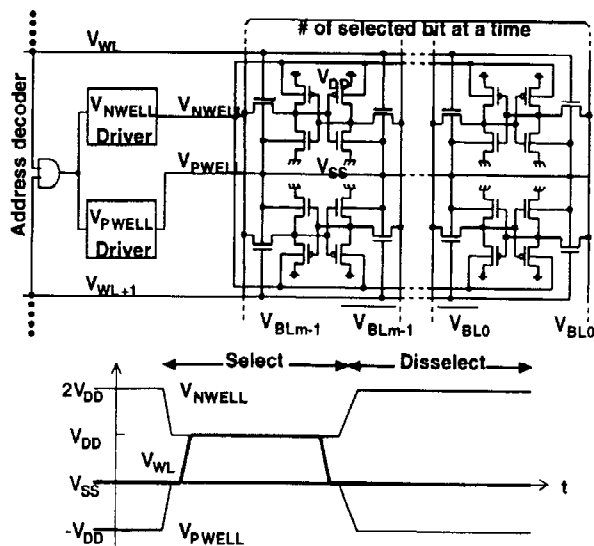


Fig.16 Dynamic Leakage Cut-off SRAM (Ref.5)

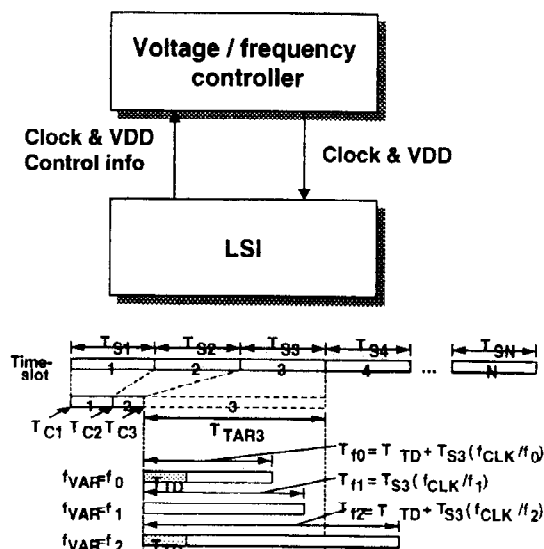


Fig.17 Software feedback loop for low-power (Ref.10)

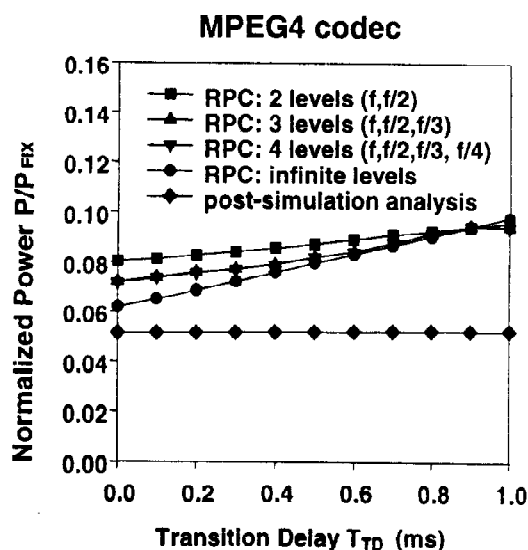


Fig.18 Power saving by software feedback loop. More than an order of magnitude reduction of power is possible with the scheme.

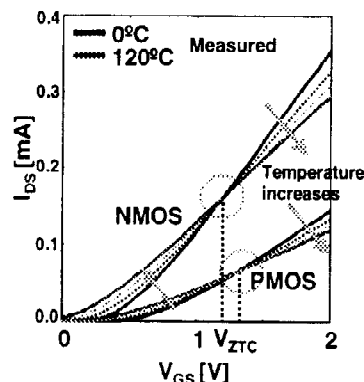


Fig.19 Positive temperature effects on I_{DS} - V_{GS} in sub-1V region (Ref.11)

• α -power law model (T = Temp. μ = Mobility)

$$I_{DS} \propto \mu(T) (V_{DD} - V_{TH}(T))^{\alpha}$$

$$\mu(T) = \mu(T_0) (T/T_0)^{-m}$$

$$V_{TH}(T) = V_{TH}(T_0) - \kappa (T - T_0)$$

Typical Value : $\alpha=1.5$, $m=1.5$, $\kappa=2.5$ [mV/T]

Effects of V_{TH} and μ on I_{DS} when temp. goes up 100[K]

| | V_{TH} effect | μ effect |
|----------------------------|-----------------|--------------|
| $V_{DD}=2.5V, V_{TH}=0.5V$ | 10% ↗ | 35% ↘ |
| $V_{DD}=1.0V, V_{TH}=0.2V$ | 55% ↗ | 35% ↘ |

Fig.20 Temperature dependence of μ and V_{TH}

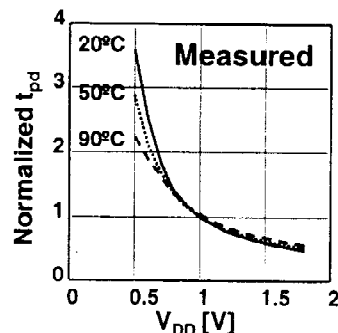


Fig.21 Measurement of 32bit full adder

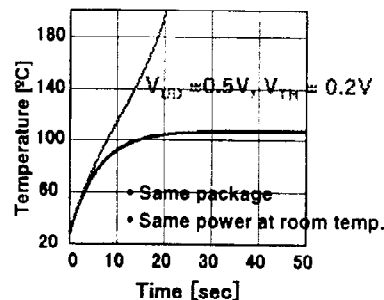


Fig.22 Transient response of chip temperature

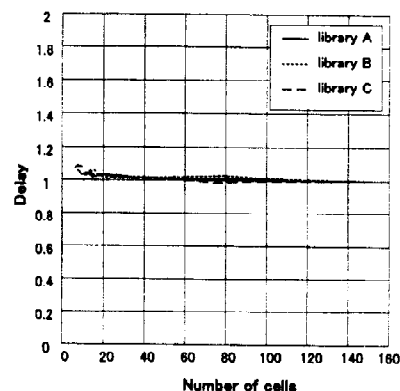


Fig.23 Average of relative delay vs. # of cells (Ref.12)

TABLE I: Contents of 11-cell CyHP library

| | |
|-----------------|------------------------------------|
| Flip-flops | D-FF x1, D-FF x2 |
| Inverters | INV x1, INV x2, INV x4 |
| Primitive gates | 2-NAND x2 2-NOR x2 2-XNOR x1 |
| Compound gates | 2-InvNAND x2 2-InvNOR x2 |
| Multiplexer | 2-MUXInv x1 |

TABLE II: Contents of 20-cell CyHP library

| | |
|-----------------|--|
| Flip flops | D-FFN x1 |
| Inverters | INV x8, INV x16 |
| Primitive gates | 2-NAND x1 2-NOR x1 3-NAND x1 3-NOR x1 |
| Compound gates | 3-AND-NOR x1 3-OR-NAND x1 |

(only cells that not in Table I are listed)

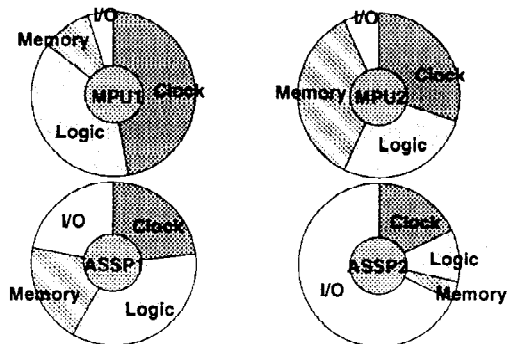


Fig.24 Power distribution in CMOS LSI's

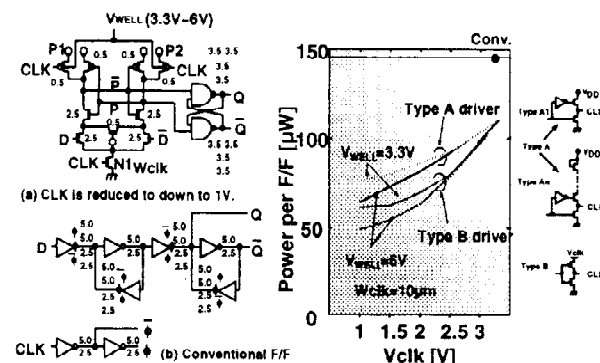


Fig.25 Reduced Clock Swing Flip-Flop (Ref.13)

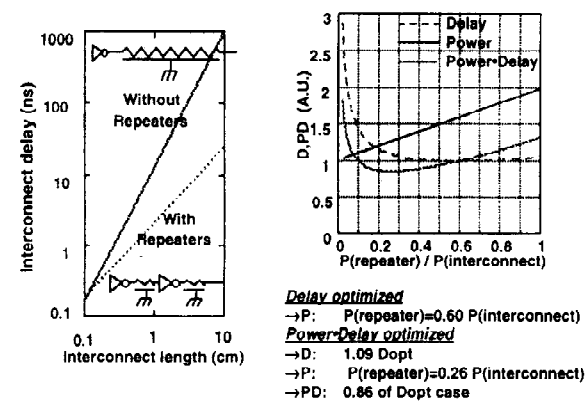
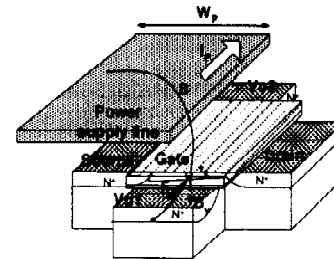


Fig.26 Delay and power optimization for repeaters



- Electrons deflected by B_p .
- Voltage difference between $Vo1$ and $Vo2$.

Fig.27 Lorentz Force MOS (LMOS) (Ref.14)

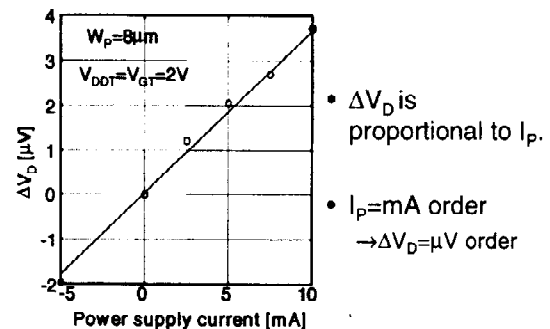


Fig.28 Measured ΔV_D dependence on I_p

Example of MPEG2 decoding

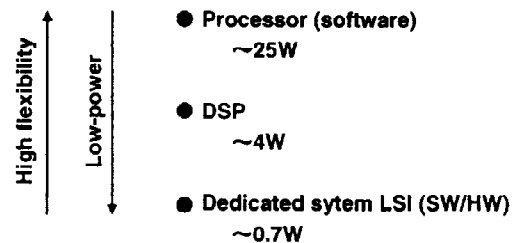


Fig.29 Architectural approach to low-power LSI's

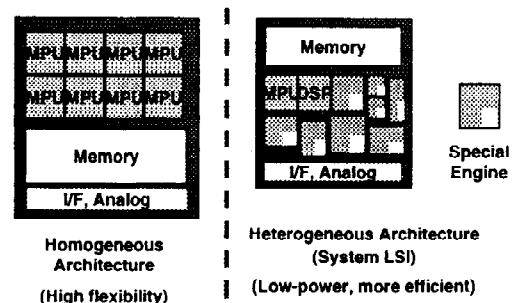


Fig.30 System LSI approach is inherently low-power reducing waste

- NMOS \rightarrow CMOS
Cost up
- Bipolar \rightarrow CMOS
Speed down
- Not cost nor speed but power set the technology trend.
- Integration can achieve low cost and high speed as a system.

Fig.31 What sets the technology trend? Low-power does.