Reducing Power Consumption of CMOS VLSI's through V_{DD} and V_{TH} Control

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Abstract

Lowering operating voltage, V_{DD}, is a key to low-power CMOS digital VLSI's. In order to complete a certain task in a required time and in order to keep leakage current within a tolerable level in the low V_{DD} designs, V_{DD} and V_{TH} control is obligatory. This talk will cover several of the schemes including multi-V_{TH}, variable V_{TH}, multi-V_{DD} and variable V_{DD} to achieve low-power systems. Circuit level ideas to software related research are described.

1. Introduction

Power consumption of the VLSI's has been ever increasing (Fig.1) and a VLSI processor dissipating more than 100W has been introduced. A roadmap is suggesting even more power increase in the future with the supply voltage less than 0.5V (Fig.2). Thus, low-power and low-voltage designs are and will continue to be important for further progress of VLSI's.

2. Power consumption of CMOS VLSI's

The expression for power consumption is shown in Fig.3. The crowbar current component (or short-circuit current component) is less than 10% of total active power at present and will be decreasing in the future when V_{TH}/V_{DD} is increased (Fig.4-7). Consequently, the charging and discharging current component is dominant in an active mode and in a standby mode, leakage current component dominates. In the leakage components, subthreshold current is dominant now but gate tunneling current and gate induced drain leakage should be considered in the future. In calculating the dynamic current component, the voltage dependent gate capacitance should be watched out for (Fig. 8, 9).

Using typical values, power and delay are calculated for various V_{DD} and V_{TH} in Figs. 10 and 11. In order to reduce the power, it is preferable to decrease V_{DD} but decreasing V_{DD} leads to the decrease of performance. When we reduce V_{DD}, if we reduce V_{TH} at the same time, it is possible to maintain the speed of circuits. Then, the issue is the increase of the subthreshold leakage in the low-V_{TH} region. This is the reason why some V_{DD}-V_{TH} control is needed to achieve low-power yet high-speed circuits.

3. Multi-V_{TH}, Variable V_{TH}, Multi-V_{DD} and Variable V_{DD}

Using two V_{TH}'s (MTCMOS) is one idea to take the trade-off between the speed in an active mode and the leakage in a standby mode (Fig.12). The other idea is to vary the V_{TH} dynamically using substrate bias effect, namely VTCMOS, which has been also pursued and productized [8, 9] (Fig.13-15). The comparison of VTCMOS and MTCMOS is tabulated in Fig. 16. MTCMOS is conceptually simple and easy to implement and VTCMOS is better performance-wise. MTCMOS is definitely one way but does not operate properly when V_{DD} decreases below 0.5V. To overcome this shortcoming, Super Cut-off CMOS (SCCMOS) is proposed (Fig.17-20). By over-driving the MOS gate in a standby mode, it is possible to completely cut off the leakage current of low-V_{TH} MOSFET's. The original MTCMOS and VTCMOS are applicable to logic part of the design but are not applicable to low-voltage SRAM's. If MTCMOS is applied to an SRAM, the stored information is lost in a standby. On the other hand, if VTCMOS is applied to an SRAM with low-V_{TH} memory cells for high-speed purpose, the leakage current in an active mode is enormous. A possible solution to this problem is row-wise selective biasing as is shown in Fig.21.

A multiple-voltage scheme known as Dual-VS scheme is shown in Figs. 22 and 24, where critical paths are driven with higher V_{DD}, while non-critical gates are operated under low V_{DD}. An example of

variable V_{DD} approach called software feedback loop is shown in Figs.25-26. Making use of data dependency, an order of magnitude reduction of power is possible with the scheme. This is a hardware-software cooperative approach for low power.

When using sub-0.5V V_{DD} and low-V_{TH}, watch out for the positive temperature dependence of speed (Fig.27-29). Thermal instability may occur when improper package is used (Fig.30). In introducing new circuit concept, layout modification of standard cell library is needed sometimes. It has been shown, however, small number of cells are sufficient in a library to achieve high performance (Fig.31-33, Table I, II).

4. Other low-power approaches

Power consumption of a clock system in a digital VLSI is comparable to the power consumed in other logic gates (Fig.34). In order to reduce the power for clocking, reduced swing clock scheme with special flip-flops has been proposed (Fig.35). In an architectural level, a system LSI approach shows lower power than a general processor approach at the sacrifice of generality and historically low-power has set the technology trend (Fig.36-38).

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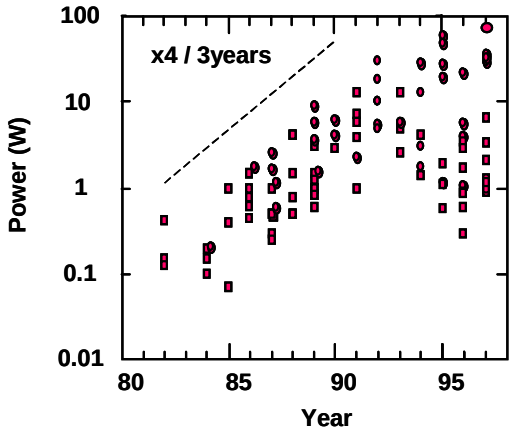


Fig.1 Trend in processor power (from ISSCC)

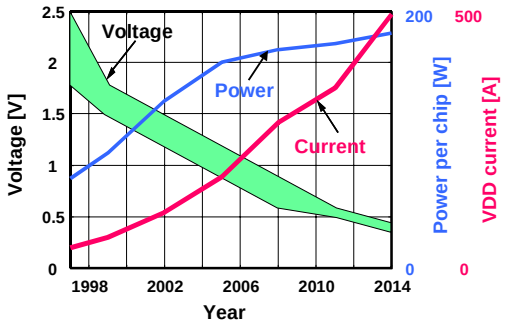


Fig.2 Trend in voltage and power (from SIA)

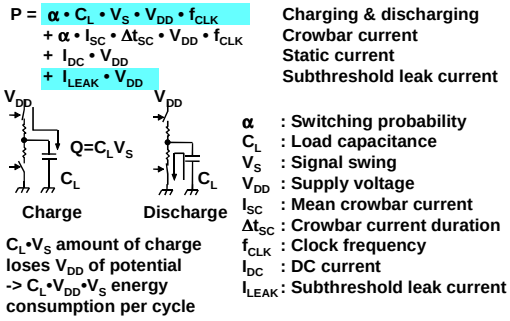


Fig.3 Expression for CMOS power

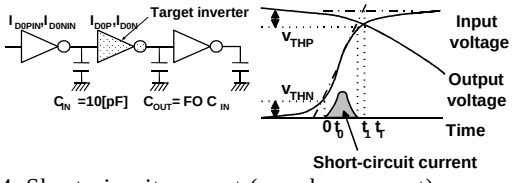


Fig.4 Short-circuit current (crowbar current)

$$P_S = \frac{k(v_{D0P})\, fo_P^2 C_{IN} {V_{DD}}^2}{\frac{v_{D0P} g(v_T,\alpha)}{2k(v_{D0P})} FO\beta_r + h(v_T,\alpha)\, fo_P}$$

$$g(v_T,\alpha) = \frac{\alpha_N + 1}{f(\alpha)} \frac{(1-v_{TN})^{\alpha_N} (1-v_{TP})^{\alpha_P/2}}{(1-v_{TN}-v_{TP})^{\alpha_P/2+\alpha_N+2}} \qquad FO = \frac{C_{OUT}}{C_{IN}} \text{ (Fanout)}$$

$$h(v_T,\alpha) = 2^{\alpha_P}(\alpha_P+1)\frac{(1-v_{TP})^{\alpha_P}}{(1-v_{TN}-v_{TP})^{\alpha_P+1}}$$

$$k(v_{D0P}) = \frac{0.9}{0.8} + \frac{v_{D0P}}{0.8} \ln \frac{10 v_{D0P}}{e} \qquad fo_P = \frac{I_{D0P}}{I_{D0PIN}} \quad \beta_r = \frac{I_{D0P}}{I_{D0N}}$$

Fig.5 Expression for short-circuit power (Ref.1)

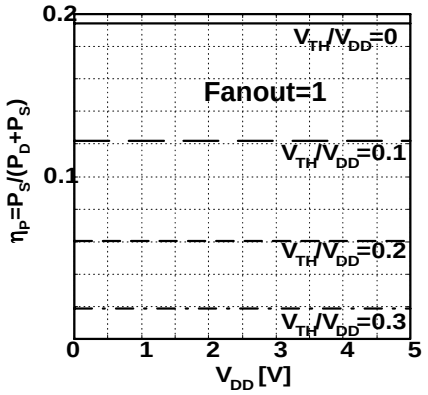


Fig.6 Ratio of short-circuit power (P_S) vs total active power ($P_S + P_D$)

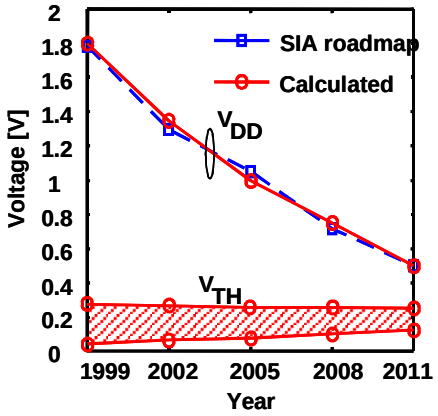


Fig. 7 Optimum V_{DD} and V_{TH} (Ref.2)

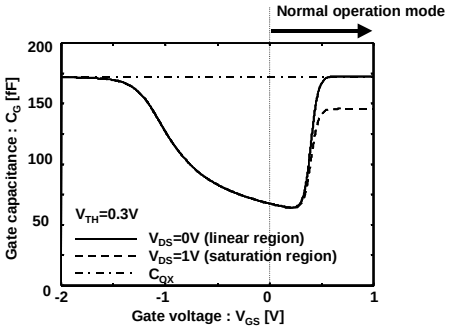


Fig.8 Voltage dependent gate capacitance (Ref.7)

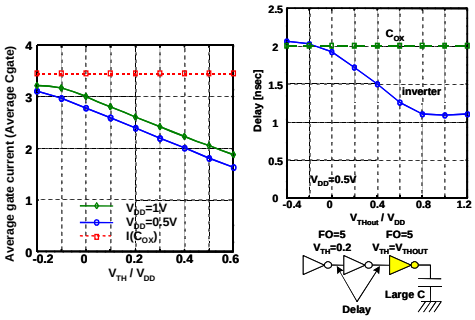


Fig9 Effect of voltage dependent gate capacitance

$$\text{Power}: \quad P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{th}}{S}} \cdot V_{DD}$$

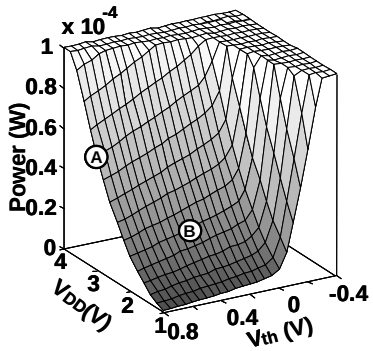


Fig.10Power dependence on V_{DD} & V_{TH}

$$\text{Delay} = \frac{k \cdot Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^{\alpha}} \quad (\alpha=1.3)$$

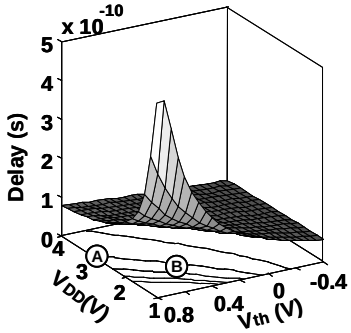
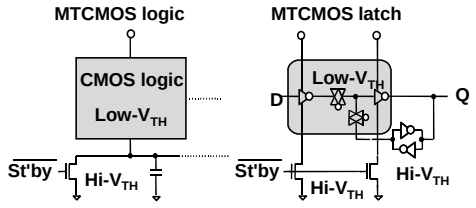


Fig.11Delay dependence on V_{DD} & V_{TH}



- In active mode, low-V_{TH} MOSFET's achieve high speed.
- In standby mode when St'by signal is high, high-V_{TH} MOSFET's in series to normal logic circuits cut off leakage current.

Fig.12Multi-Threshold CMOS (MTCMOS) (Ref.3)

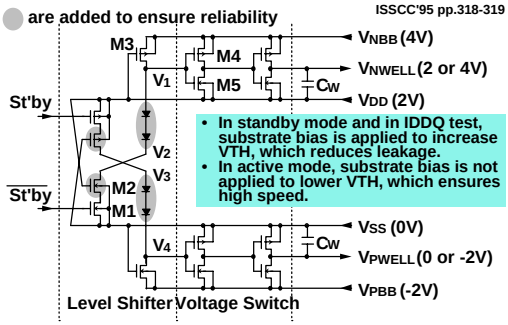
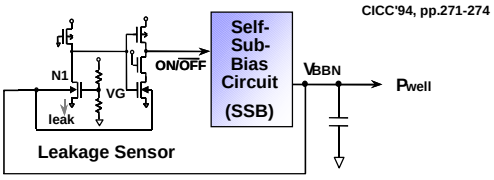


Fig.13 Stanby Power Reduction circuit(SPR). Part of Variable Threshold CMOS (VTCMOS)



- control Vth to adjust leakage current
- compensate Vth fluctuation

Fig.14 Self-Adjusting Threshold-voltage Scheme (SATS). Part of Variable Threshold CMOS (VTCMOS)

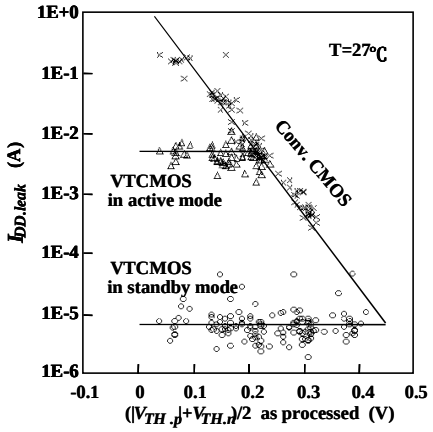


Fig.15Measurement on VTCMOS

	Variable VTH	Multi-VTH
Principle	n-well, V_{DDL}, Low-Vth, VT control, GND, p-well	V_{DD}, Low-Vth, St'by, GND, Hi-Vth
	Threshold control with sub-bias	On-off control of internal VDD/VSS
Merit/ Demerit	+ Low leakage in standby + Already productized + Compensate Vth fluctuation + I_{DDQ} test + No serial MOSFET + Conventional design env. + Conventional F/F's - Triple well is desirable - Scalability? (junction leakage)	+ Low leakage in standby + Already productized - Compensate Vth fluctuation - I_{DDQ} test - Large serial MOSFET slower, larger, lower yield... + Conventional design env. - Special F/F's, Two V_{TH}'s - Ultra-low voltage region? - Delay fluctuates on activity

Fig.16Comparison between VTCMOS & MTCMOS

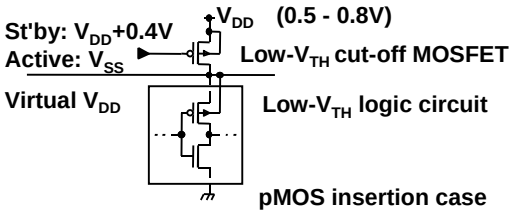


Fig.17Concept of Super Cut-off CMOS (SCCMOS) (Ref.4)

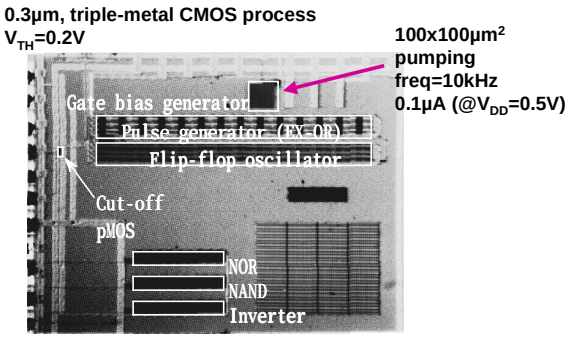


Fig.18Super Cut-off CMOS Scheme (SCCMOS)

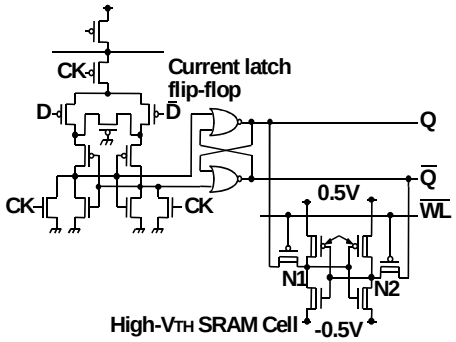


Fig.19Maintaining information in standby

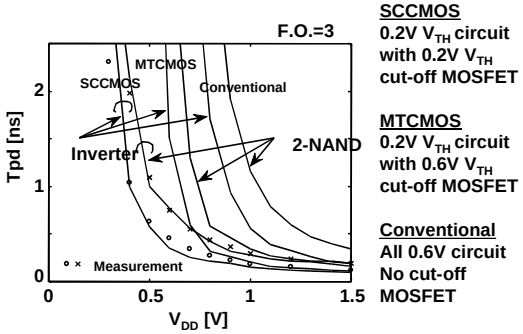


Fig.20Delay characteristics (inverter & NAND) of SCCMOS. SCCMOS can push the limit of low-voltage operation down to 0.5V.

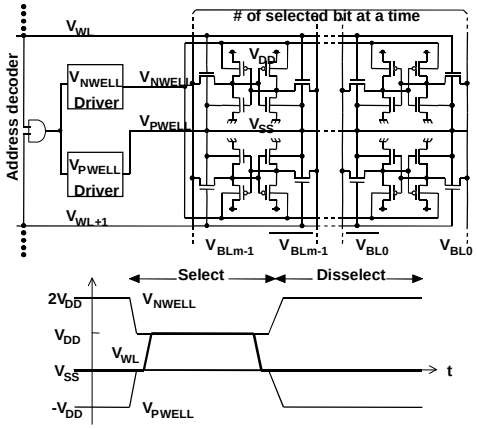


Fig.21Dynamic Leakage Cut-off SRAM (Ref.5)

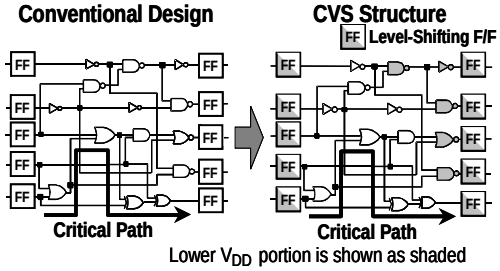


Fig.22Clustered Voltage Scaling for Multiple VDD's. Dual voltage supply scheme (Dual-VS) (Ref.6)

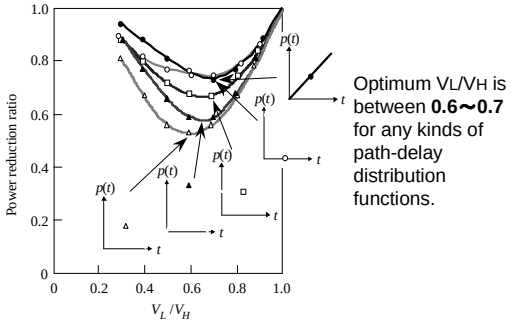


Fig.23Power Reduction vs. V_L/V_H

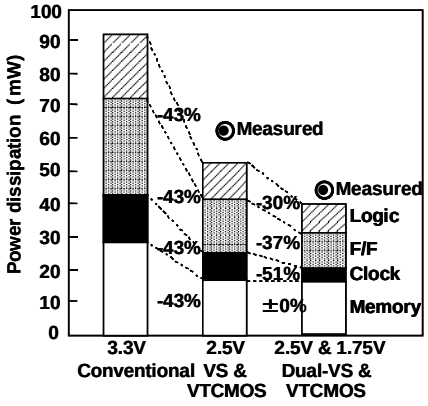


Fig.24Power reduction by Dual-VS

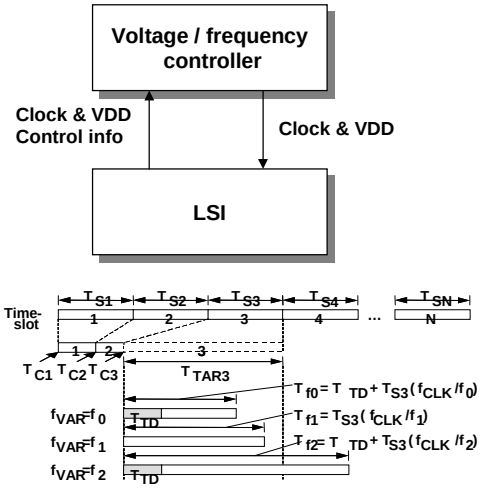


Fig.25Software feedback loop for low-power (Ref.10)

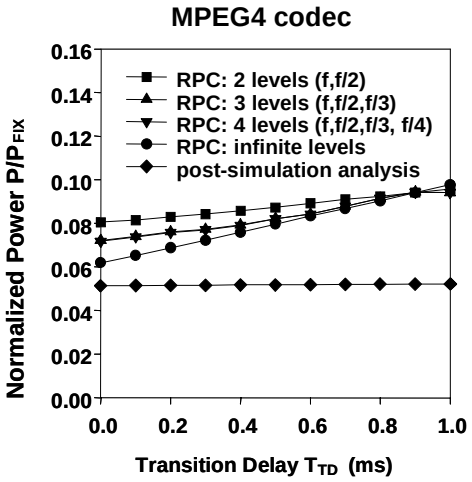


Fig.26Power saving by software feedback loop. More than an order of magnitude reduction of power is possible with the scheme.

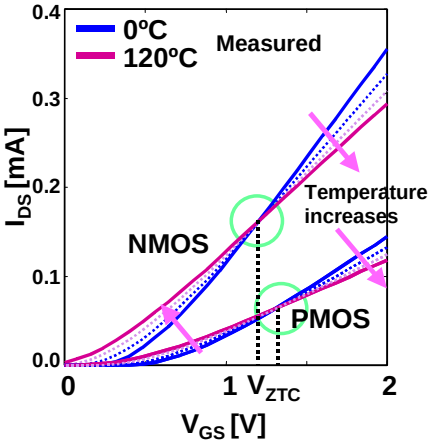


Fig.27Positive temperature effects on I_{DS}- V_{GS} in sub-1V region (Ref.11)

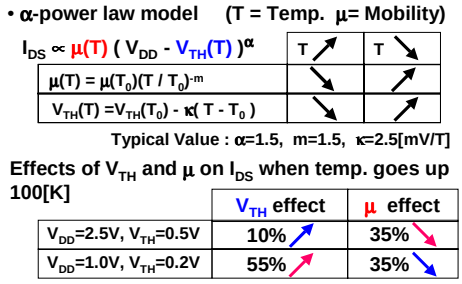


Fig.28Temperature dependence of μ and V_{TH}

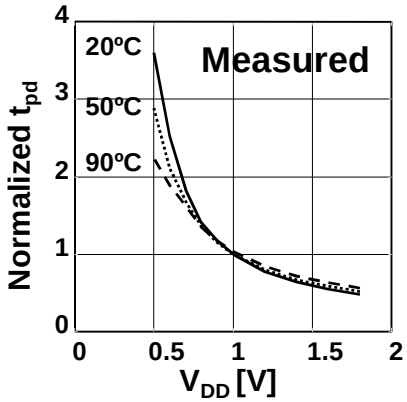


Fig.29Measurement of 32bit full adder

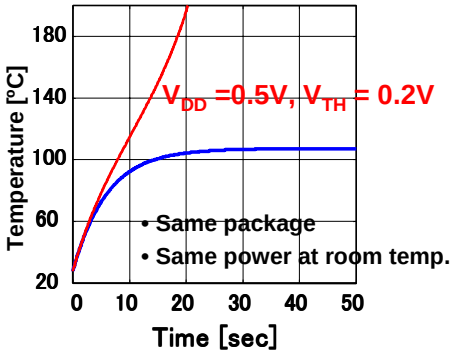


Fig.30Transient response of chip temperature

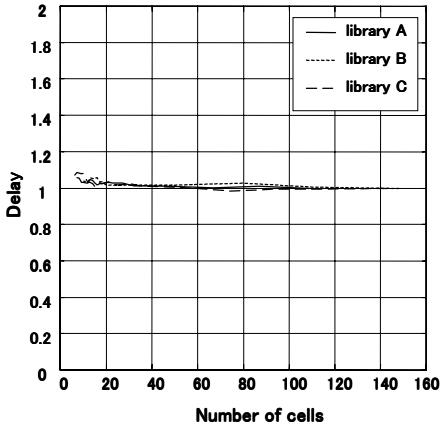


Fig.31Average of relative delay vs. # of cells (Ref.12)

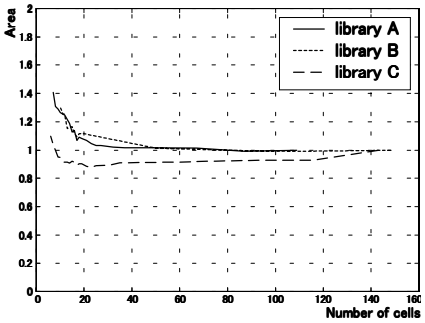


Fig.32Average of relative area vs. number of cells

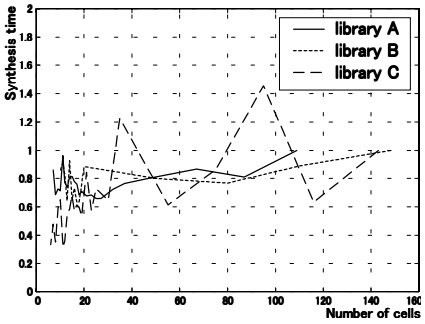


Fig.33Relative synthesis time vs. # of cells.

TABLE I: Contents of 11-cell CyHP library

Flip-flops	D-FF x1, D-FF x2
Inverters	INV x1, INV x2, INV x4
Primitive gates	2-NAND x2 2-NOR x2 2-XNOR x1
Compound gates	2-InvNAND x2 2-InvNOR x2
Multiplexer	2-MUXInv x1

TABLE II: Contents of 20-cell CyHP library

Flip flops	D-FFN x1
Inverters	INV x8, INV x16
Primitive gates	2-NAND x1 2-NOR x1 3-NAND x1 3-NOR x1
Compound gates	3-AND-NOR x1 3-OR-NAND x1

(only cells that not in Table I are listed)

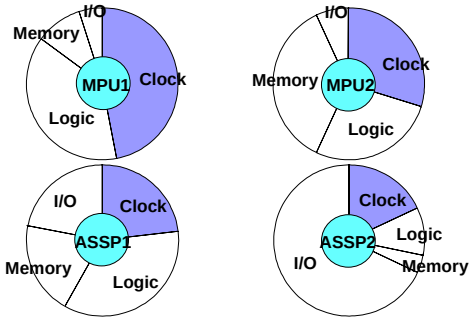


Fig.34Power distribution in CMOS LSI's

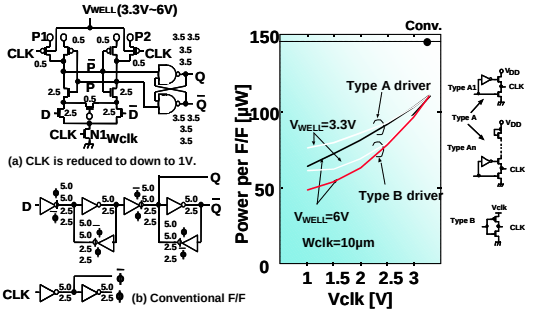


Fig.35Reduced Clock Swing Flip-Flop (Ref.13)

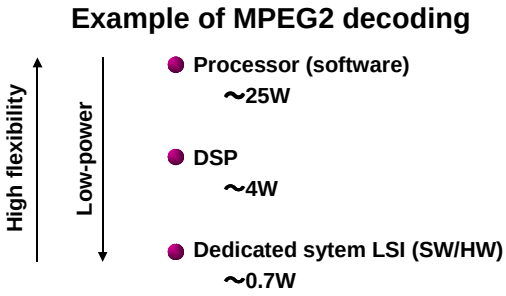


Fig.36Architectural approach to low-power LSI's

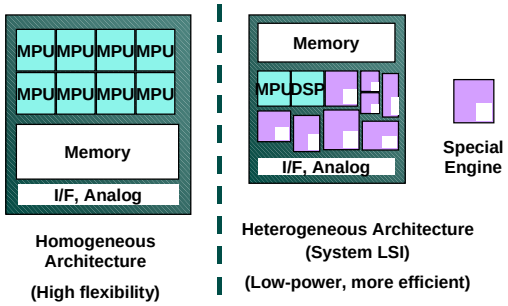
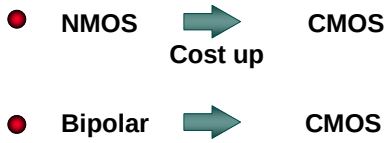
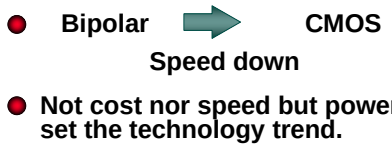


Fig.37System LSI approach is inherently low-power reducing waste





- **Not cost nor speed but power set the technology trend.**
- **Integration can achieve low cost and high speed as a system.**

Fig.38What sets the technology trend? Low-power does.