Voltage Dependent Gate Capacitance and its Impact in Estimating Power and Delay of CMOS Digital Circuits with Low Supply Voltage

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ABSTRACT

Gate capacitance has complex voltage dependency on terminal voltages but the impact of this voltage dependency of gate capacitance on power and delay has not been fully investigated, especially, in low-voltage, low-power designs. Introducing an effective gate capacitance, $C_{G,eff}$, it is shown that the power and delay of CMOS digital circuit can be estimated accurately. $C_{G,eff}$ is a strong function of V_{TH}/V_{DD} and V_{TH}/V_{DD} tends to increase in low-voltage region. Hence, the effective capacitance relative to oxide capacitance, C_{OX}, is decreasing in low-voltage, low-power designs. Therefore, considering $C_{G,eff}$ in accurate power and delay estimation becomes more important in the future.

Keywords

Gate capacitance, low supply voltage, low-power design.

1. Introduction

Capacitance plays an important role in estimating power and delay of CMOS digital VLSI's. Load capacitance of CMOS circuits, C_{LOAD}, which determines the power and delay is expressed as follows.

$$C_{LOAD} = \sum C_G + \sum C_J + \sum C_{INT} , \quad (1)$$

where C_G, C_J and C_{INT} denote gate, junction and interconnection capacitance, respectively. In these capacitances, C_G and C_J have complex voltage dependency on terminal voltages but the impact of this voltage dependency of C_G and C_J on power and delay has not been fully investigated, especially, in low-voltage, low-power designs. In this paper, the effect of the voltage dependent gate capacitance on circuit behaviors is analyzed and an appropriate choice of the effective constant gate capacitance is discussed. The impact of the voltage dependent nature is investigated for low-voltage, low-power designs.

2. Voltage dependent capacitance of MOSFET

Gate capacitance seen from the input, C_G, is a function of terminal voltages as is shown in Fig. 1. C_G is not equal to C_{OX}, which is calculated from oxide thickness and is constant. In a subthreshold region, C_G is much smaller than C_{OX} and in an on-state, C_G is different between a linear region and a saturation region. If a CMOS inverter is formed, the input capacitance changes as in Fig. 2. In calculating the capacitance, the current flown into a gate terminal is integrated over time. It is obvious that the behavior of C_G changes depending on the threshold voltage. Since C_G is always smaller than C_{OX} and shows the minimum just before the threshold voltage, the effect of C_G is expected to decrease when V_{TH}/V_{DD} gets larger.

There is also a gate-drain overlap capacitance, C_{OV}, associated with a MOSFET. Since the overlap capacitance is not voltage dependent, it is not considered in this paper. The overlap capacitance effect can be considered by just adding $2C_{OV}$ in an estimation process.

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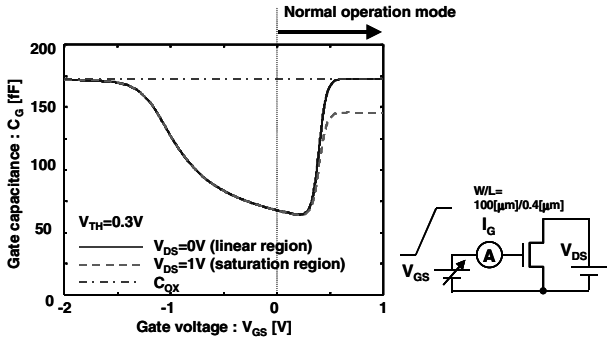

Fig. 1 Dependence of gate capacitance on gate and drain voltage

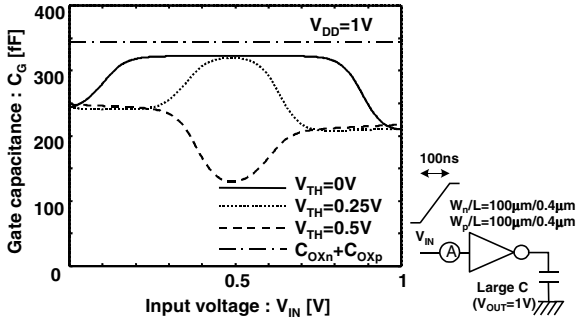

Fig. 2 Dependence of inverter input capacitance on gate voltage and threshold voltage

3. Definition of effective gate capacitance

Let us consider an NMOS case for simplicity. An extension to a PMOS case is straightforward. Considering an inverter turning on, in an initial state, V_{GS} is 0 and V_{DS} is V_{DD} and V_{GS} reaches

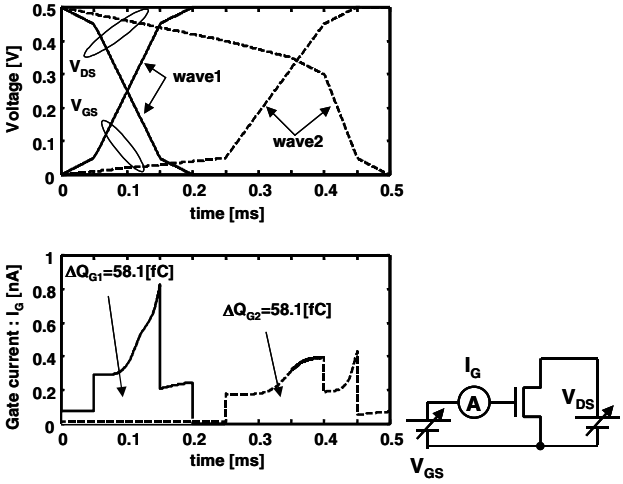

Fig. 3 Method to obtain $C_{G,eff}$ and ΔQ_G dependence on the waveforms of gate voltage and drain voltage

V_{DD} and V_{DS} reaches 0 at a final state. Considering this situation, let us define an effective gate capacitance, $C_{G,eff}$, as follows.

$$C_{G,eff} = \frac{\Delta Q_G}{V_{DD}} = \frac{1}{V_{DD}}\{Q_G(V_{GS}=V_{DD}, V_{DS}=0, V_{BS}=0) - Q_G(V_{GS}=0, V_{DS}=V_{DD}, V_{BS}=0)\} \quad (2)$$

Q_G is charge stored on a gate and ΔQ_G is gate charge difference between the final state and the initial state. This amount of charge should be poured into a gate terminal in circuit operation, which determines power and delay of digital circuits.

In calculating ΔQ_G, the current flown into a gate terminal can be integrated over time as is shown in Fig.3. As is seen from the same figure, ΔQ_G is not path dependent so that any waveforms for V_{GS} and V_{DS} can be used to obtain ΔQ_G.

It should be noted that $C_{G,eff}$ is defined for an NMOS and a PMOS transistor. Thus, the number of simulations needed to extract $C_{G,eff}$ for an LSI is limited to the number of kinds of transistors in a design, which is usually two or a little more for most digital designs. Input gate capacitance of a complex gate can be calculated by adding $C_{G,eff}$ of MOSFET's.

Junction capacitance is also voltage dependent but it is a two-terminal device and the definition of the effective capacitance, $C_{J,eff}$, is trivial as follows.

$$C_{J,eff} = \frac{1}{V_{DD}}\int_0^{V_{DD}} C_J(V)dV = \frac{Q_J(V_{DD}) - Q_J(0)}{V_{DD}} = \frac{\Delta Q_J}{V_{DD}} \quad (3)$$

ΔQ_J is not dependent on voltage wave shape and well-defined.

4. Application of effective gate capacitance

The effective gate capacitance, $C_{G,eff}$, is applied to estimate power and delay of a CMOS inverter in Figs. 4 and 5. Power and delay simulated by using constant C_{OX} and $C_{G,eff}$ as gate capacitance are denoted as $P(C_{OX})$, $t_d(C_{OX})$, $P(C_{G,eff})$, and $t_d(C_{G,eff})$, respectively. Power and delay simulated by using real MOS gate is denoted as P(MOS) and t_d(MOS), which are supposed to be true. Two different device models are used to check the effectiveness of the proposed $C_{G,eff}$. Both models are based on BSIM model and charge conservation in capacitance

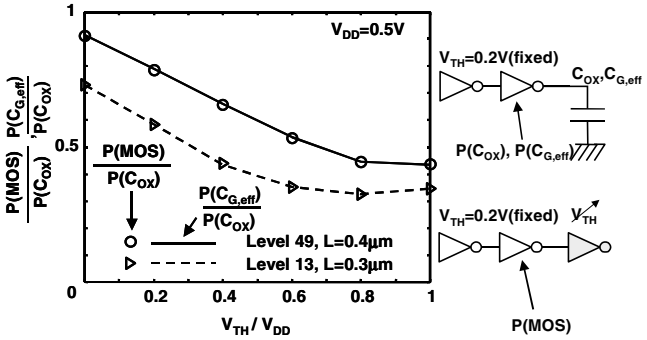

Fig. 4 Comparison of power estimated by using $C_{G,eff}$ ($P(C_{G,eff})$), C_{OX} ($P(C_{OX})$)and real MOS gate (P(MOS))

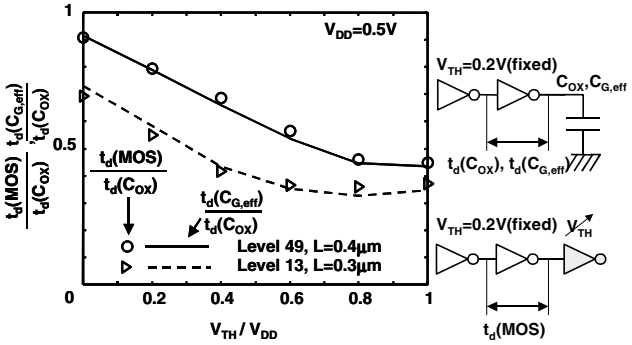

Fig. 5 Comparison of delay estimated by using $C_{G,eff}$ ($t_d(C_{G,eff})$), C_{OX} ($t_d(C_{OX})$)and real MOS gate (t_d(MOS))

models is observed [2]. In order to concentrate on the gate capacitance effect, C_J and C_{INT} are set zero in the simulations.

$P(MOS)/P(C_{OX})$ and $t_d(MOS)/t_d(C_{OX})$ are less than 0.5 when V_{TH}/V_{DD} is above 0.6. This means that constant C_{OX} approximation for a gate capacitance becomes poor when V_{TH}/V_{DD} increases. The discrepancy is mainly due to the smaller capacitance in the subthreshold region. If we use $C_{G,eff}$ instead of C_{OX}, $P(C_{G,eff})$ and $t_d(C_{G,eff})$ can reproduce P(MOS) and t_d(MOS) well.

In order to check the validity of the $C_{G,eff}$ approximation, a more complex circuit, 4-bit counter, is analyzed. Again, simulations are carried out using $C_{G,eff}$, C_{OX} and real MOS gate for gate capacitances. Circuits shown in Fig.6 are adopted to represent three cases. Each gate in a counter is substituted by one of the three types of gates. The results are shown in Fig. 7. In both power and delay comparison, $C_{G,eff}$ reproduce well the real gate for gate capacitance, while C_{OX} approximation gives larger power and delay by a factor of more than two.

Slight disagreement in power and delay between $C_{G,eff}$ approximation and the MOS gate simulation is due to the fact that the operation of MOSFET does not always start with V_{GS} =0 and V_{DS} = V_{DD} and end with V_{GS} =V_{DD} and V_{DS} = 0. This situation is observed in series connected MOS structures in NAND and other complex gates. The disagreement is also due to the substrate bias effect in the stacked structure. It can be said, however, that the disagreement is small and using $C_{G,eff}$ is much more accurate than to use C_{OX} as a constant capacitance in estimating power and delay.

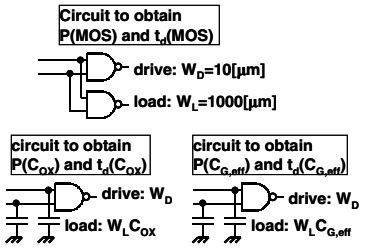

Fig. 6 Circuit to simulate effect of substituting real MOS gate capacitance by C_{OX} and $C_{G,eff}$

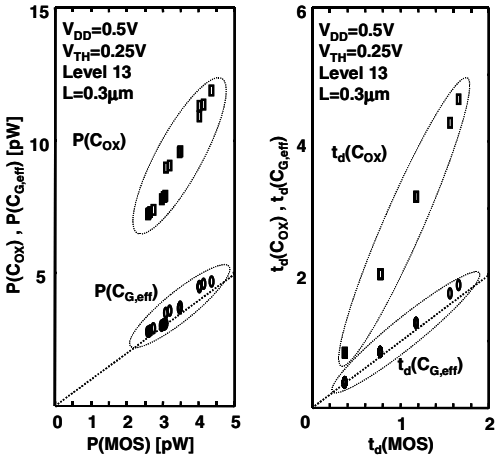

Fig. 7 Dynamic power dissipation and delay of 4-bit counter

5. Discussion

A future trend of an optimum threshold voltage has been discussed in a previous publication [3]. The trend in optimum V_{TH} is calculated using the device parameters given in the ITRS Roadmap[6]. Figure 8 shows the calculated result of the trend of the optimum threshold voltage. Supply voltage, V_{DD}, will be decreased in the future to cope with the power increase problem and to guarantee sufficient reliability. Low V_{DD} is also used for achieving low-power CMOS VLSI's. The threshold voltage, however, cannot be decreased with the same rate as V_{DD} decreases due to the exponential increase of subthreshold leakage. As a result, V_{TH}/V_{DD} tends to increase in the future and the discrepancy between $C_{G,eff}$ and C_{OX} gets bigger.

Although CAD tools take the voltage dependent capacitance effect correctly, designers use C_{OX} instead of $C_{G,eff}$ as an effective gate capacitance from time to time and it seems working well at present. This is because V_{TH}/V_{DD} is about 0.15 and the discrepancy between $C_{G,eff}$ and C_{OX} is about 10%, that is, small.

Moreover, although the power and delay are estimated a little larger than reality, this effect is being canceled out by neglecting short-circuit current component which tends to increase the delay and the power by about 10% [4]. In low-voltage designs, however, V_{TH}/V_{DD} becomes larger and the short-circuit current tends to diminish while the discrepancy between $C_{G,eff}$ and C_{OX} tends to increase. Then the cancellation does not take place. Consequently, the constant capacitance approximation using C_{OX} becomes less and less accurate and $C_{G,eff}$ should be used instead in the future.

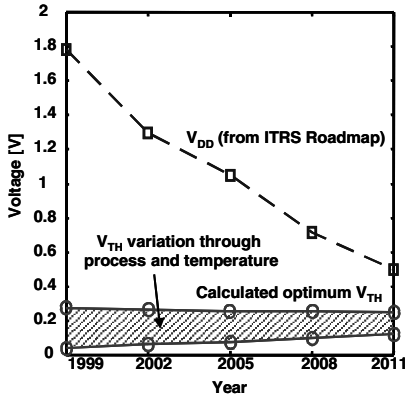

Fig. 8 Future trend of optimum V_{DD} and V_{TH}[4]

C_{INT} is dominant in C_{LOAD} in many cases, and in that situation, the accuracy of the gate capacitance approximation is less important but there are cases where C_{INT} is small and gate capacitance affects the circuit behavior much like in some hand crafted data-path circuits.

6. Conclusion

Appropriate effective gate capacitance, $C_{G,eff}$, has been defined and a method is proposed to extract the value by using SPICE. It is shown that the power and delay of CMOS digital circuit can be estimated accurately by introducing $C_{G,eff}$. $C_{G,eff}$ helps designers give insights into the circuit behavior more accurately. Since $C_{G,eff}$ is V_{TH} dependent so is the power. This is one source of fluctuation in power for mass produced VLSI's.

The discrepancy between $C_{G,eff}$ and C_{OX} is increasing in low-voltage regime and adopting $C_{G,eff}$ in accurate power and delay estimation becomes more important in the future.

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