Interconnection from Design Perspective

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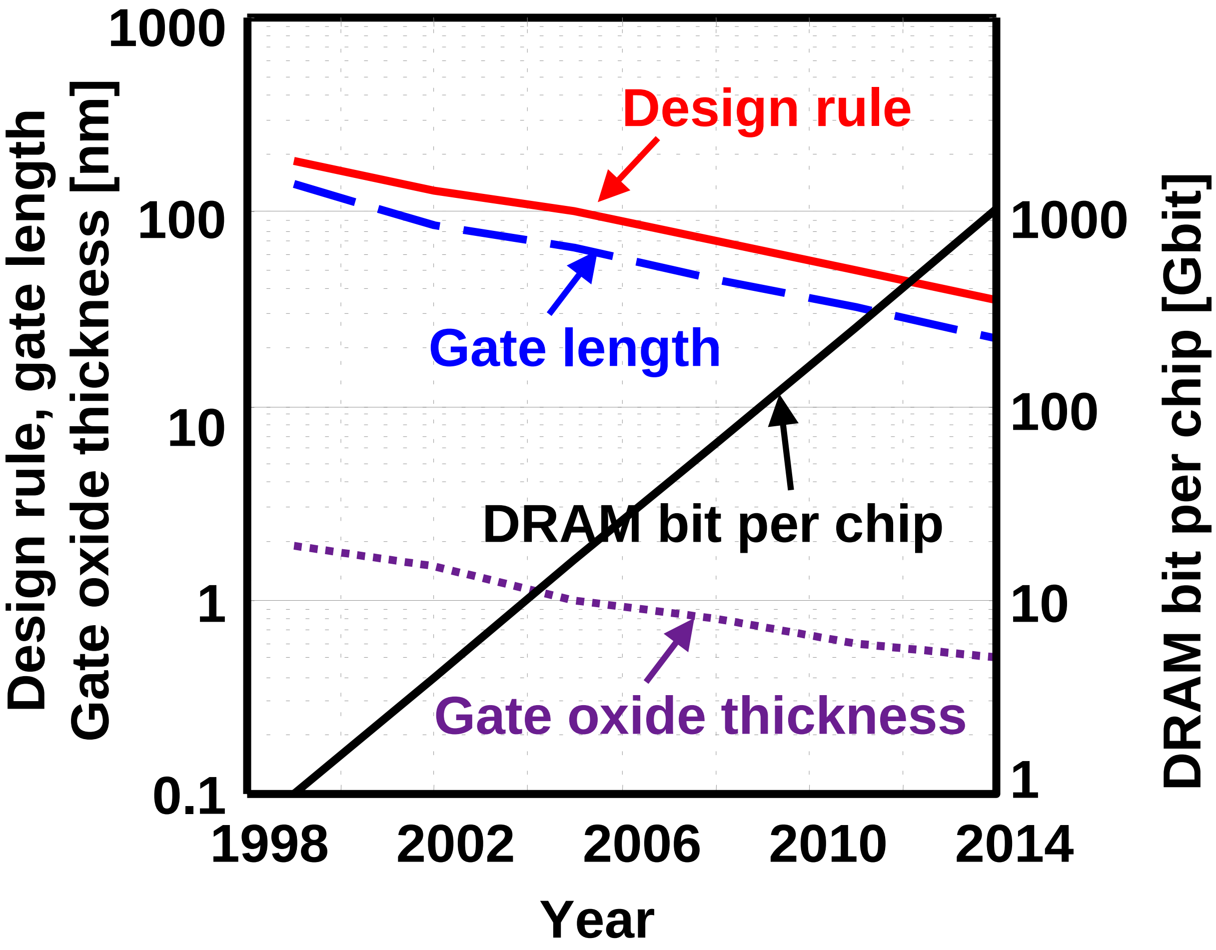
Moore's Law

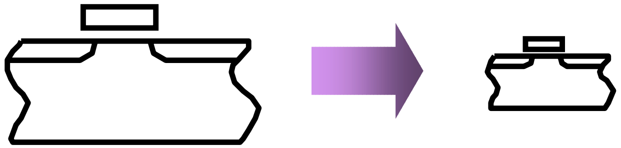


Design rule
Gate length
DRAM bit per chip
Gate oxide thickness
1000
100
10
1
0.1
1000
100
10
1
1998
2002
2006
2010
2014
Year
Design rule, gate length
Gate oxide thickness [nm]
DRAM bit per chip [Gbit]

Scaling Law

Transistors		Scaling coefficients
V_{DD}	[V]	1/k
Tr. dimensions	[x]	1/k
Drain current	[I~1/x x/x V^1.3]	$1/k^{0.3}$
Gate capacitance	[C~1/x xx]	1/k
Tr. delay	[d~CV/I]	$1/k^{1.7}$
Tr. power	[P~VI~CVV/d]	$1/k^{1.3}$
Power density	**[p~P/x/x]**	**$k^{0.7}$**
Tr. density	**[n~1/x/x]**	**k^2**

Interconnects			
Type		**Local**	**Global**
Scaling scenario		**Scaled**	**Anti-scaled**
Line thickness	[T]	1/k	k
Width	[W]	1/k	k
Separation	[S]	1/k	k
Oxide thickness	[H]	1/k	1
Length	[L]	1/k	1
Resistance	[R_{INT}~L/W/T]	k	$1/k^2$
Capacitance	[C_{INT}~LW/H]	1/k	k
RC delay/Tr. delay	**[D~$R_{INT}C_{INT}$/d]**	**$k^{1.7}$**	–
Current density	**[J~pWL/V /W/T]**	–	**$k^{0.7}$**
DC noise / V_{DD}	**[N~JWTR/V]**	–	**$k^{1.7}$**

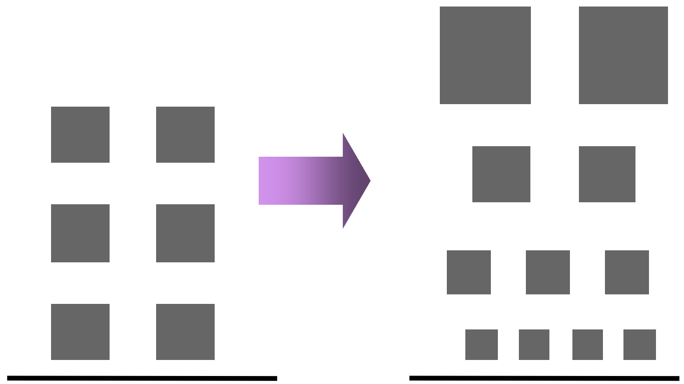


K=2

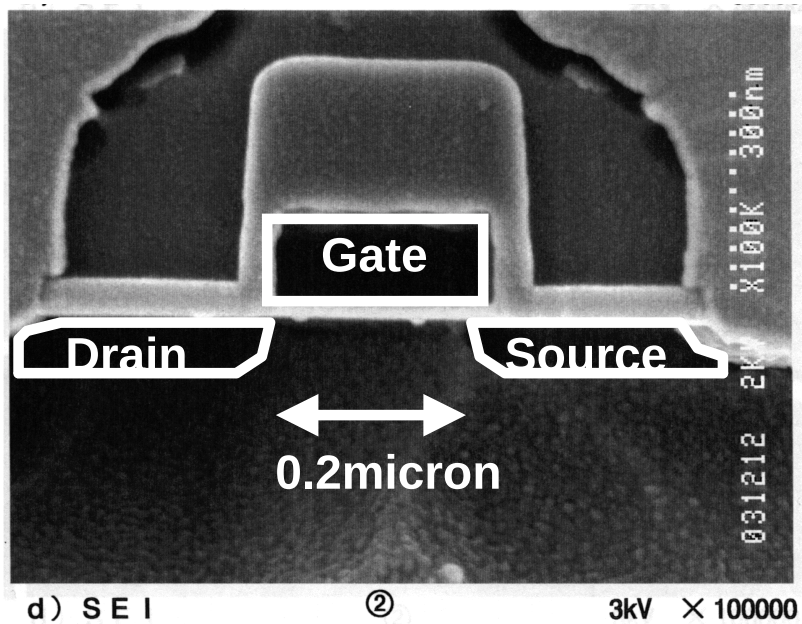
$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)\frac{(V_{gs}-V_t)^{\alpha}}{2} \sim [V^{\alpha}/t]$$

$$\alpha = 1.3$$

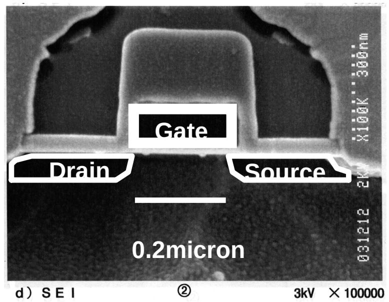
T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no,2, pp.584-594, Apr. 1990.



Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

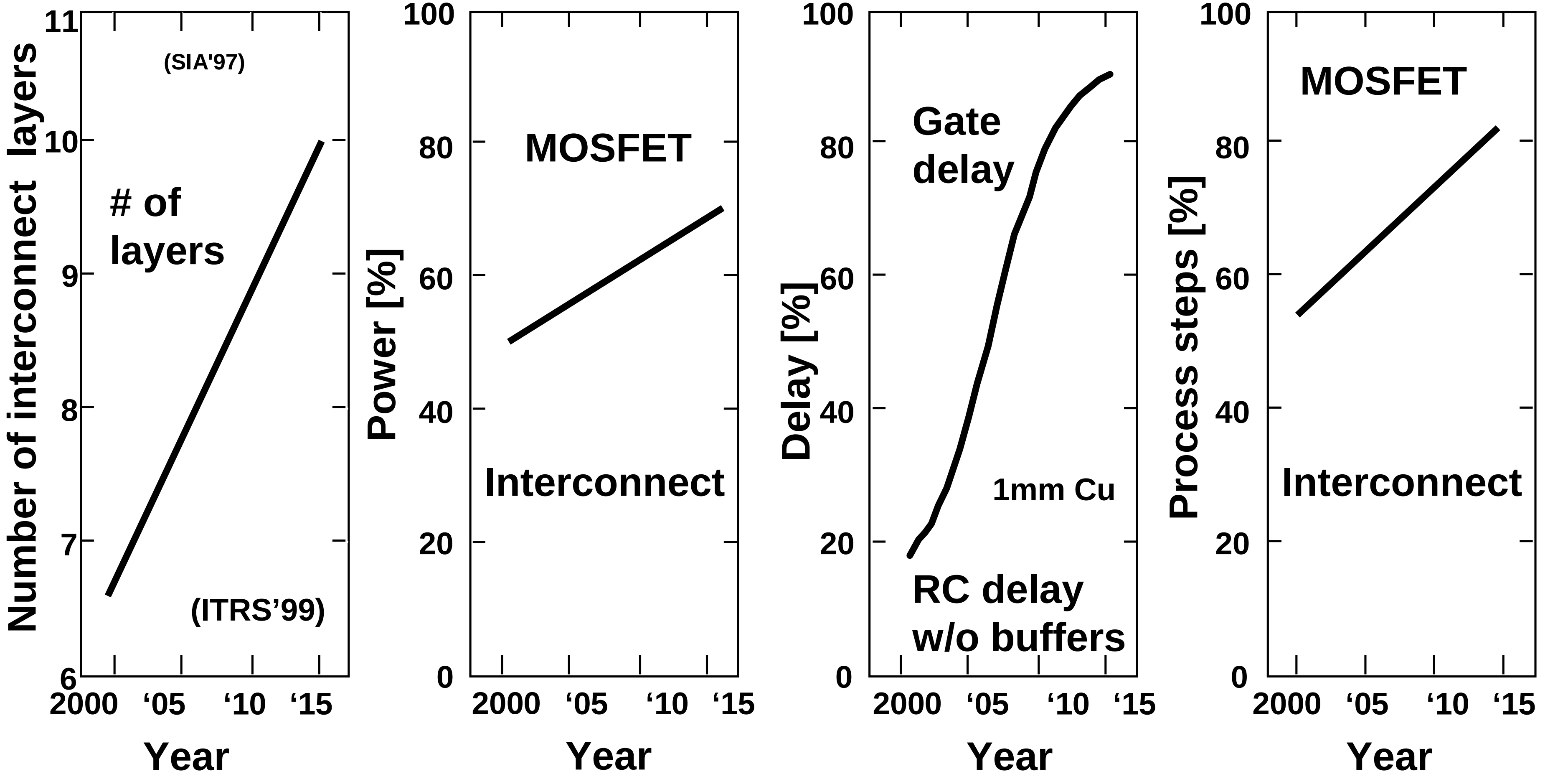
Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



DSM interconnect design issues

<u>**Larger current**</u>

- **IR drop (static and dynamic)**
- **Reliability (electro-migration)**

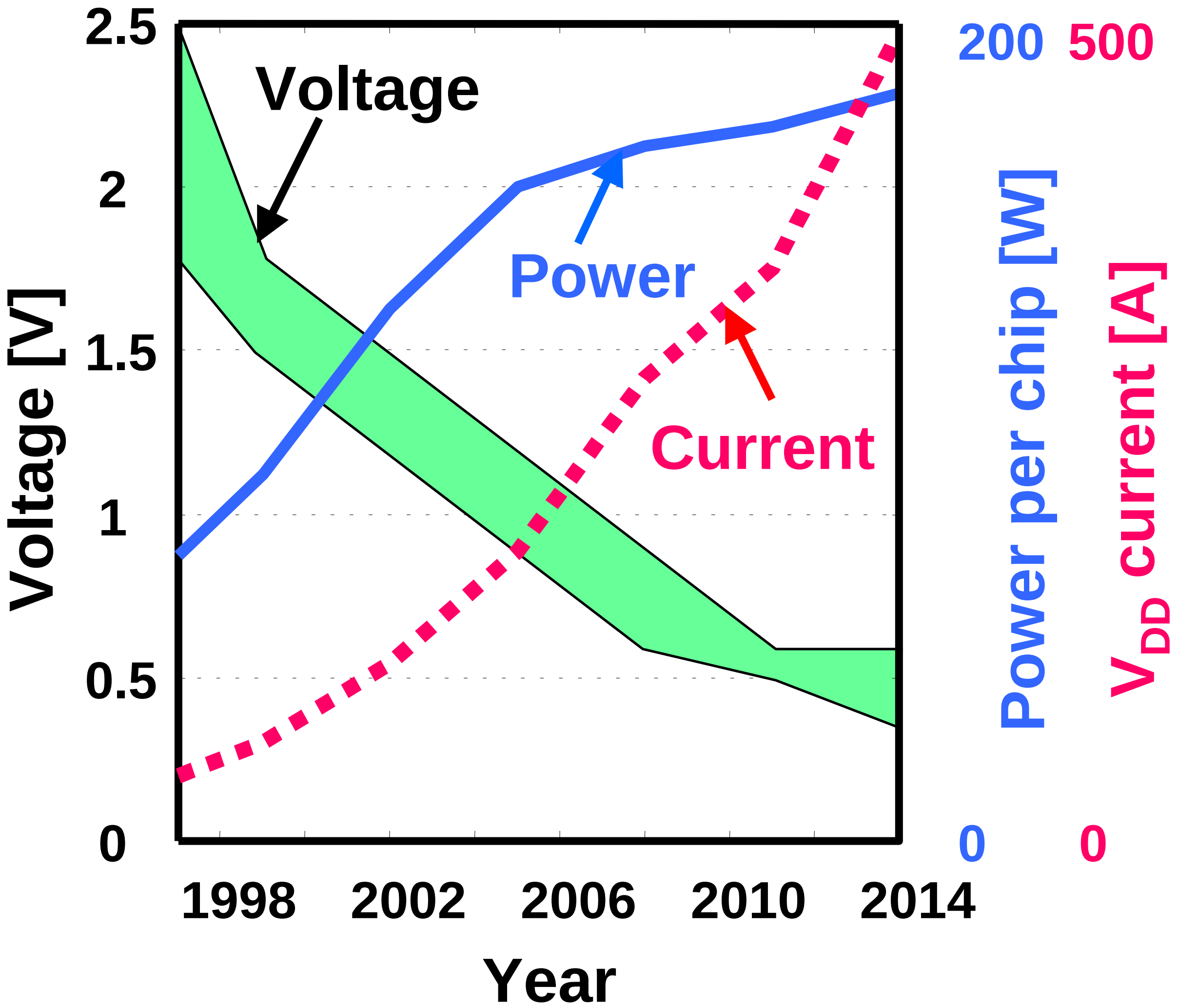
<u>**Smaller geometry / Denser pattern**</u>

- **RC delay**
- **Signal Integrity**
- **Crosstalk noise**
- **Delay fluctuation**

<u>**Higher speed**</u>

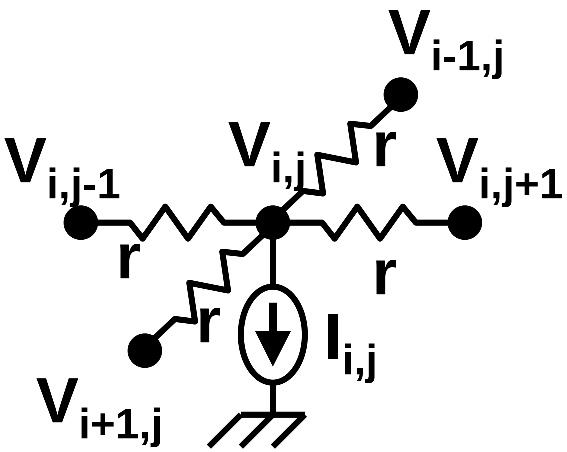
- **Inductance**
- **EMI**

VDD, Power and Current Trend

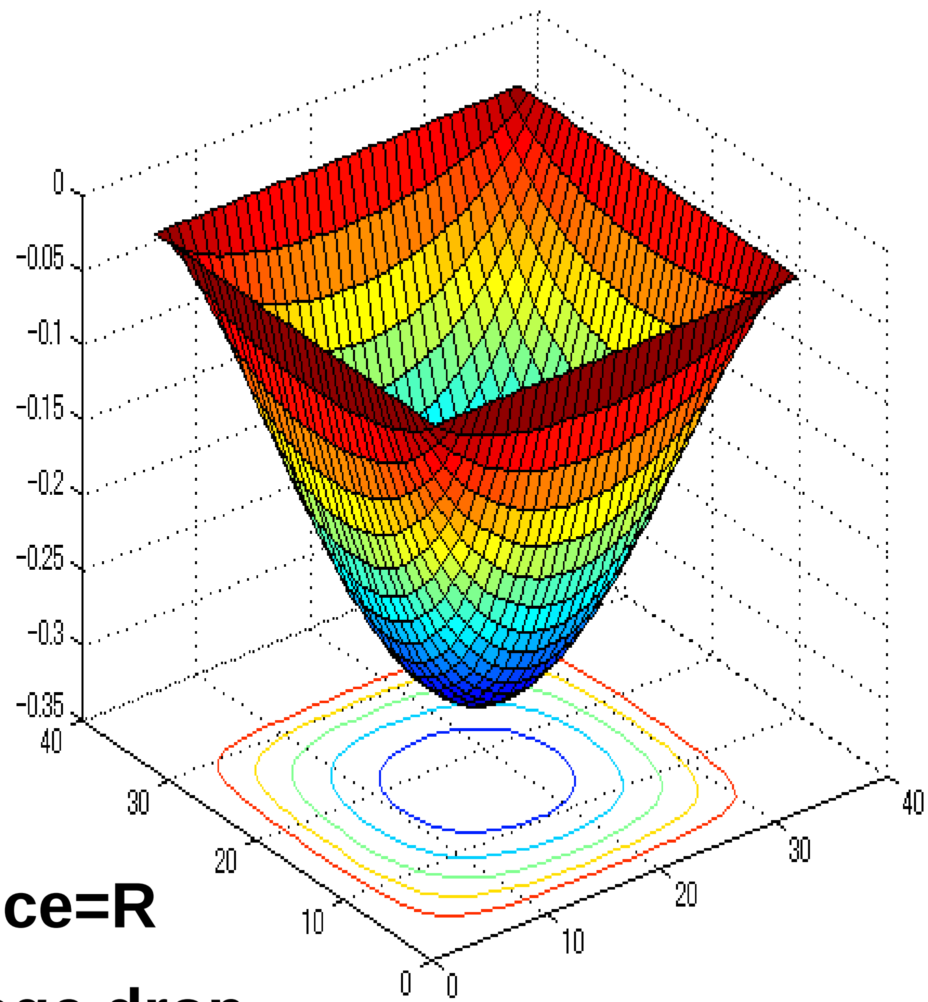


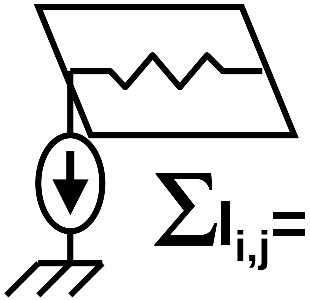
International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

IR Drop



$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\ I_{i,j}$$



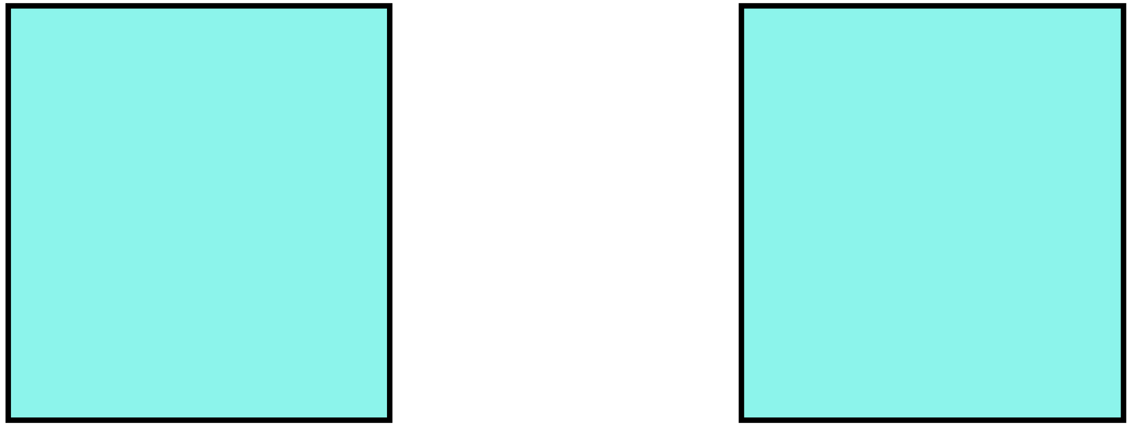


$\sum I_{i,j}=I$, Sheet resistance=R

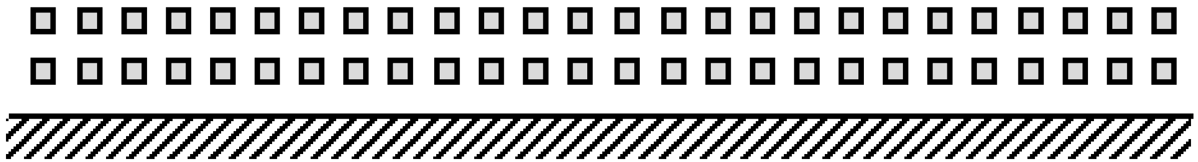
Take IR as unity voltage drop

Interconnect Cross-Section and Noise

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply



Scaled interconnect
- Signal

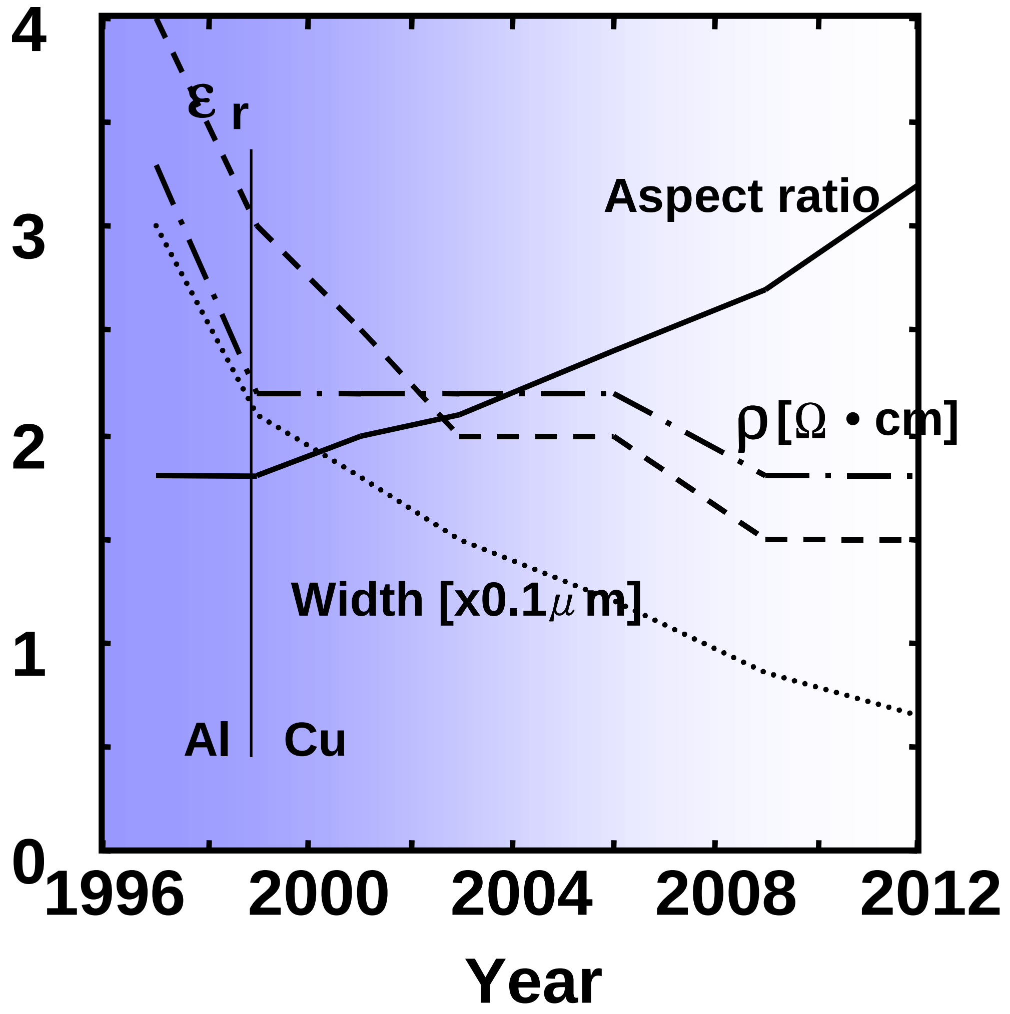


1V 20W → 20A current

2% noise on VDD & VSS → ~0.02V / 20A → ~10μm thick Cu

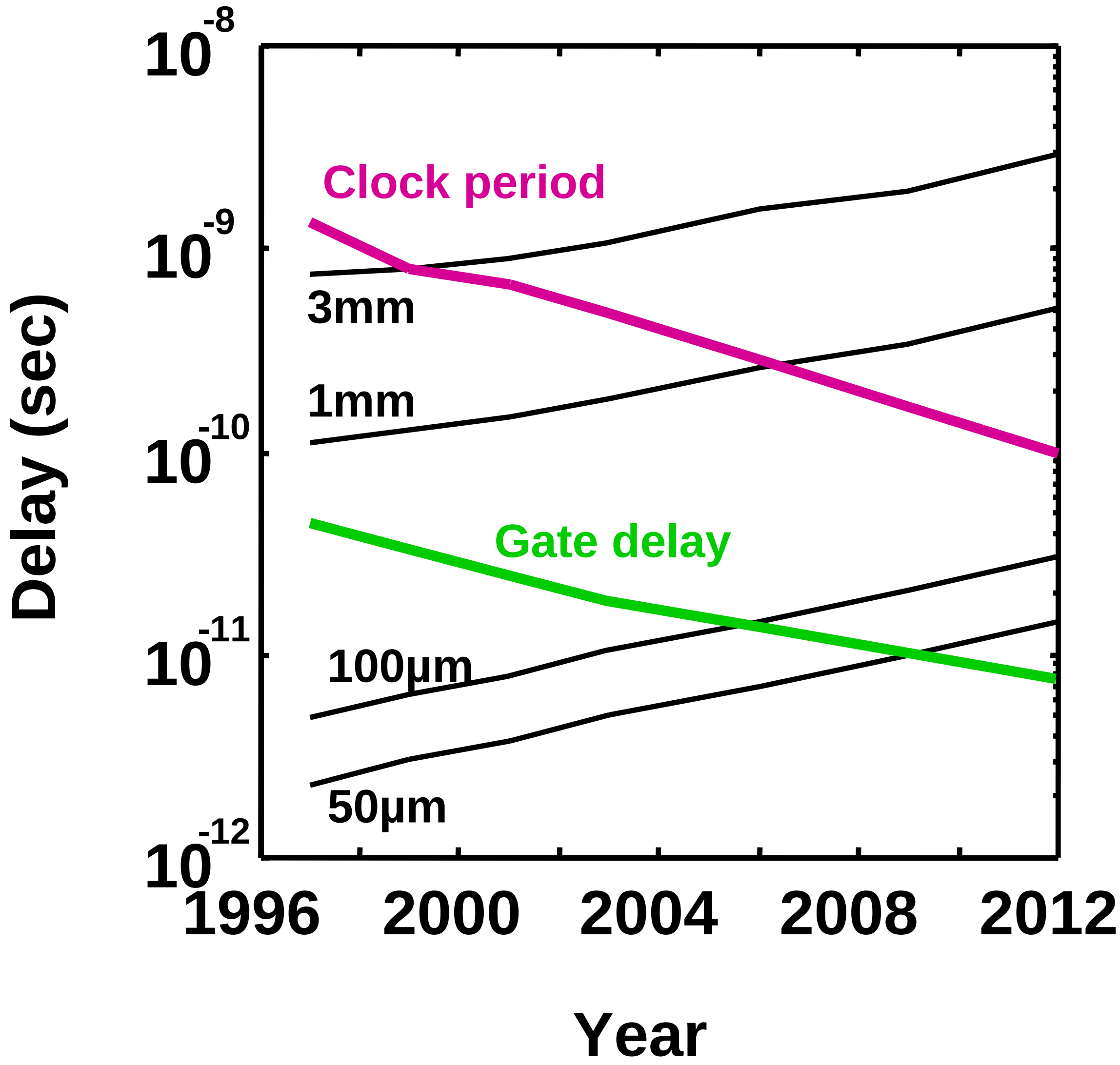
Thick layer interconnect, area pad, package are co-designed.

Interconnect parameters trend

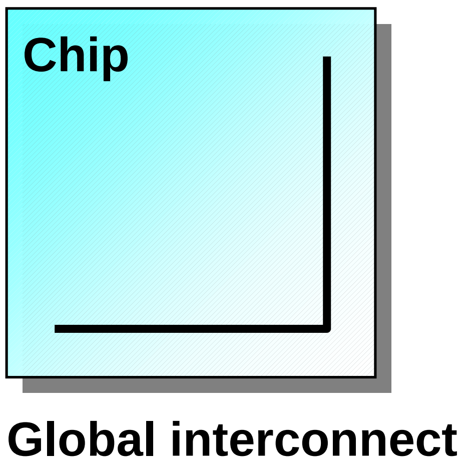


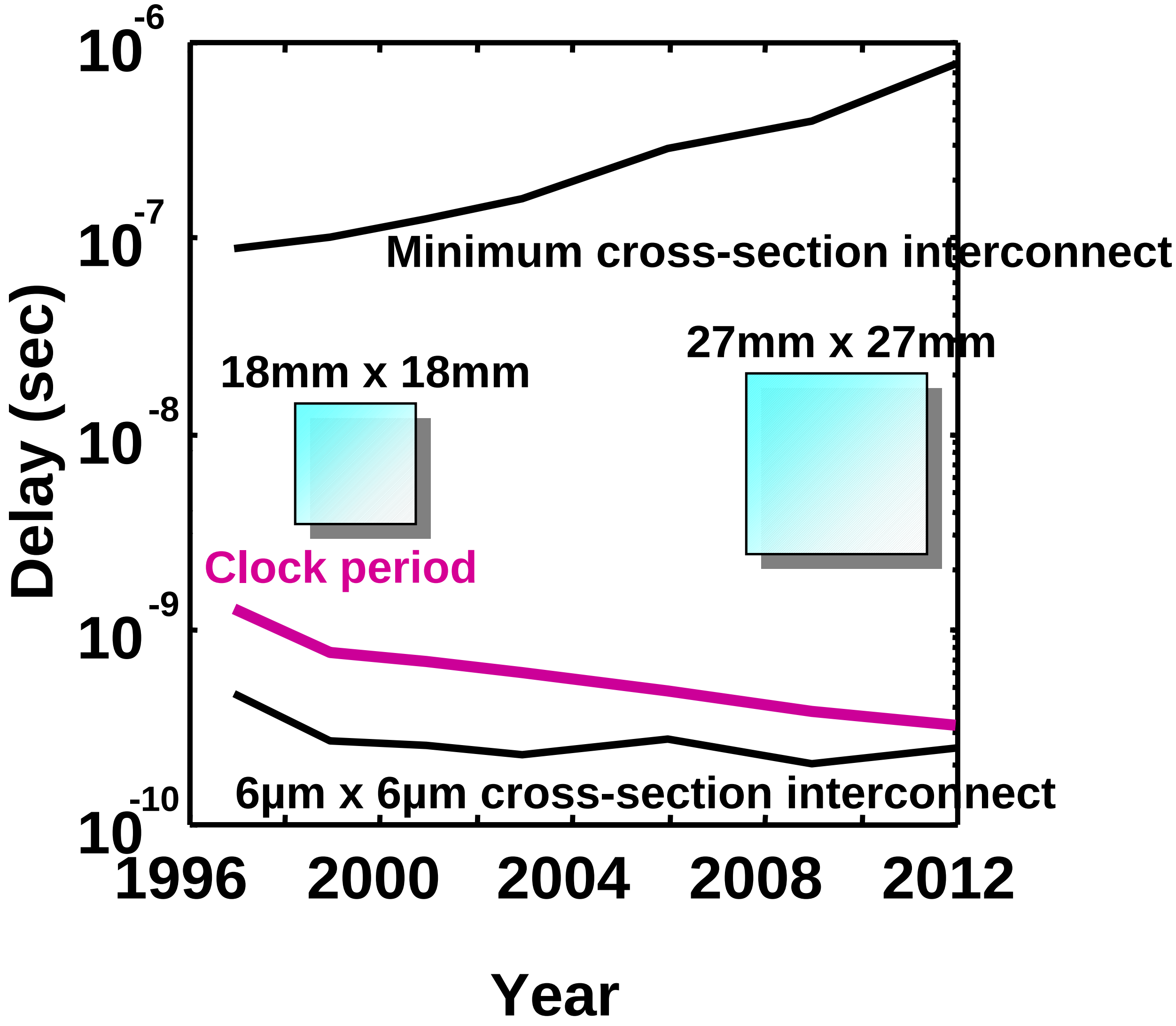
Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

RC delay and gate delay

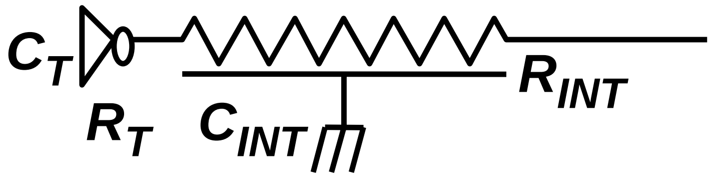


RC delay of global interconnections

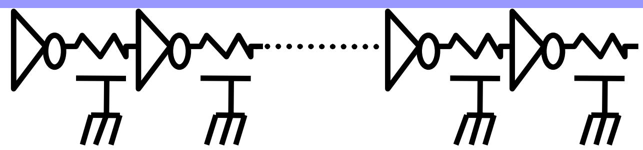




Repeaters



a) Without repeaters



b) With repeaters

$$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693(R_T C_T + R_T C_{INT} + R_{INT} C_T)$$

$$C_0 : Gate\ capacitance\ of\ minimum\ MOSFET$$

$$R_0 : Gate\ effective\ resistance\ of\ minimum\ MOSFET$$

$$Delay \approx k\left[p_1 \frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h} hC_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k} hC_0\right)\right] : Buffered$$

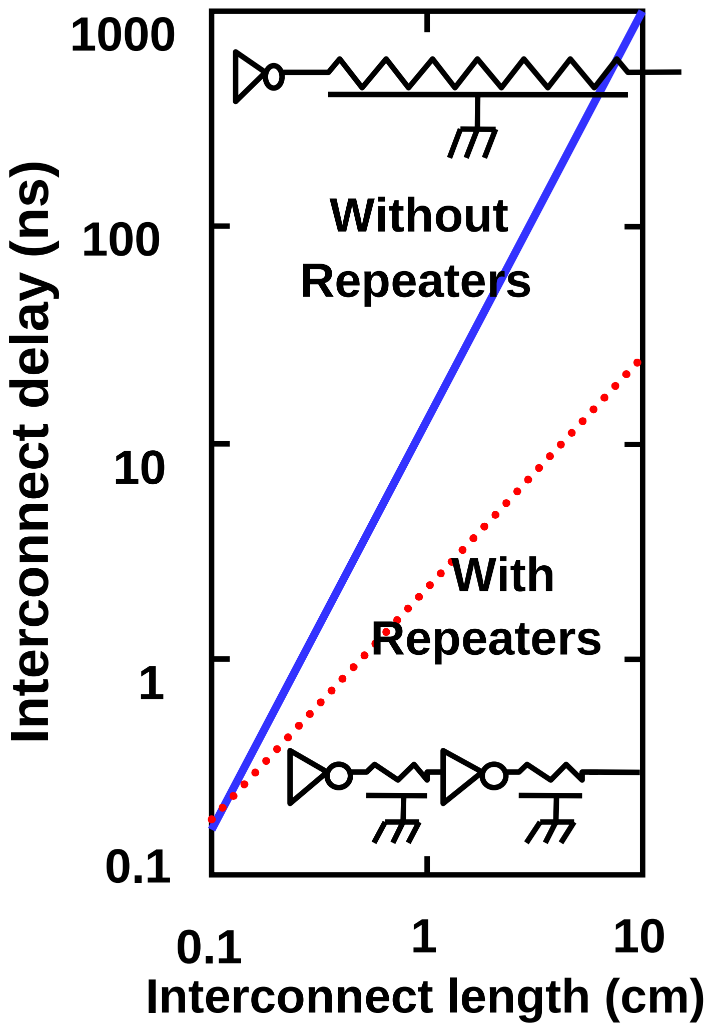
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT} R_0}{R_{INT} C_0}} : Optimized\ size\ of\ buffer\ inverter$$

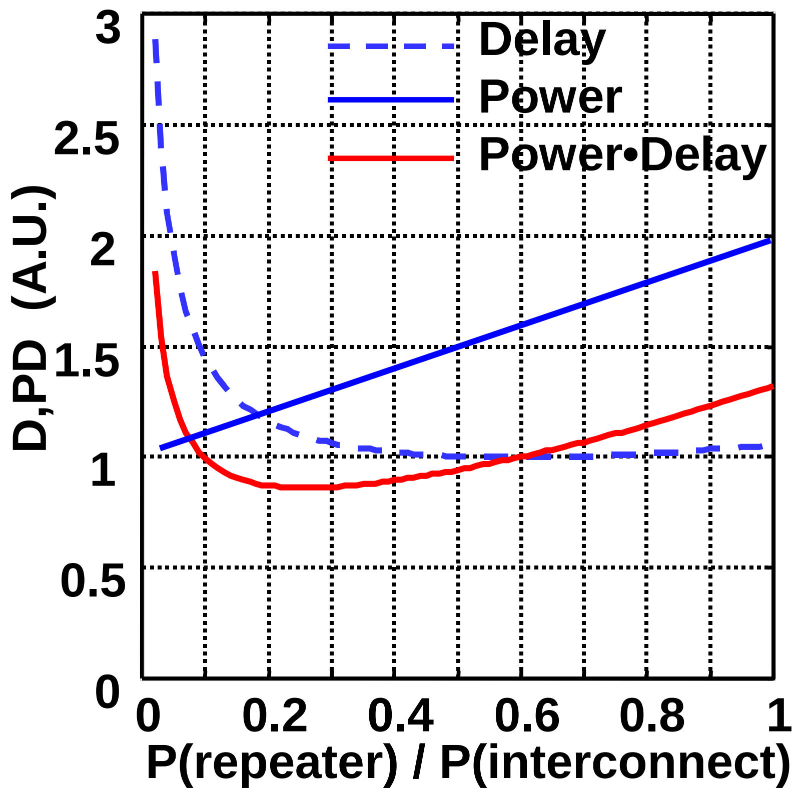
$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}}\sqrt{\frac{R_{INT} C_{INT}}{R_0 C_0}} : Optimized\ number\ of\ stages$$

$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right)\sqrt{R_{INT} C_{INT} R_0 C_0} \approx 2.4\sqrt{\tau_{INT}\tau_{MOS}}$$

$$Cap.\ of\ gates = k_{OPT} h_{OPT} C_0 = \sqrt{p_1 / p_2}\, C_{INT} = 0.73 C_{INT}$$

Delay and Power Optimization for Repeaters





Delay optimized

→P: P(repeater)=0.60 P(interconnect)

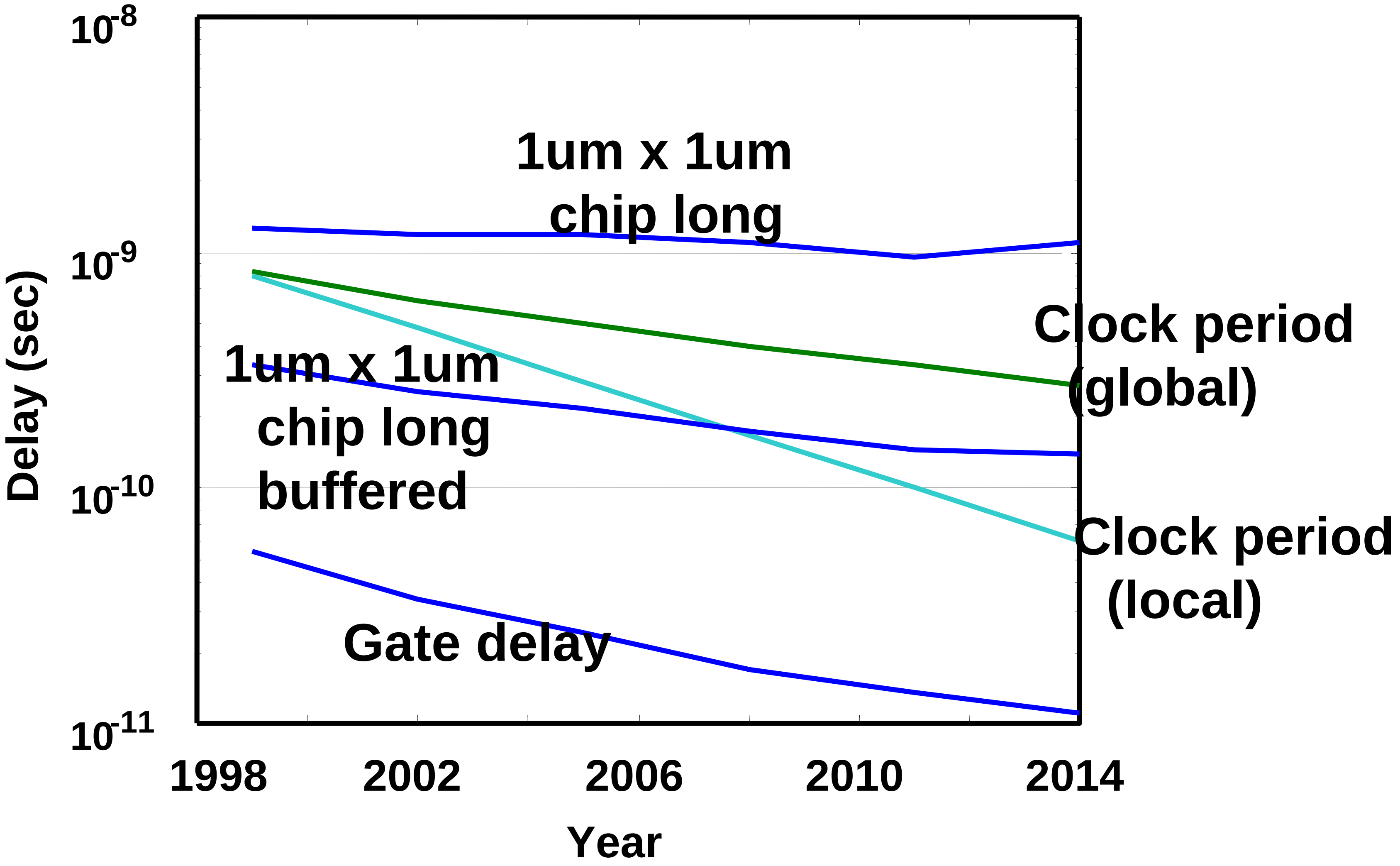
Power•Delay optimized

→D: 1.09 Dopt

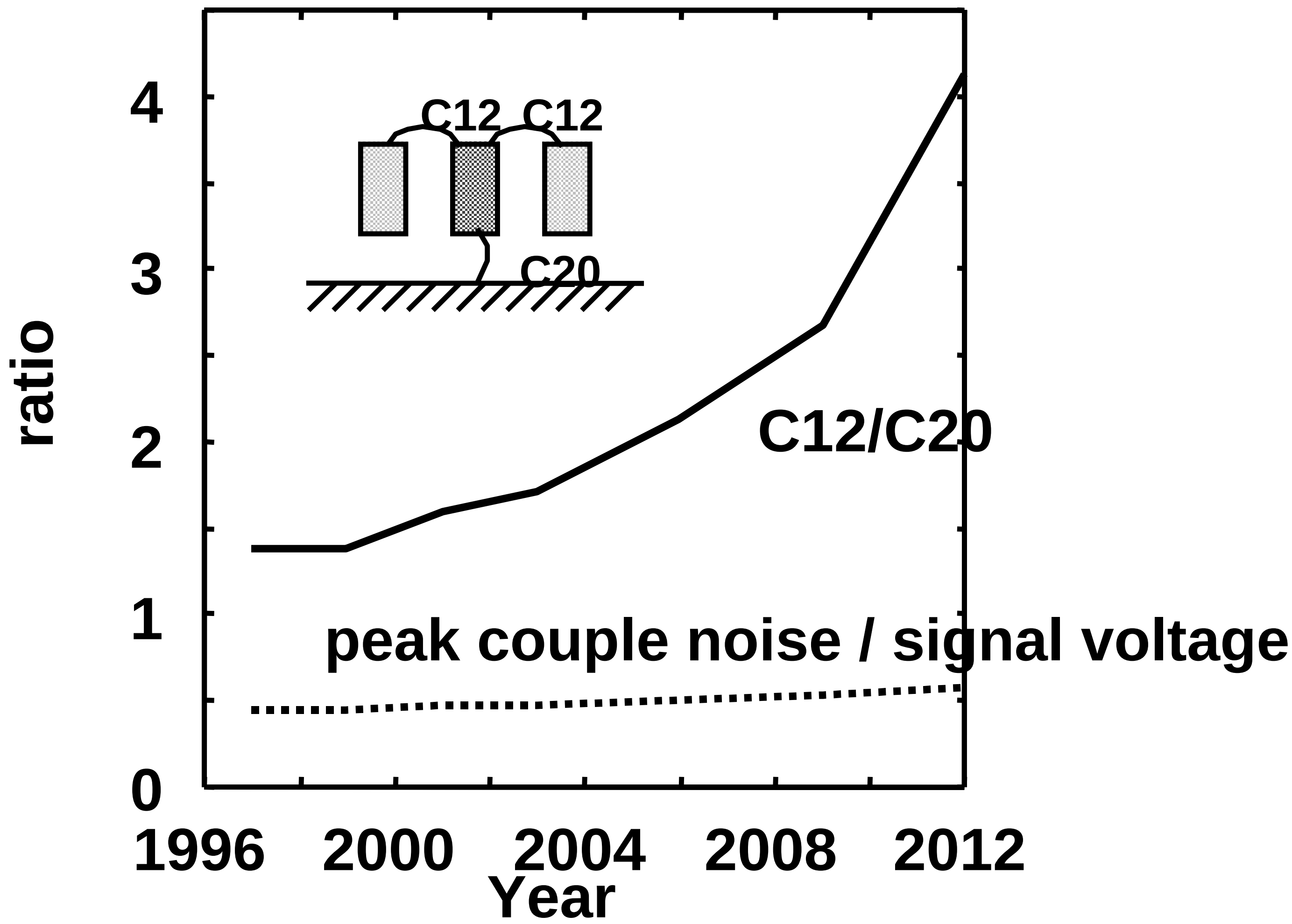
→P: P(repeater)=0.26 P(interconnect)

→PD: 0.86 of Dopt case

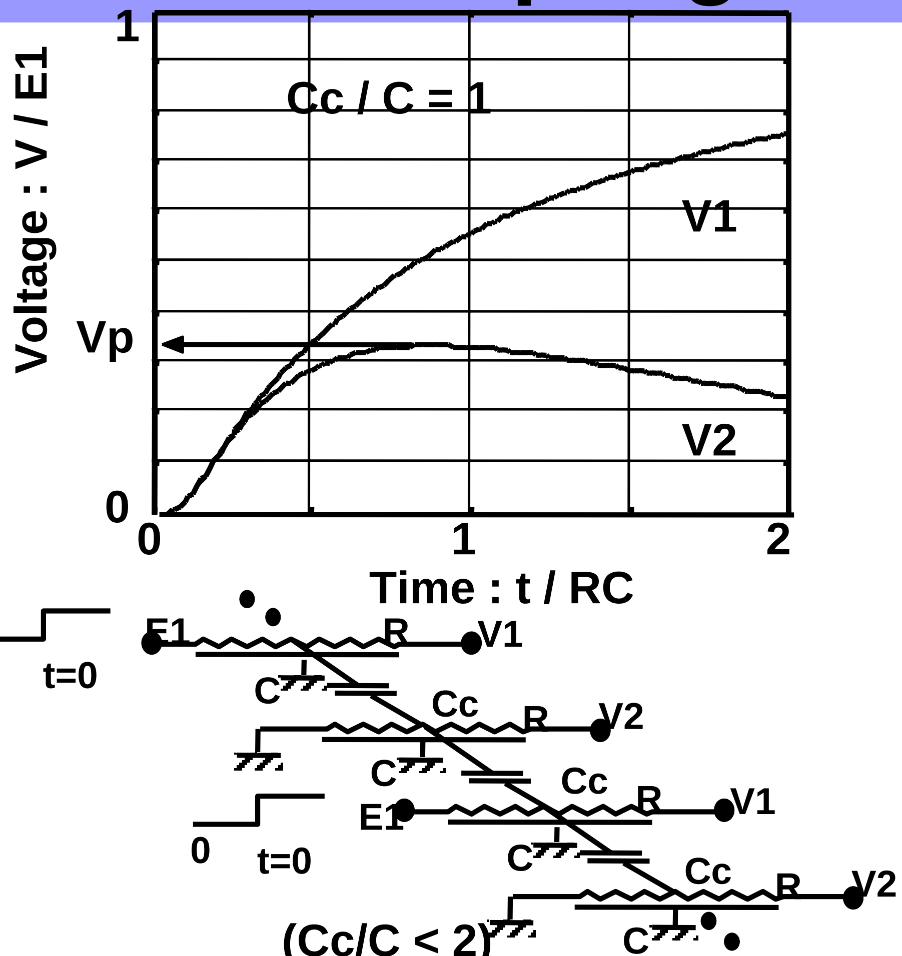
Buffered interconnect delay

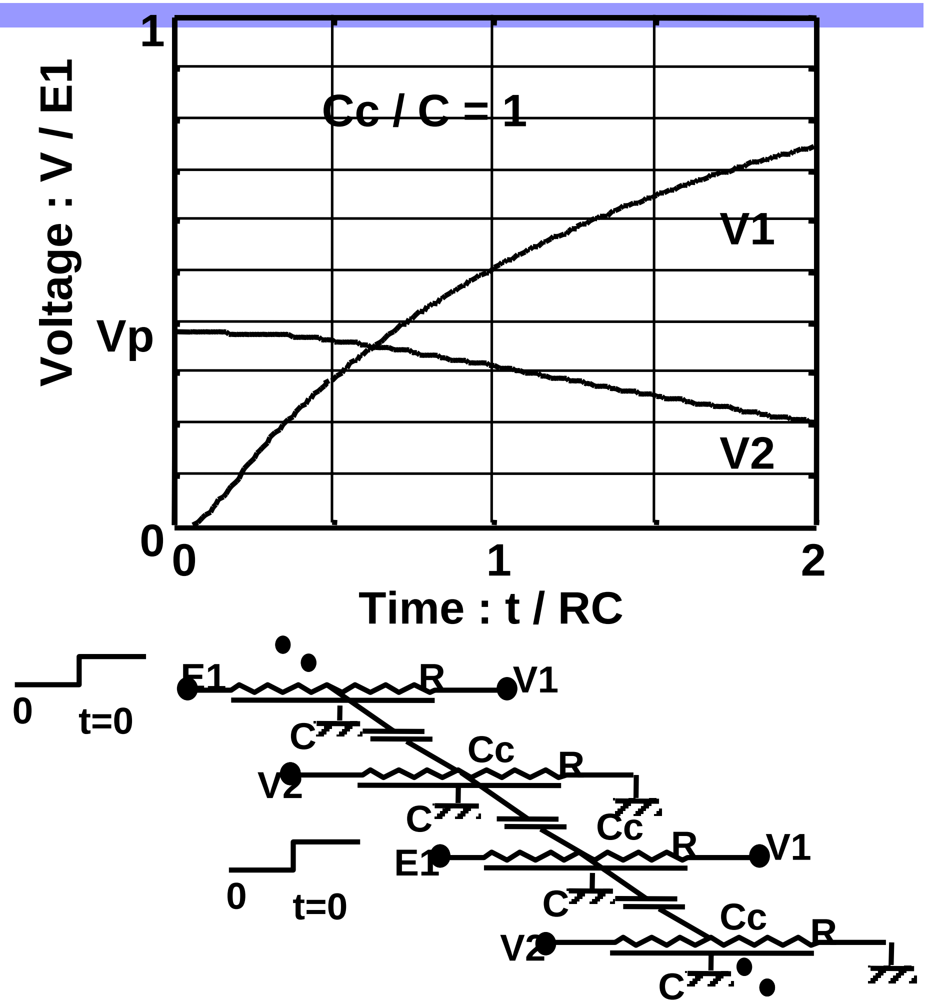


Capacitive Coupling Noise



Coupling noise in RC bus





(Cc/C < 2)

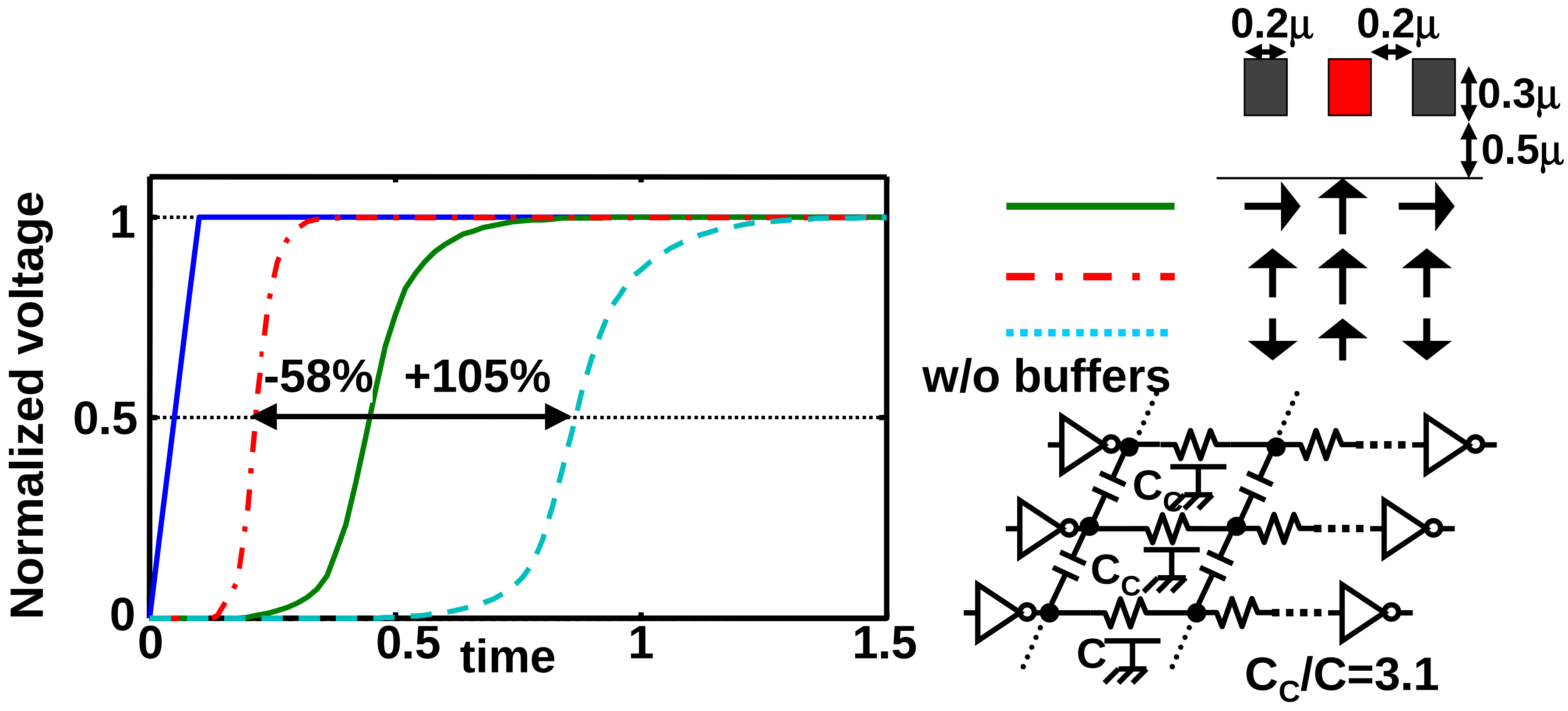
$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$

$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnections

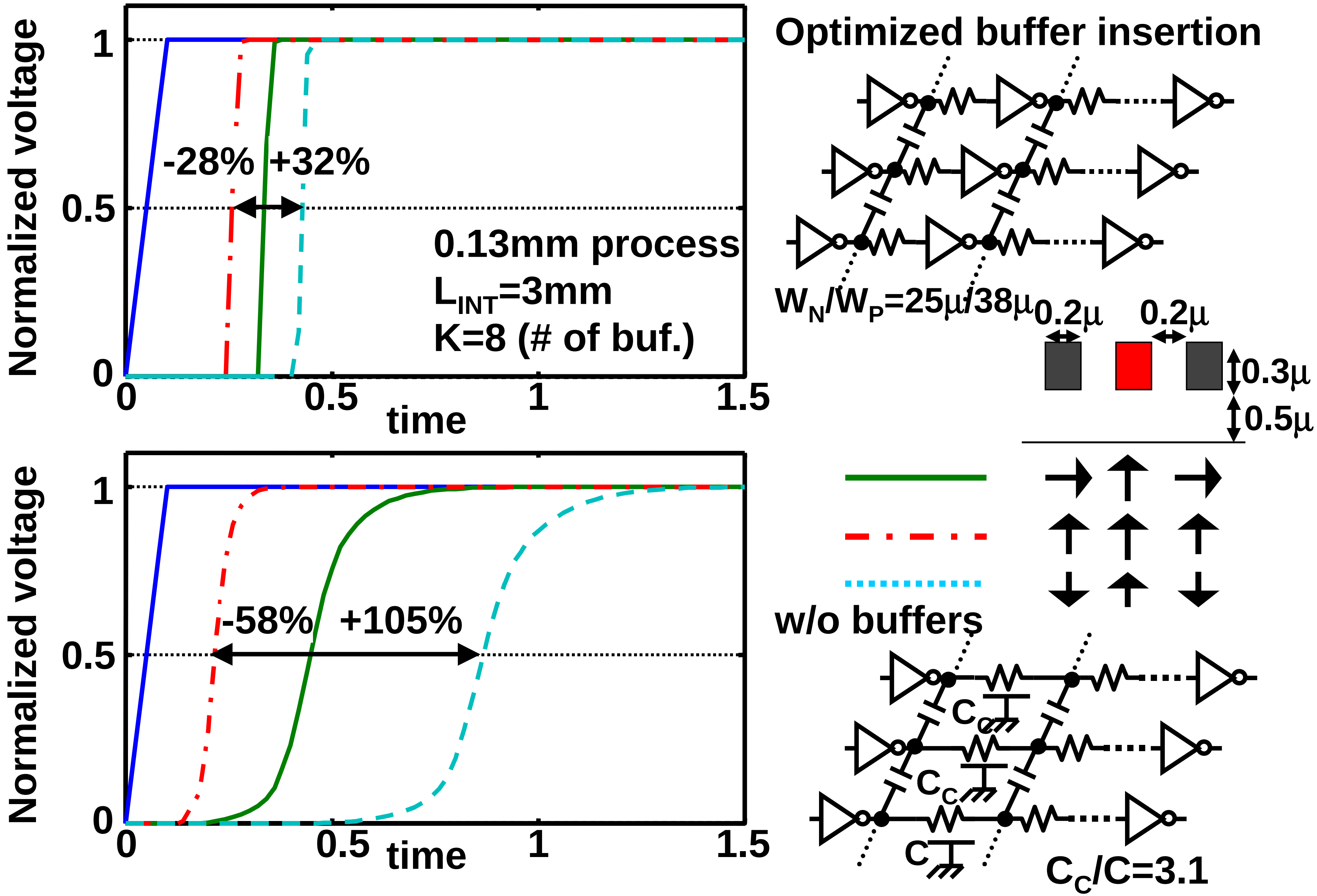


$$\frac{t_{pd}}{RC} = \frac{1}{2} + 2\eta - \frac{1}{\sqrt{6}} \log \frac{e}{2} \sqrt{1 + 8\eta + 6\eta^2}$$

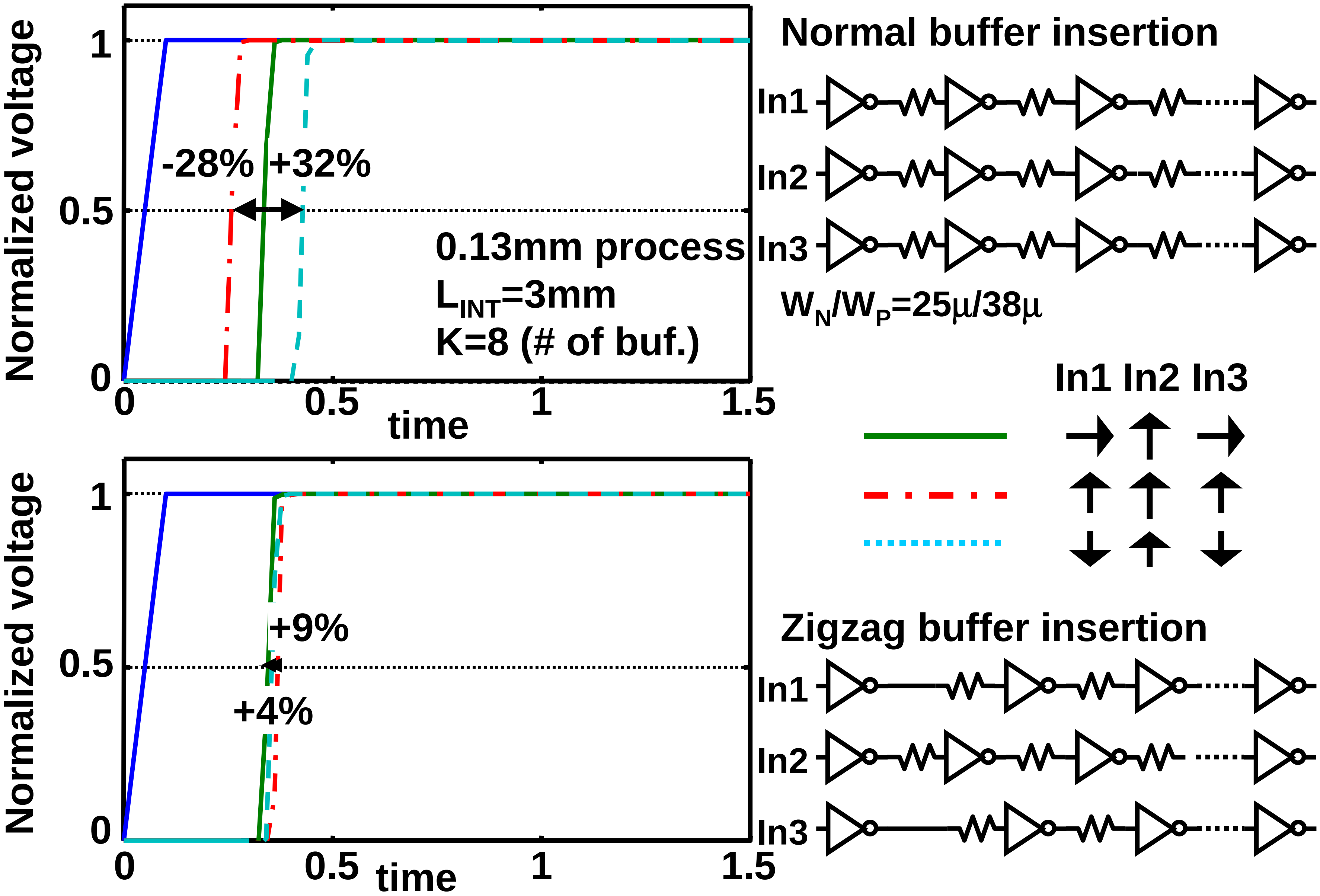
$$\approx 1.63\eta + 0.37 (\eta \le 2)\ (\eta = C_C / C)$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," 1998 ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

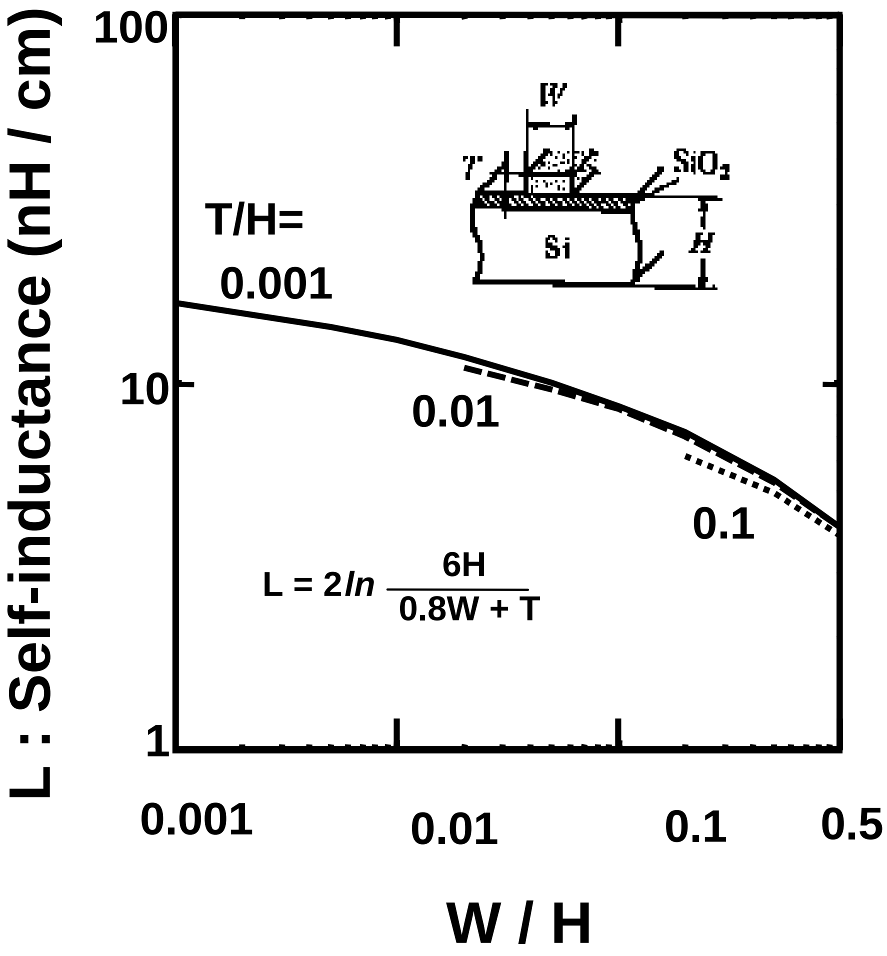
Coupling among Interconnections



Coupling among Interconnections



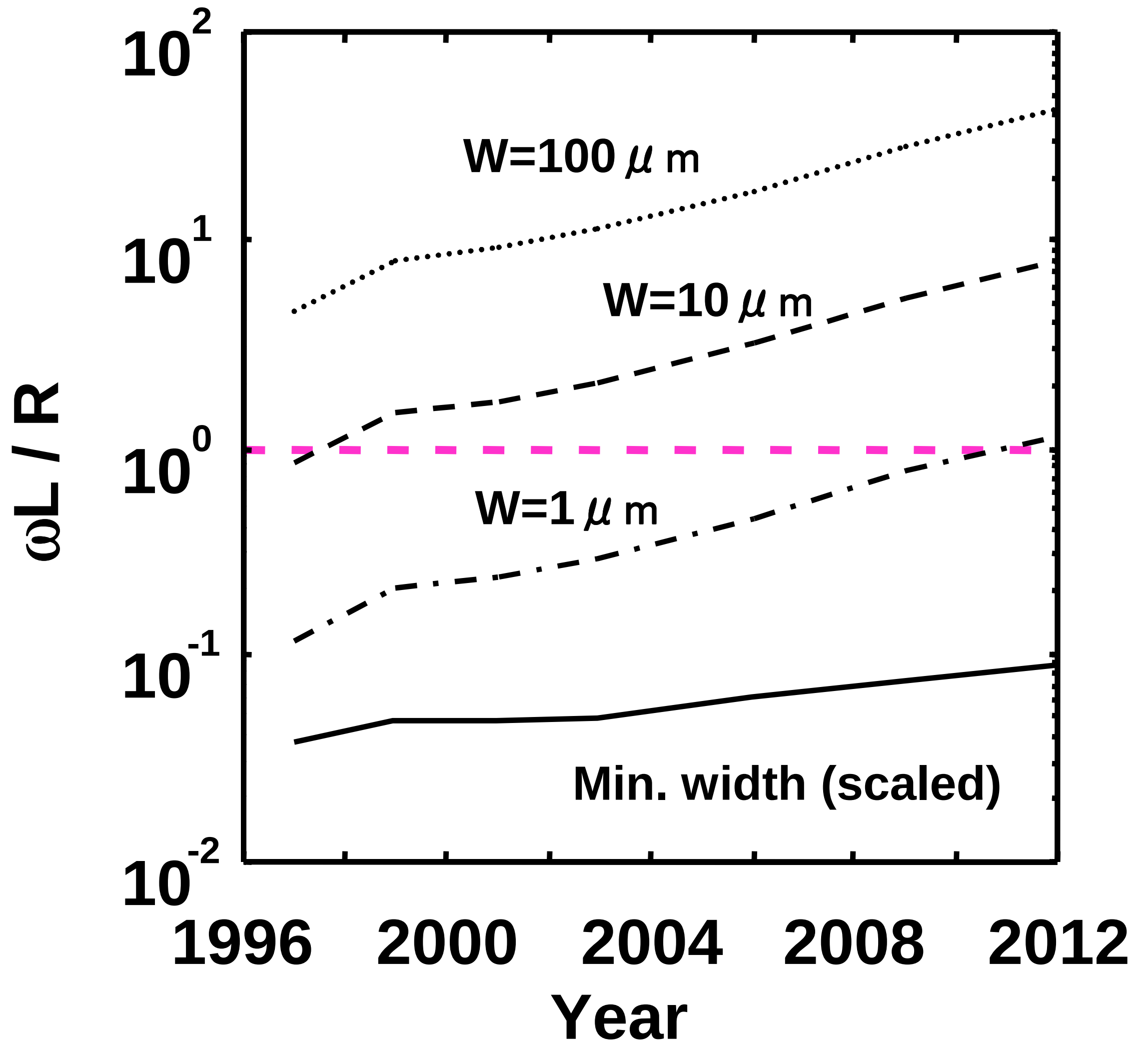
Inductance?



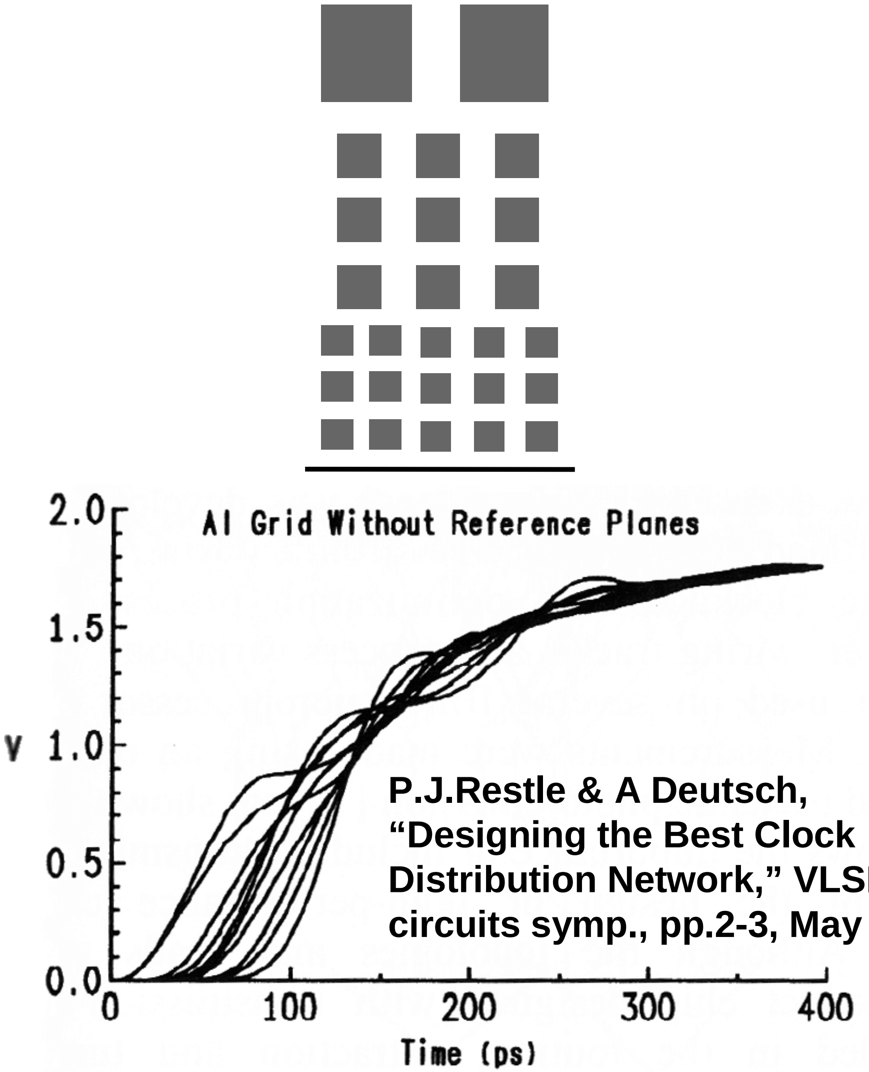
- **Now RC effects surmounts LC effects because R > |jωL|.**
- **In the future, both of R and ωL increase (R increases more rapid?).**
- **Exception in low-R lines**
- **Inductive effects in wide clock lines in a fast processor are claimed to be observed in simulation.**
- **Clock lines are placed on power plane to reduce inductive effects.**

[1] D.A.Priore, "Inductance on Silicon for Sub-micron CMOS VLSI," Symp. on VLSI Circuits, 1993.

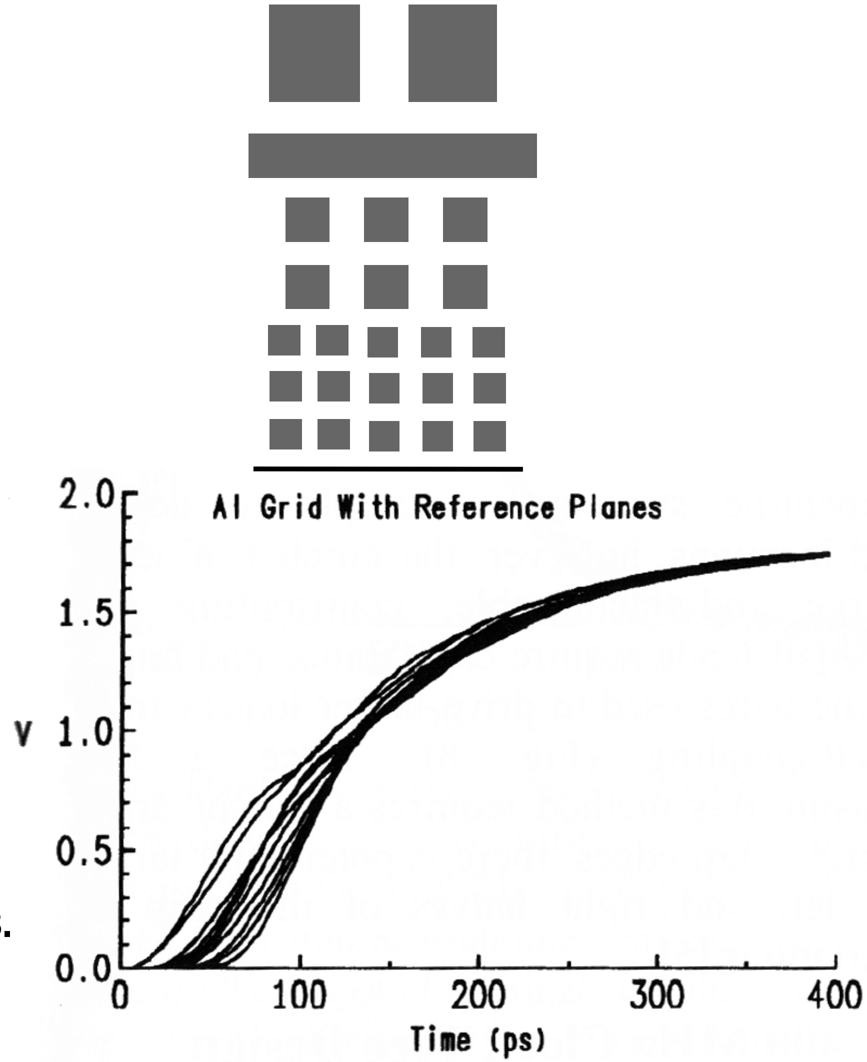
Inductive Effects



Inductive Effects in Clock Lines

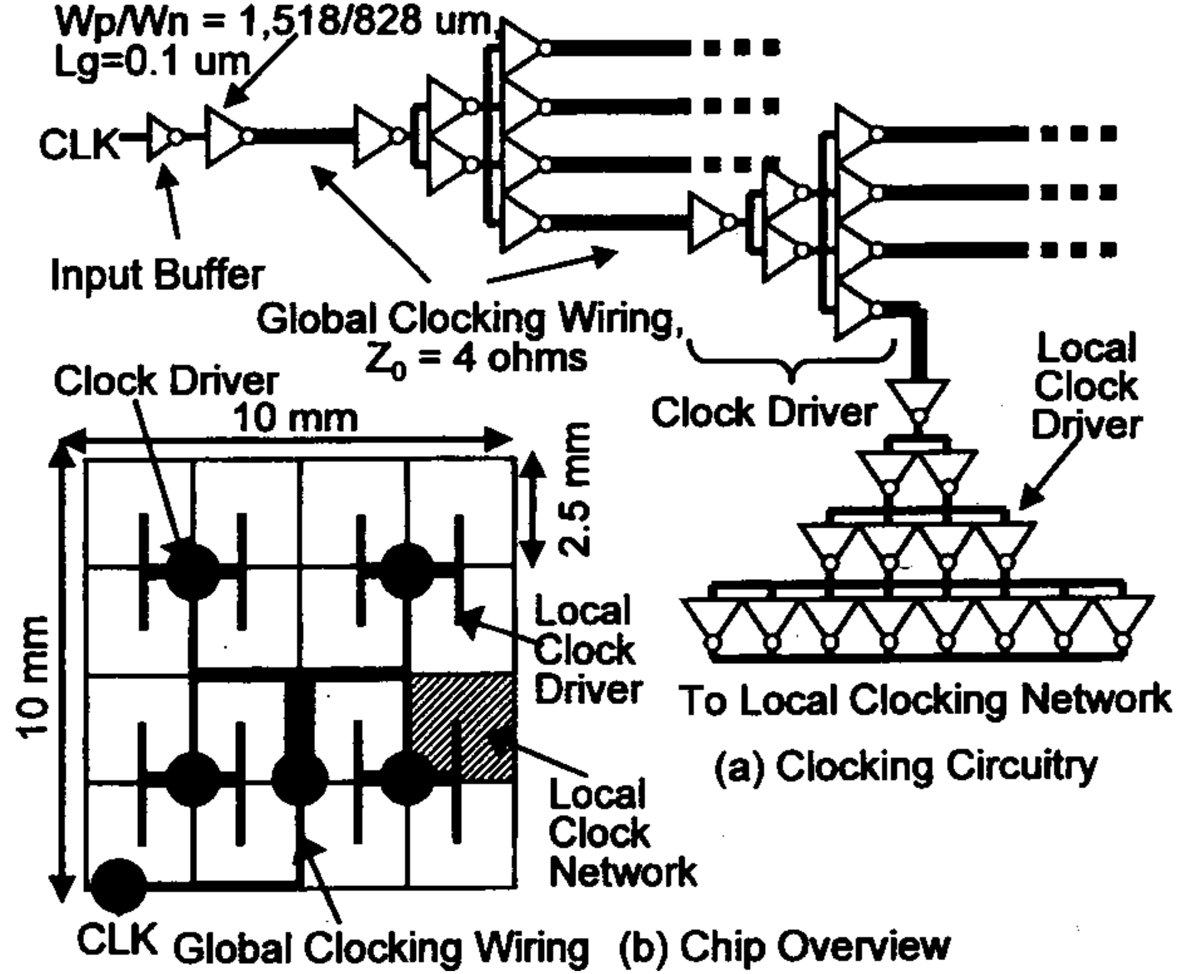


P.J.Restle & A Deutsch, "Designing the Best Clock Distribution Network," VLSI circuits symp., pp.2-3, May 1998.



Board design practice is imported in LSI.

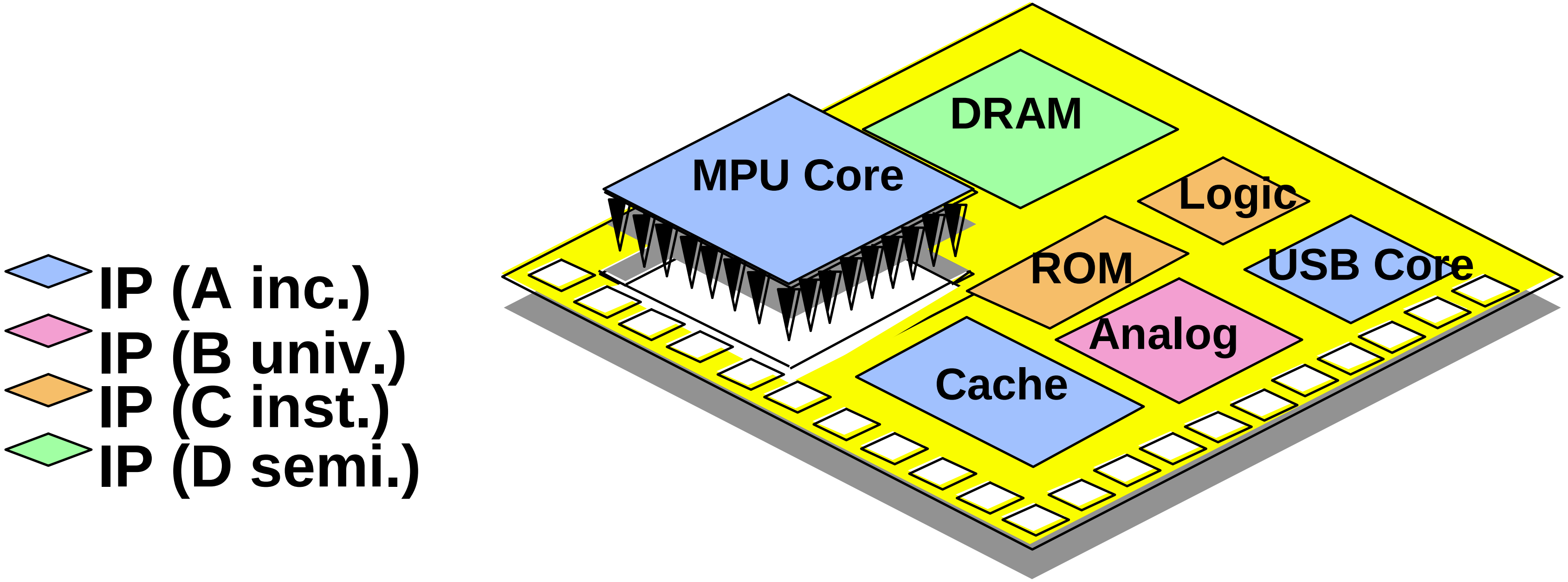
H-tree clock distribution



M.Mizuno, K.Anjo, Y.Sumi, H.Wakabayashi, T.Mogami, T.Horiuchi, M.Yamashina, “On-Chip Multi-GHz Clocking with Transmission Lines,” ISSCC, pp.366-367, Feb. 2000

System on a Chip (SoC)

- Re-use and sharing of design
- Design in higher abstraction



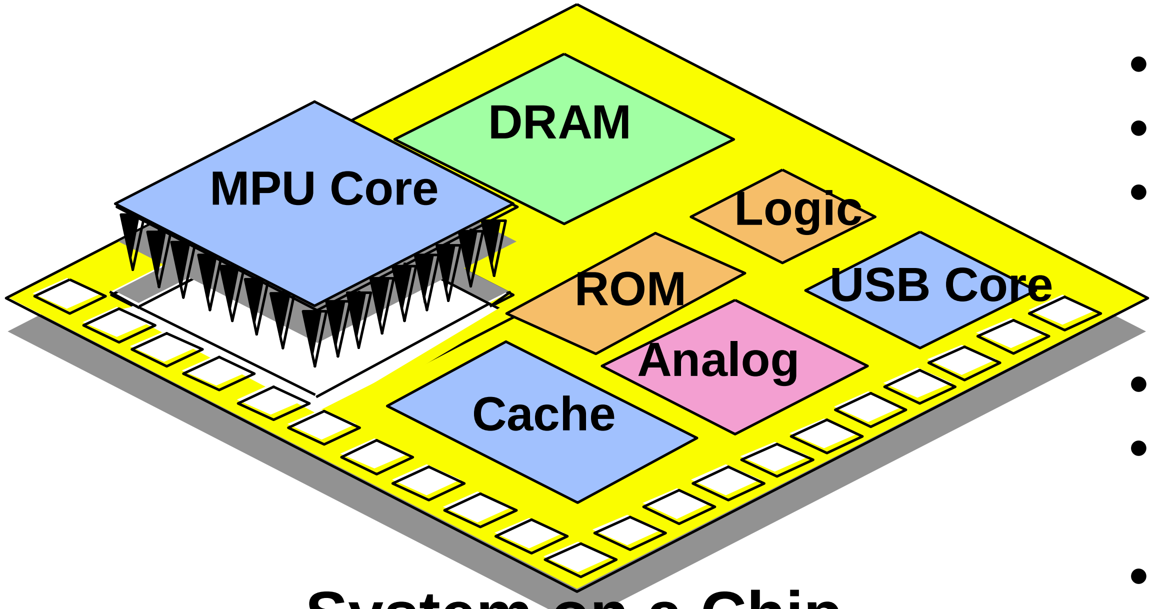
IP ; CPU, DSP, memories, analog, I/O, logic..

HW/FW/SW

Issues in System-on-Chip

- Un-distributed IP’s (i.e. CPU, DSP of a certain company)
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP’s
- Difficulty in high precision analog IP’s due to noise
- Process incompatibility with non-Si materials and/or MEMS

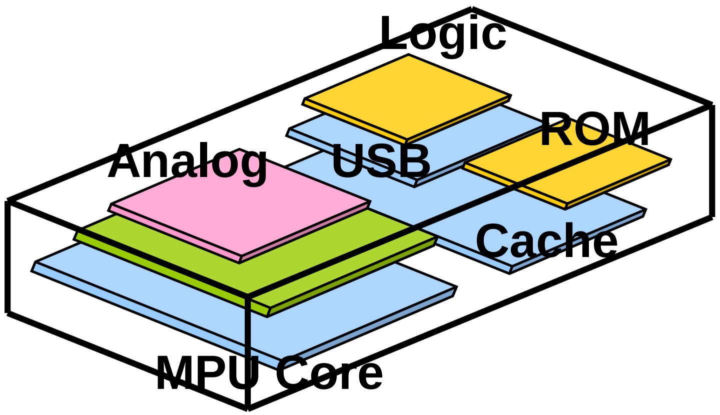
System in Package

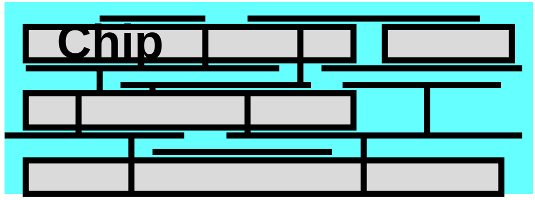


System on a Chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

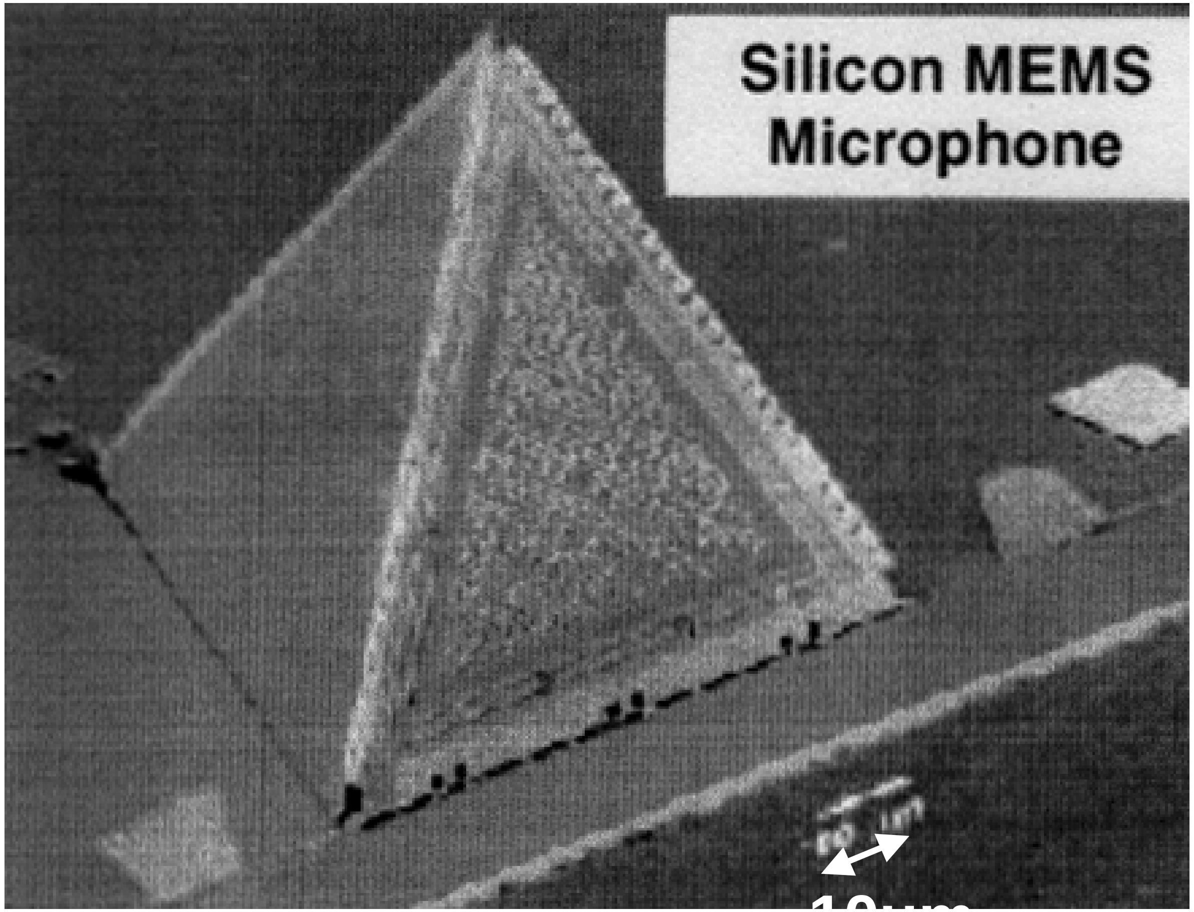
- Heat dissipation is an issue





System in Package

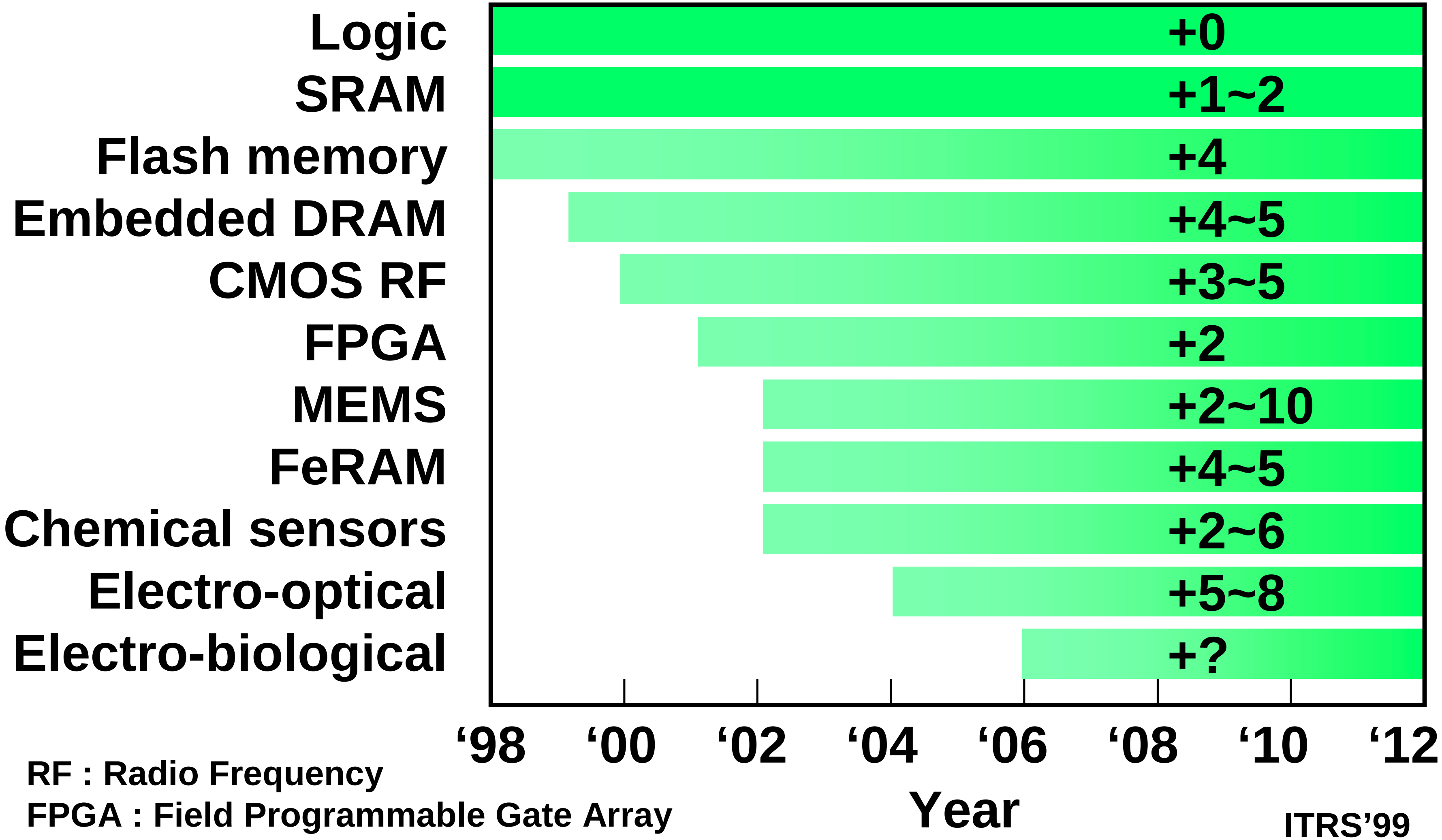
Silicon MEMS microphone



Will soon exceed the performance of the best commercial microphones, yet be inexpensive and potentially integrated with on-chip electronics.

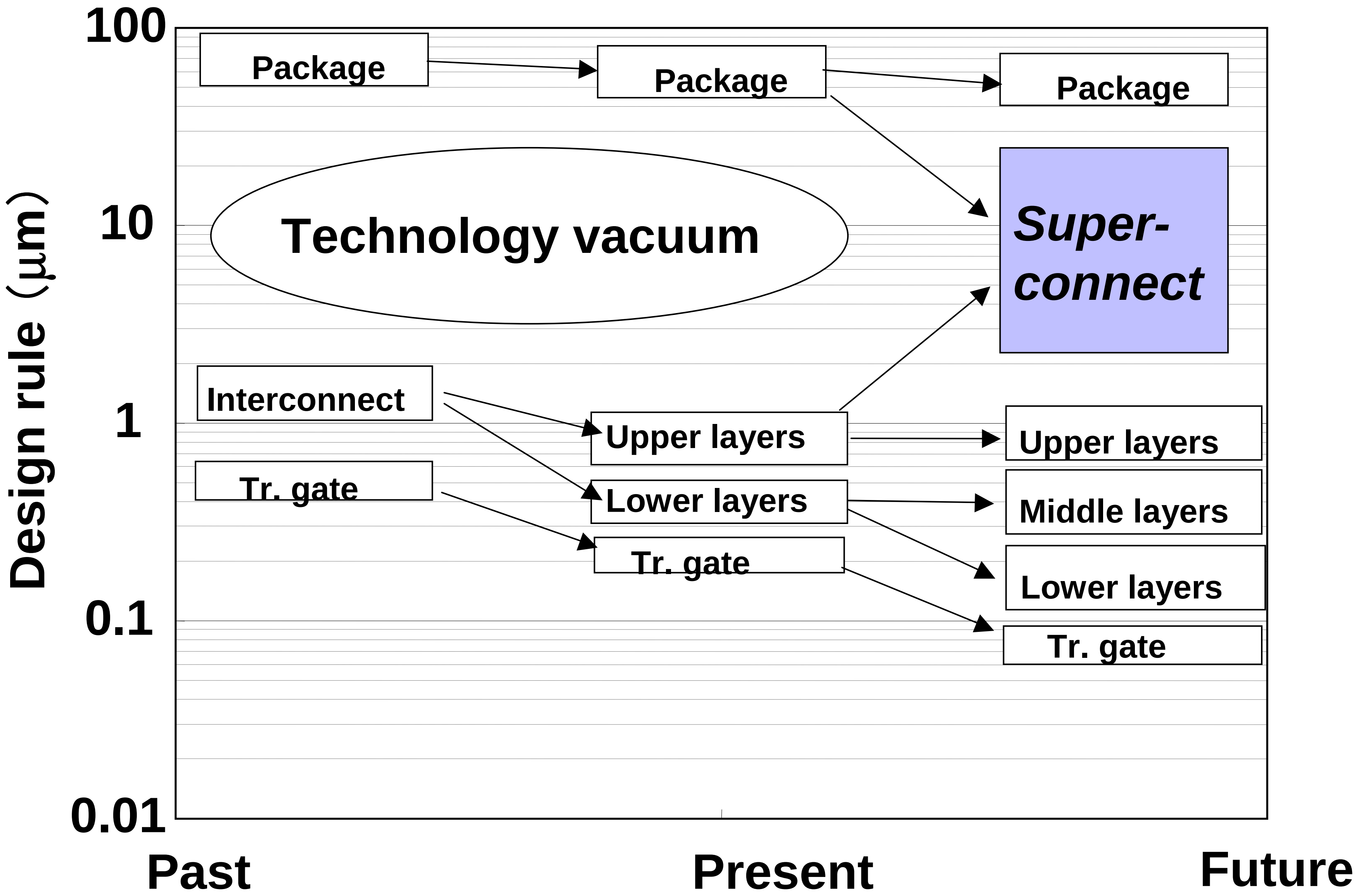
M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

Technologies integrated on a chip



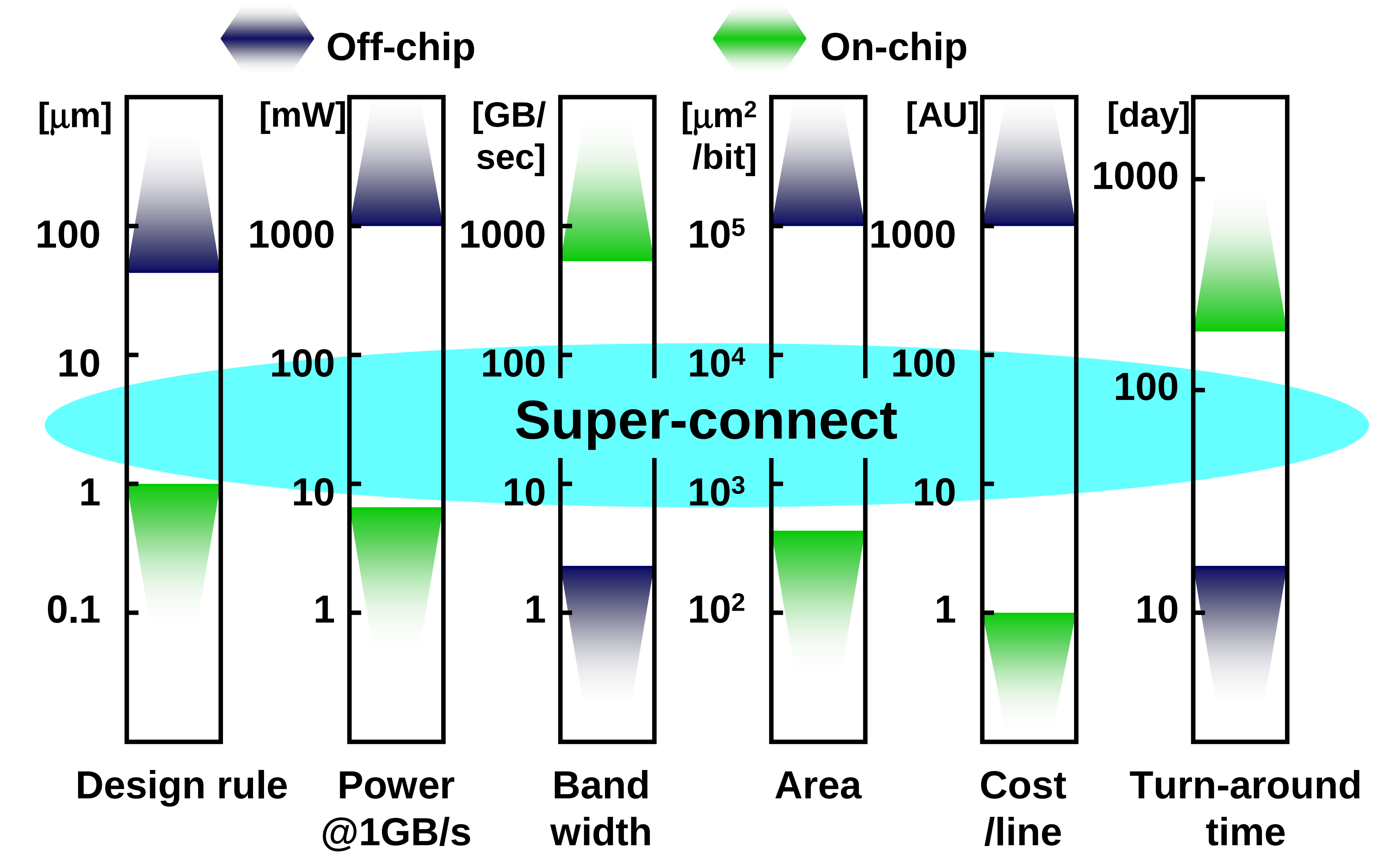
RF : Radio Frequency
FPGA : Field Programmable Gate Array
MEMS : Micro Electro Mechanical Systems
FeRAM : Ferroelectric RAM

Super-connect



Nikkei microdevices

Super-connect



LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	µm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (µP)		21M	3.6G	170
DRAM capacity		1G	1T	1000
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	µcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

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