11.4 Abnormal Leakage Suppression (ALS) Scheme for Low Standby Current SRAMs

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Abnormal leakage suppression (ALS) repairs standby current errors in SRAMs. By introducing leakage sensors, shift registers, and fuses, the ALS senses 1mA abnormal leakage and isolates the memory cell from Vpp lines, thus suppressing abnormal leakage current. A 64Kb test SRAM demonstrated effectiveness. The area overhead is 7%.

SRAMs are widely used as key components such as main memories, caches, and buffer memories in high-speed portable systems, where low standby current is required to extend lifetime of batteries. Power consumption of SRAMs in standby mode is normally negligibly small due to the highly resistive nature of MOSFETs in off-state. However, if memory cells and/or related circuits have defects due to process fluctuations and/or dust, the standby current is increased drastically making SRAM unsuitable for portable applications. A number of schemes to repair defective memory cells, rows, and columns have been proposed by introducing redundant rows and columns and redundancy schemes are widely used [1]. Although all of these schemes repair faults, unsure considers leakage path elimination possibly associated with the defects. This paper describes an abnormal leakage repair scheme to eliminate leakage paths.

Figure 11.4.1 shows an SRAM memory cell in standby mode with various possible defects in channel or in gate oxide. In standby mode, word lines are set to Vdd, while bit lines are precharged to Vpp. The dotted lines in the figure represent leakage paths from Vpp to Vdd caused by a single defect in the memory cell. The case where a cell has multiple defects is not taken into account since it is unlikely. There are two ways to eliminate abnormal leakage paths in a memory cell. One is to completely isolate the error cell from Vpp, and the other is to isolate the cell from Vdd. In this paper, the latter is pursued. The former approach is difficult to realize since the Vdd lines for an SRAM cell array are usually structured as a mesh and are impossible to cut off selectively. There are only three types of paths that convey Vpp to a memory cell in a standby mode, that is, cell Vpp lines, bit lines and wells.

In the ALS scheme, a fuse is inserted in each cell Vpp line and each bit line pair as shown in Figure 11.4.2. When the fuse is blown, the Vpp is cut from these lines, isolating memory cells from Vpp. There is no need to insert a fuse between Vdd and the n-well, because when a drain junction of pMOS (M1) is short-circuited to an n-well, the drain junction is set to Vdd in a power-on sequence. Then M4 turns on, which in turn turns M3 off. Thus, there is no abnormal leakage path, if the memory cell is not accessed in a normal mode. This is achieved by replacing the cell with a redundant memory cell. There are many ways to introduce redundancy in an SRAM bit, but, since it is established technique, is not dealt in this paper. Any type of redundancy works well with ALS. Since the scheme systematically isolates Vpp in a memory cell, it repairs most leakage errors even those other than the transistor-related defects as shown in Figure 11.4.1. Metal shorts and junction shorts are other types of defects that cause standby errors.

The first step is to identify location of the defective memory cell in terms of leakage. This is accomplished by leakage sensors, as shown in Figure 11.4.3. After detecting the leakage, dynamic shift registers in Figure 11.4.3 transfer the result to the external tester in a scan-path method. The timing diagram for the operation of ALS is shown in Figure 11.4.4. Two pMOS transistors, M7 and M8, are inserted in parallel between Vpp and memory cell Vdd lines. M7 is activated in a test mode and has small on-state conductance to cause a voltage drop when a certain amount of leakage current flows through it. M8 is activated only in normal SRAM operation. The channel width of M8 should be large enough so that it delivers sufficient current into each row and column without degrading yield of normal operation. In test mode, the voltage drop across M7 is sampled and held in node N1 which is compared with a reference voltage Vref when the Sense Enable signal is asserted. If there is abnormal leakage, the voltage on N1 becomes lower than the reference voltage Vref on N2. When the leakage sensor is activated, the voltage difference between N1 and N2 is amplified and N1 goes to '0' while N2 goes to '1'. The signals are transferred to N4 and N3. Thus N3 is set '1' when there is a certain level of leakage and it is set to '0' when there is no leakage. This error indicator is scanned out to the leakage sensor output. The '0' and '1' pattern on the leakage sensor output terminal indicates the rows and columns where leakage error cells exist.

Sensitivity of the leakage sensor can be tuned by adjusting Vref and VLEAK_MONITOR. The measured sensitivity is shown Figure 11.4.5. The target leakage level of a test chip is 14nA but can be adjusted by selection of Vref and the size of M7.

Figure 11.4.6 shows the reduction of leakage current by blowing fuses in the ALS scheme. Four leakage error cells, each of which shows about 40nA leakage, are made intentionally and leakage is decreased by blowing fuses one by one. This assures elimination of leakage paths by the fuses.

Figure 11.4.7 shows a micrograph of the test ALS SRAM chip fabricated with 0.6um and triple-layer metal technology. The SRAM cell array that has 256 rows and 256 columns occupies 2.6x2.8mm². The area overhead with ALS is calculated at 7.8%. This value is reduced to 2% when ALS is applied to 1Mb SRAMs.

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Reference:
Figure 11.4.1: SRAM cell circuit in standby mode with possible leakage paths due to the transistor related defects.

Figure 11.4.2: Overall structure of ALS scheme.

Figure 11.4.3: Detailed circuit diagram of ALS scheme.

Figure 11.4.4: Timing diagram for ALS circuit.

Figure 11.4.5: Measured sensitivity on bias conditions for $V_{\text{REF}}$ and $V_{\text{LEAK-MONITOR}}$.

Figure 11.4.6: Measured leakage current reduction by blowing fuses.