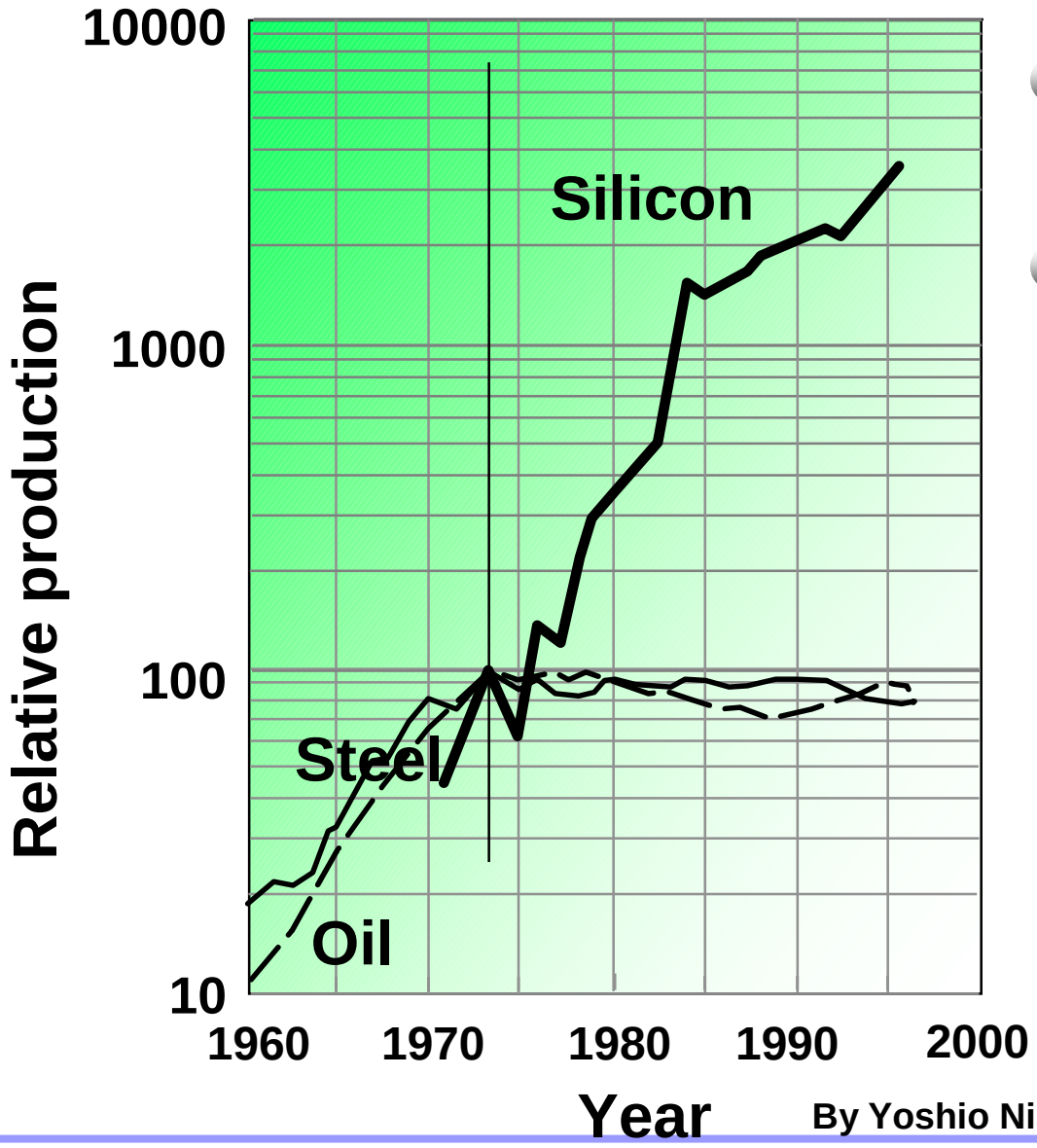
ニューガラスフォーラム　’00/9

エレクトロニクス産業の将来技術
―　シリコンLSIを中心に　―

Prof. Takayasu Sakurai
Center for Collaborative Research, and
Institute of Industrial Science,
University of Tokyo
E-mail:tsakurai@iis.u-tokyo.ac.jp

1　　産業を取り巻く環境
2　　消費電力の危機
3　　配線の危機
4　　複雑さの危機
5　　将来展望

Silicon Age



By Yoshio Nishimura

- Info processing by LSI (Si)
- Info transfer by fibers (SiO_2)

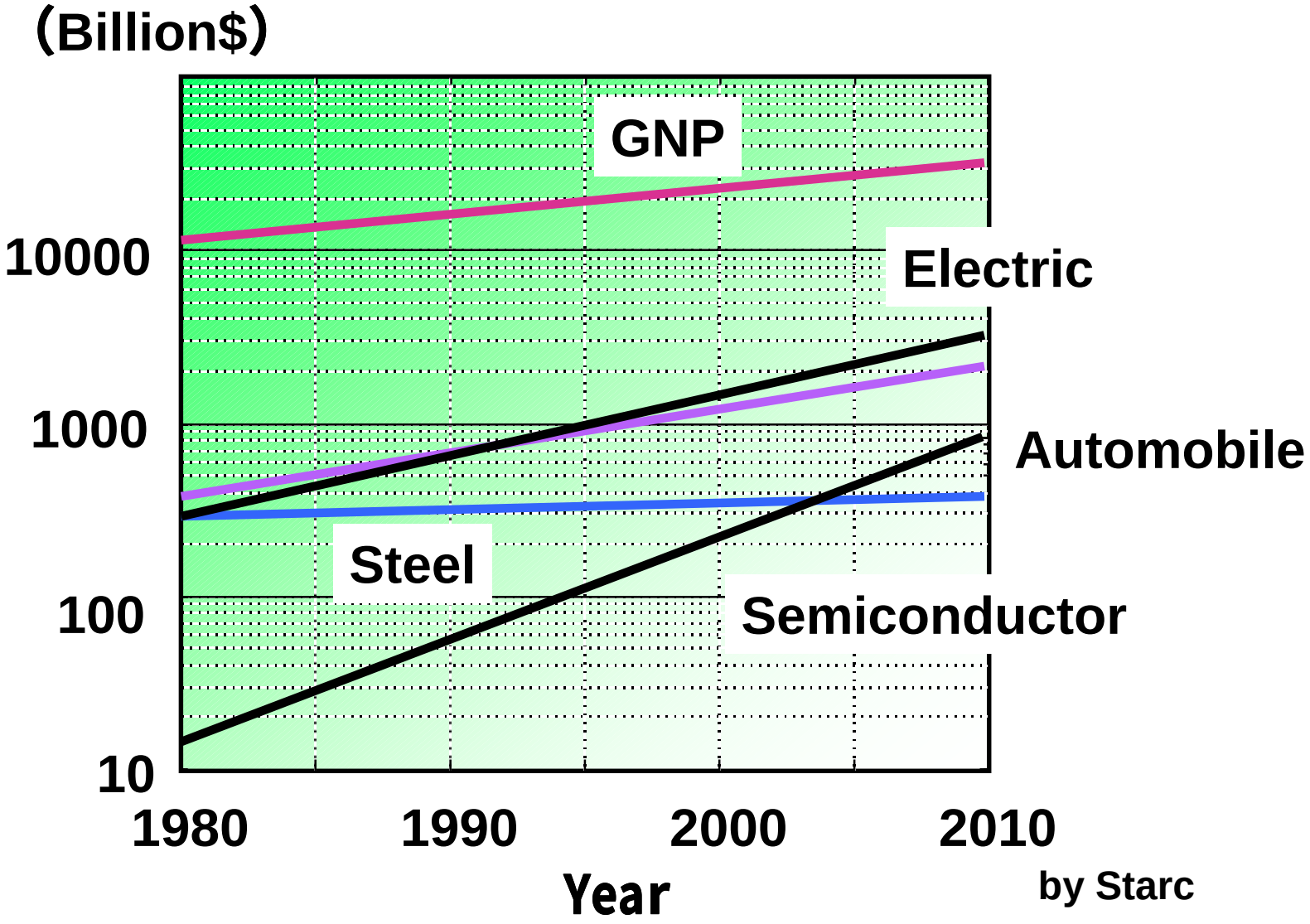
Memory

Processors

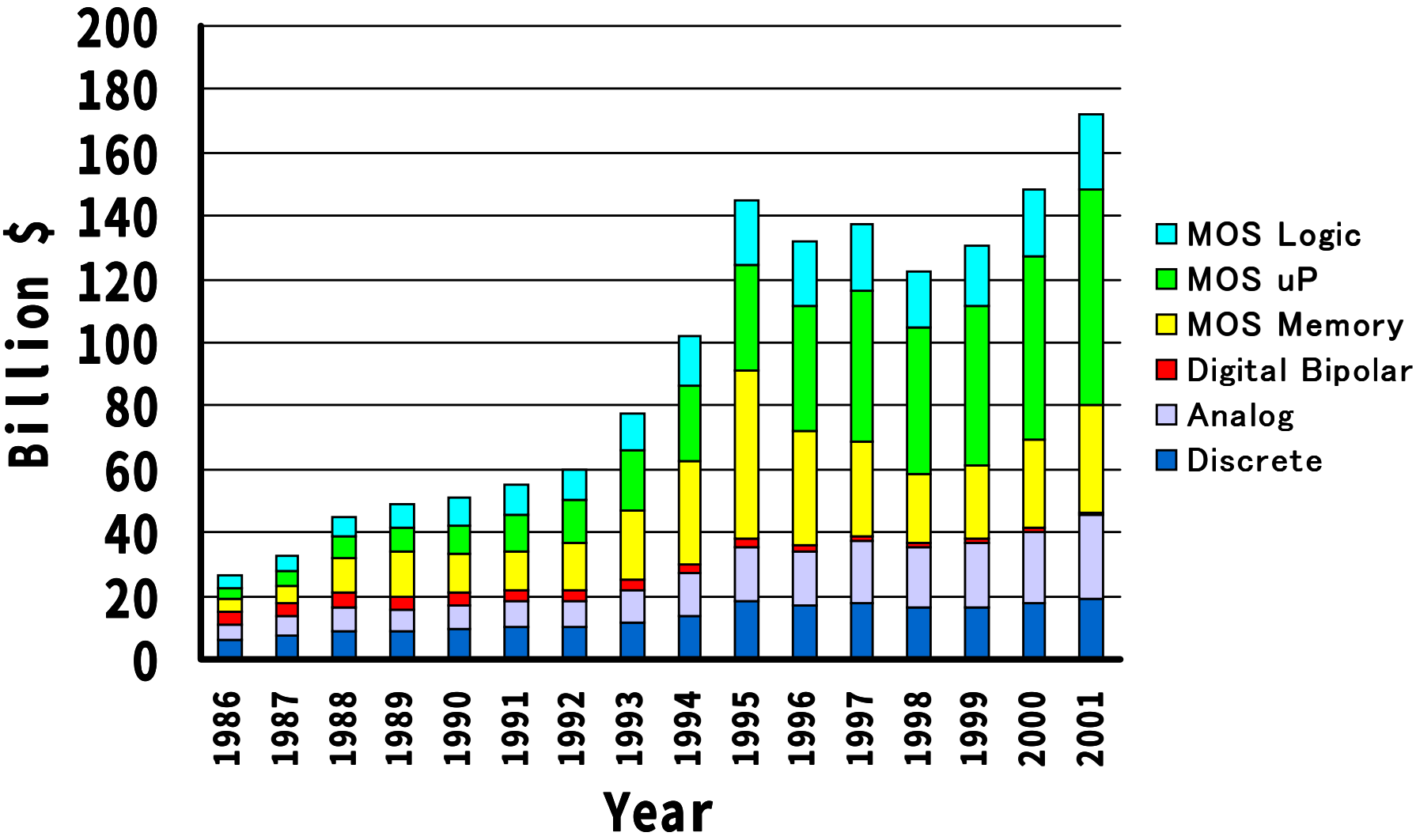
Sensors

Communicators

World-Wide Semiconductor Market



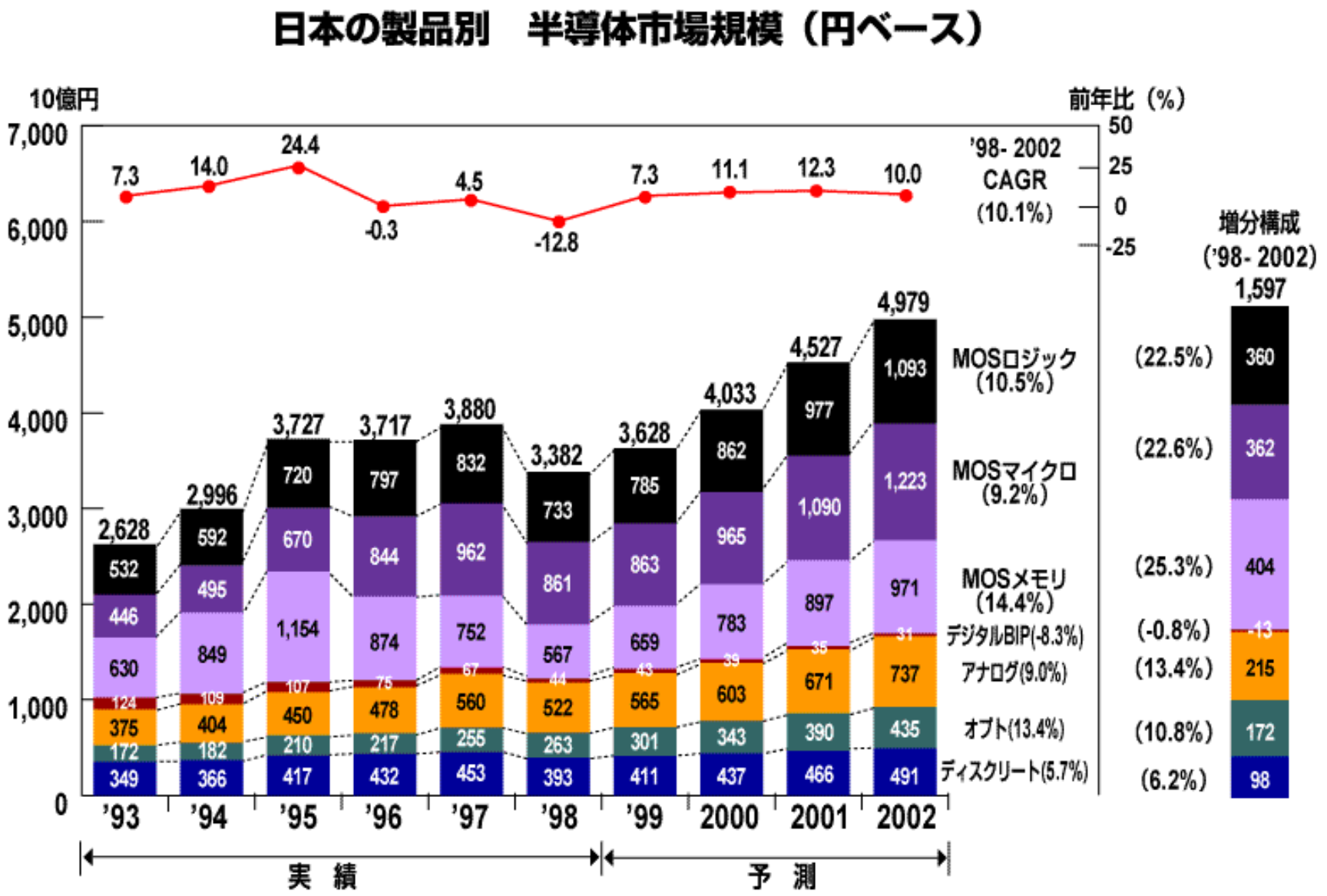
World semiconductor market



Data : World semicon market statistics

T.Sakurai

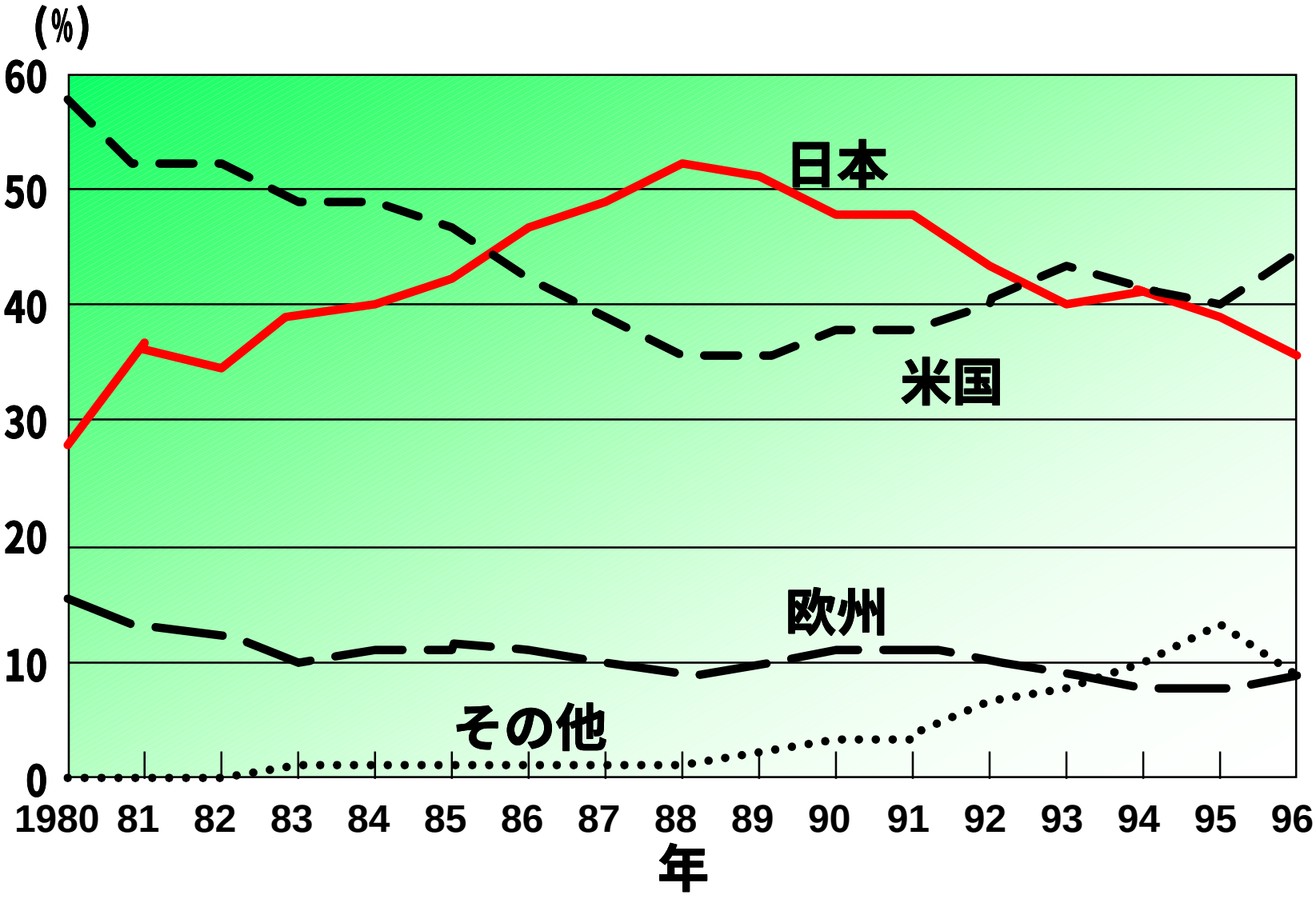
日本の半導体市場



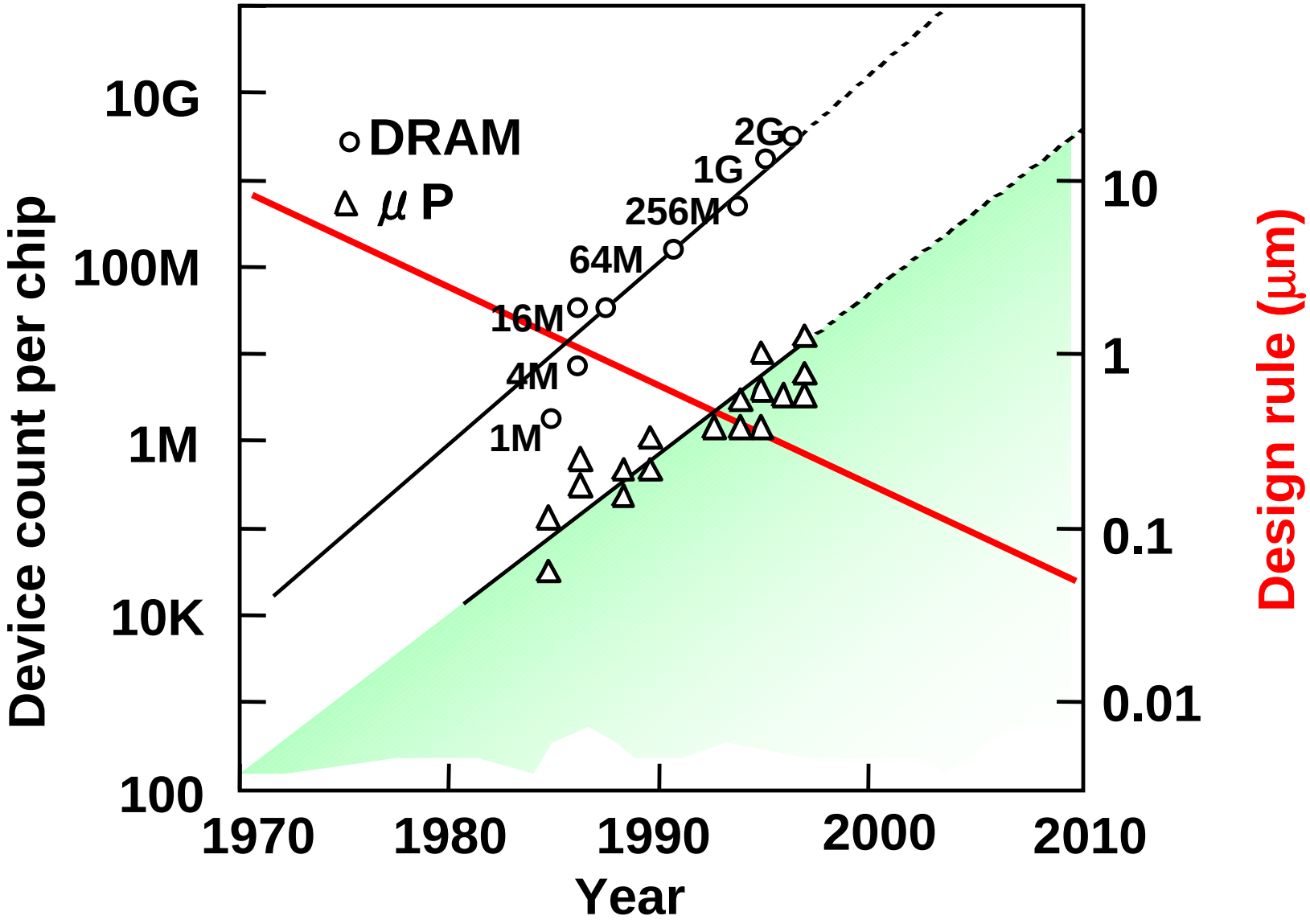
http://www.eiaj.or.jp/japanese/press/pre64/index_2.htm

T.Sakurai

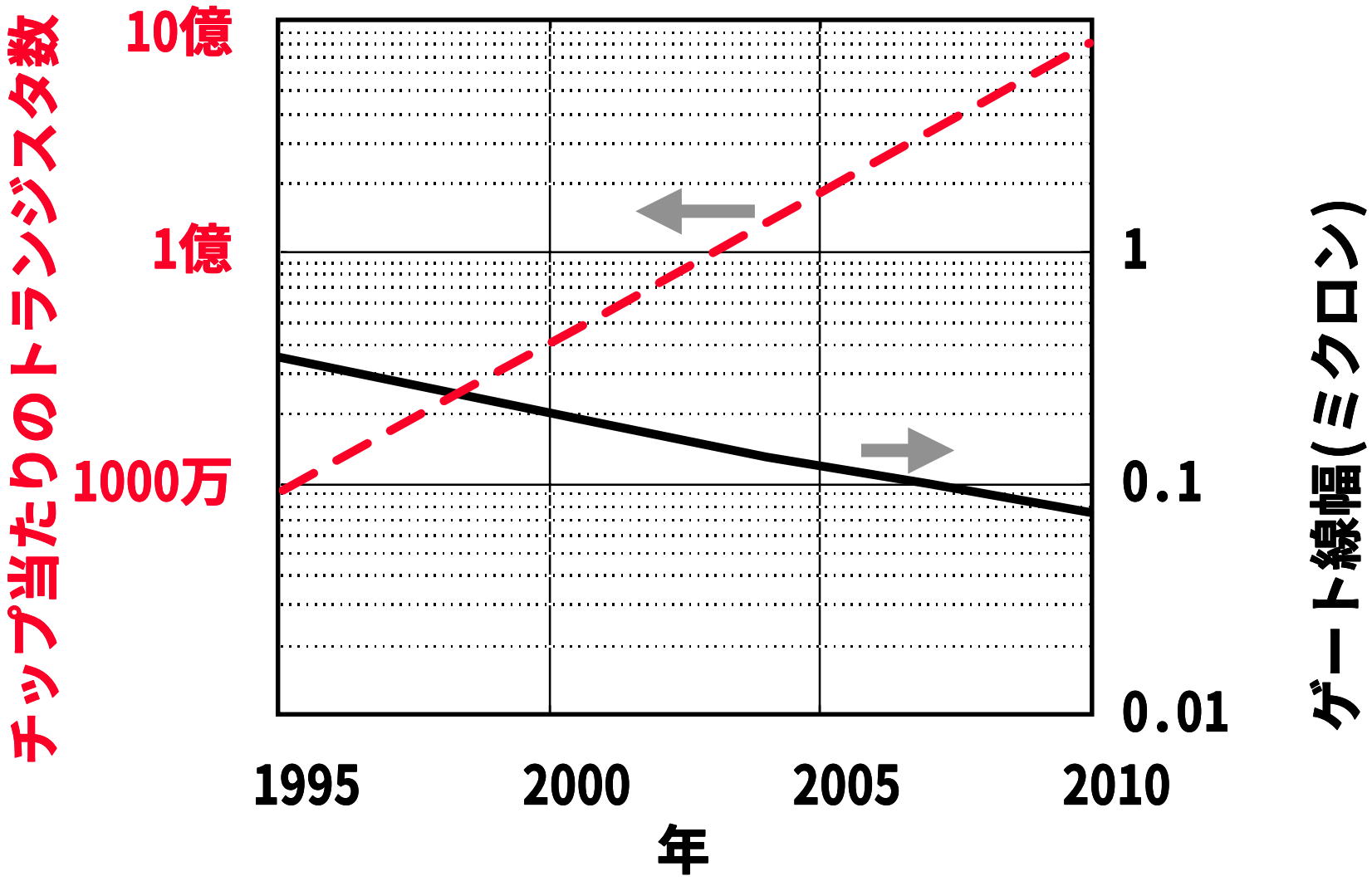
地域別半導体メーカシェア



Moore's Law


DRAM
μP
2G
1G
256M
64M
16M
4M
1M
10G
100M
1M
10K
100
1970
1980
1990
2000
2010
Year
Device count per chip
10
1
0.1
0.01
Design rule (μm)

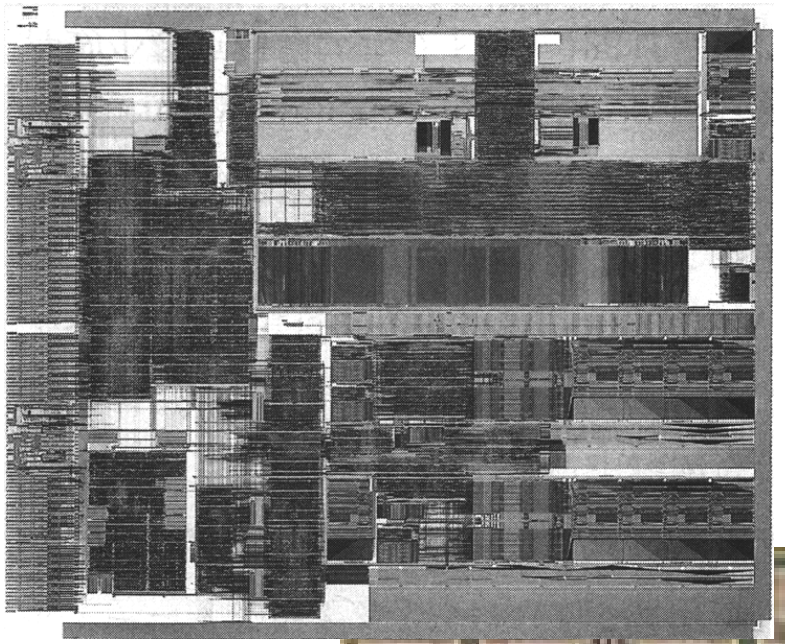
微細加工技術の進展

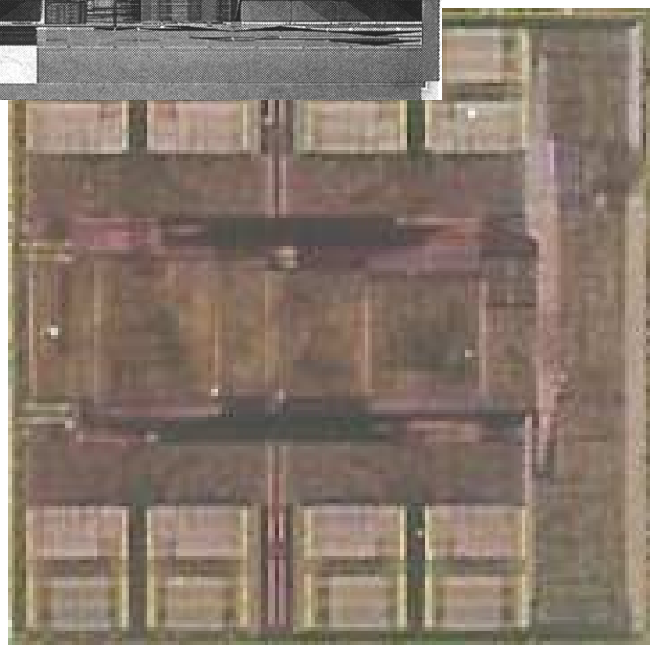

チップ当たりのトランジスタ数
10億
1億
1000万
1
0.1
0.01
ゲート線幅(ミクロン)
1995
2000
2005
2010
年

System LSI for Next Generation Games

- Clock freq. 300MHz
- 10M transistors
- Graphics synthesizer integrate

  40M tr. With embedded DRAM
- Memory bandwidth 3.2GB/s
- Floating operation 6.2GFLOPS/sec
- 3D CG 6.6M polygon/sec
- MPEG2 decode

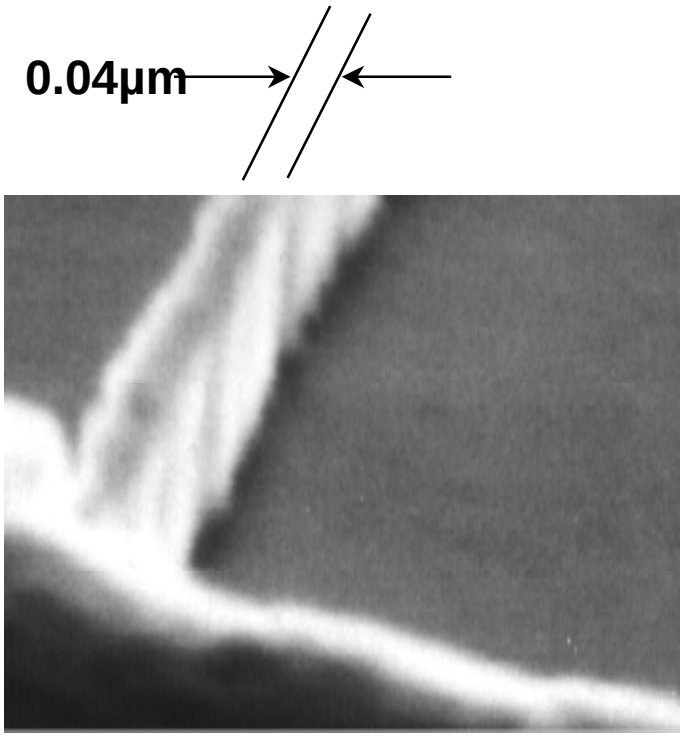


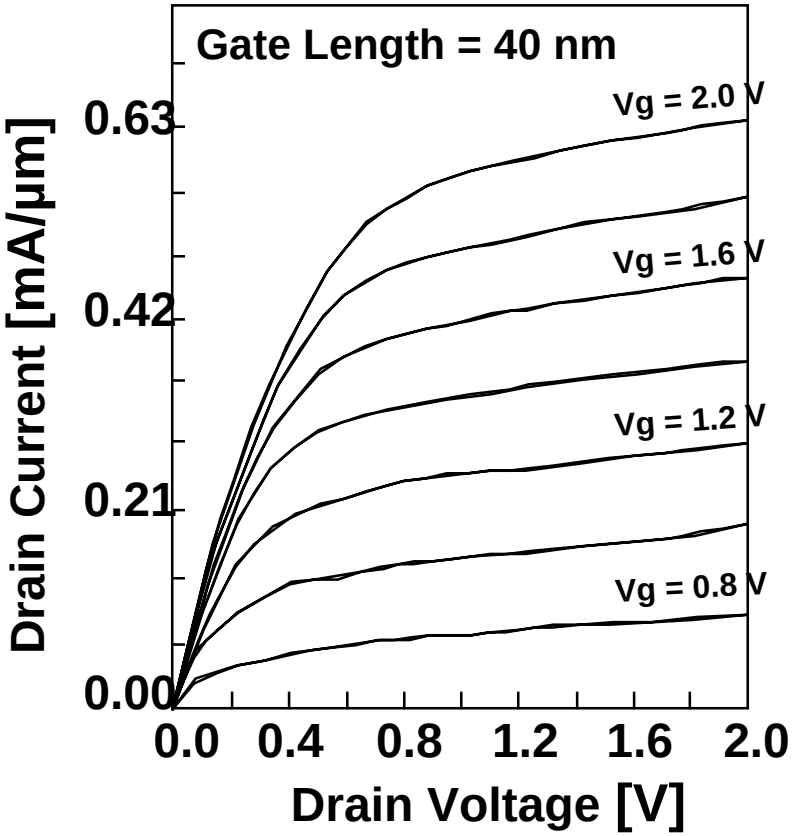


T.Sakurai

Limit of Miniturization

0.04μm MOSFET





Conventional I-V curve at 0.04μm (Even down to 0.014μm)

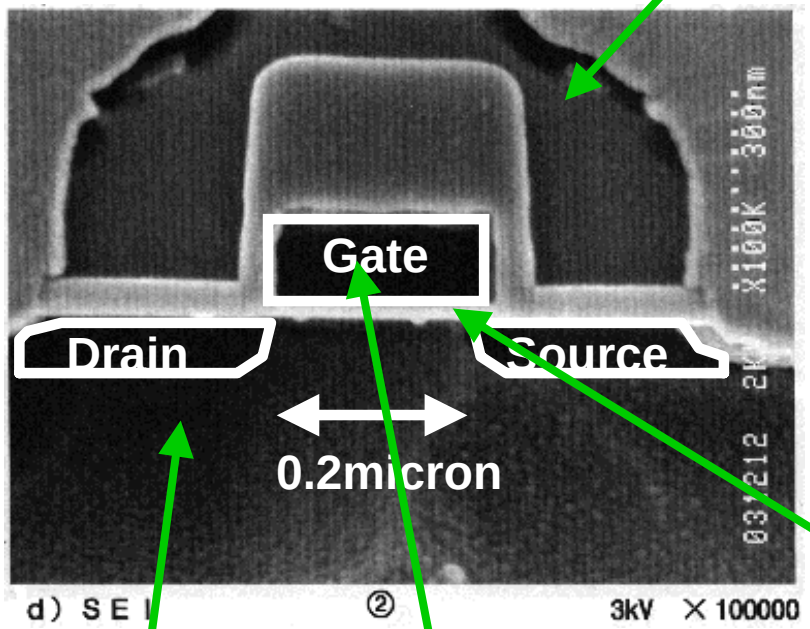
M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50nm gate Length N-MOSFETs with 10 nm Phosphorus Source and Drain Junctions", IEDM Technical Digest, pp. 119 - 122, 1993.

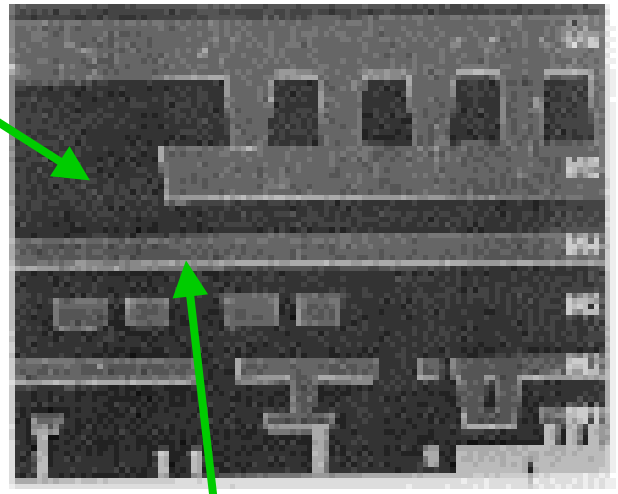
H. Kawaura, T. Sakamoto, Y. Ochiai, J. Fujita, and T. Baba, "Fabrication and Characterization of 14-nm-Gate-Length EJ-MOSFETs", Extended Abstracts of SSDM, pp.572-573, 1997.

MOSトランジスタに使われる材料

配線間、素子間絶縁：

SiO_2（なるべく低誘電率に）





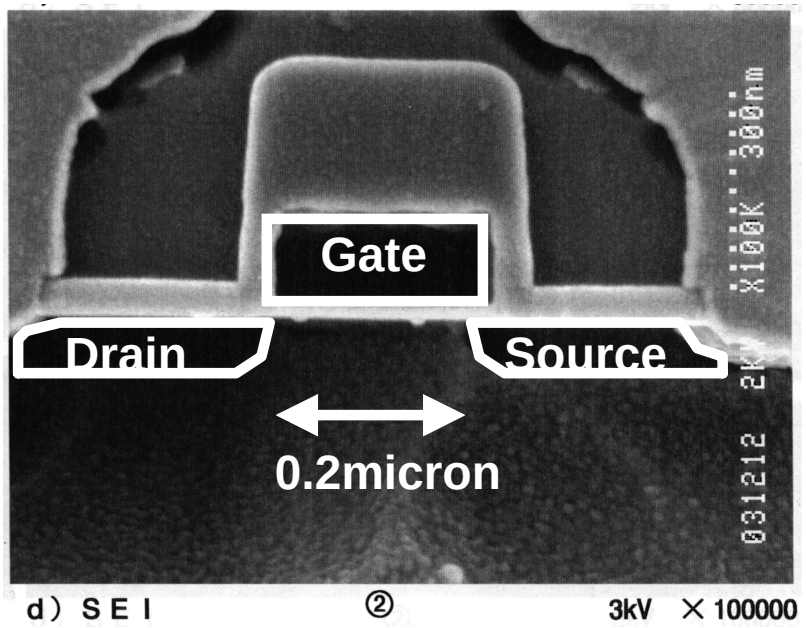
配線：　Al → Cu

ゲート絶縁膜：SiO_2（なるべく高い誘電率に）

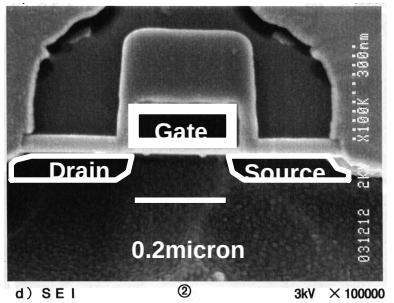
基板：　Si

ゲート：　多結晶Si　→ 高融点金属

Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

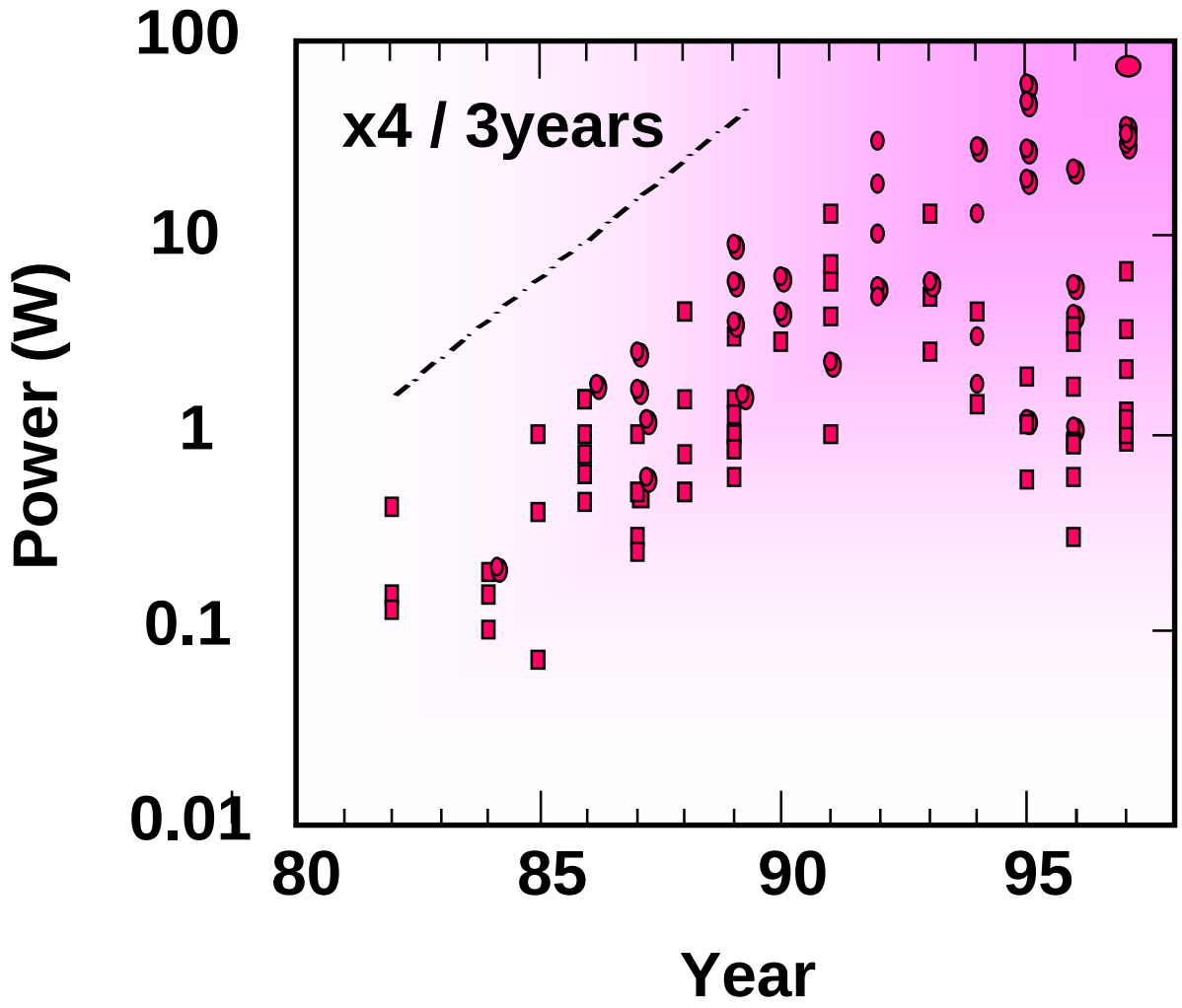
T.Sakurai

Three crises in VLSI designs

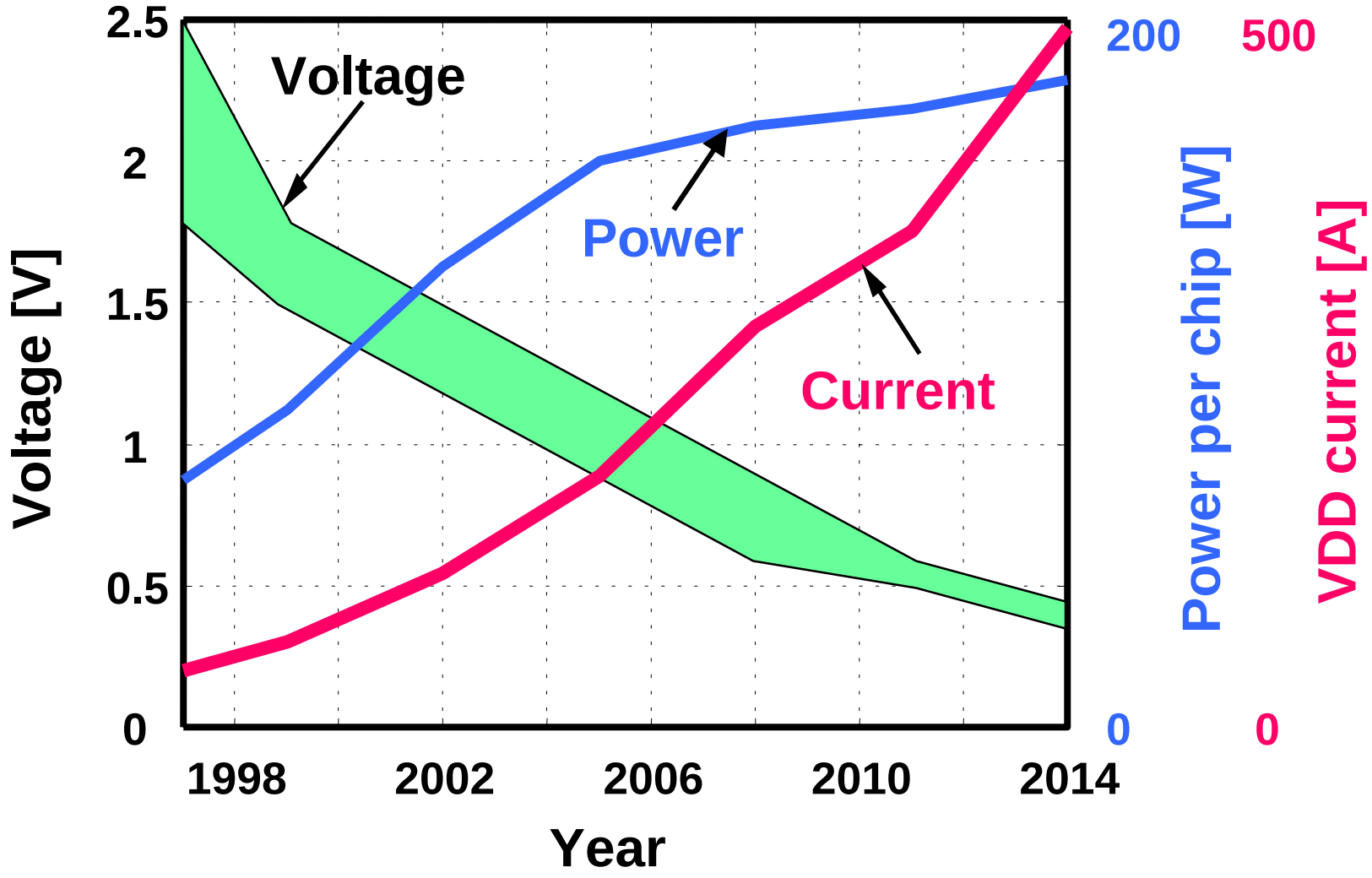
- Power crisis
- Interconnection crisis
- Complexity crisis

Ever Increasing VLSI Power

(Power consumption of processors published in ISSCC)



VDD, Power and Current Trend



International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

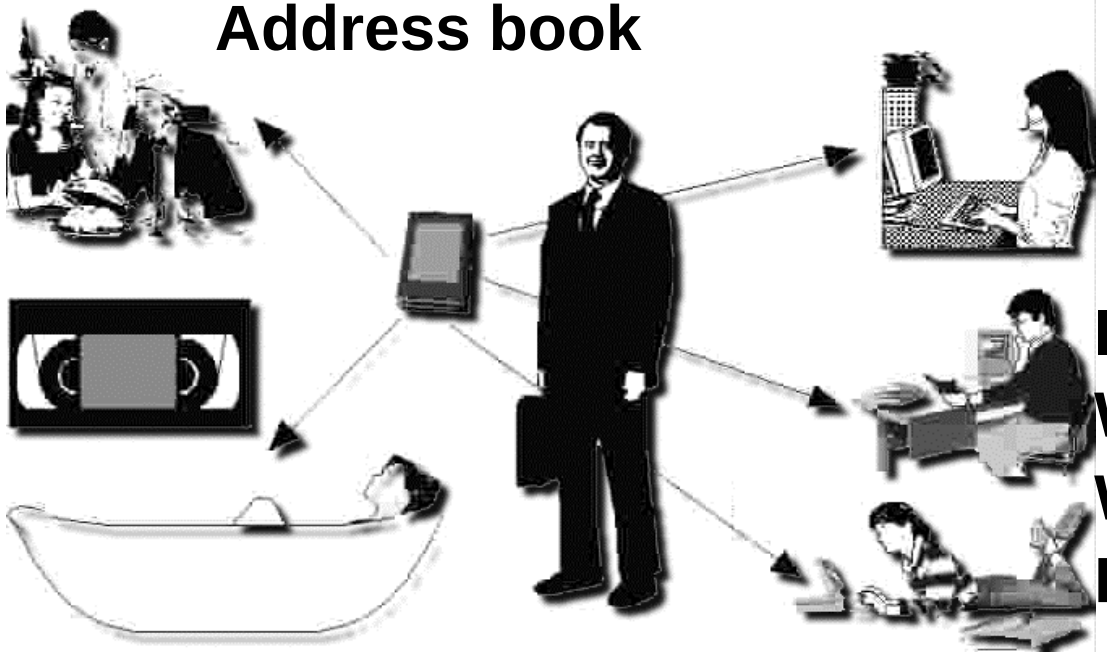
T.Sakurai

IT from anywhere by anybody

Low-power and wireless are the keys

Cell phone
Tecketing
Reservation

PDA
Schedule
Address book



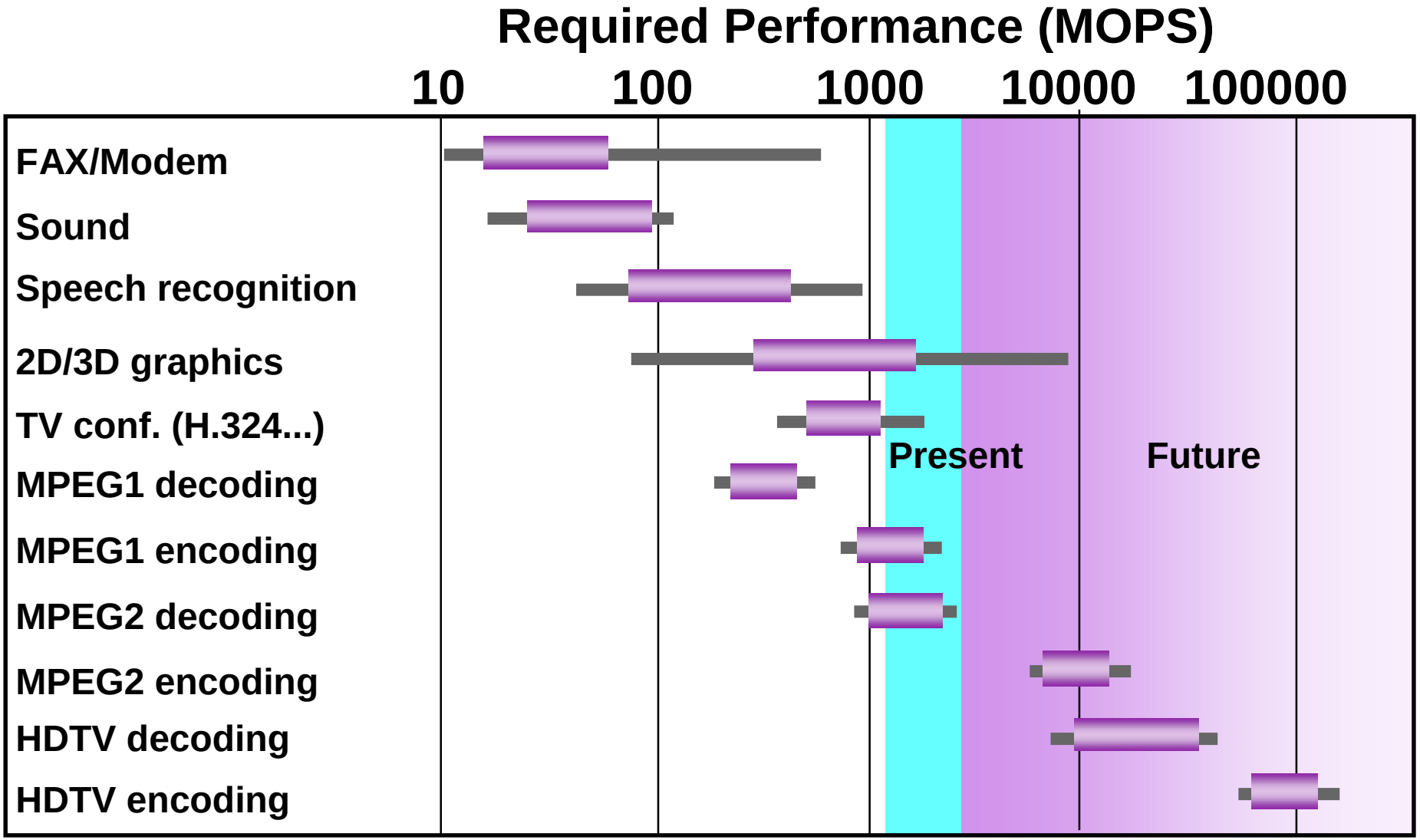
E-cashing
E-trading
E-banking

Internet
Web brouse
Web TV
E-mail

Home automation
Game on net
Entertainment

Computer centric →
Communication centric,
Display centric

Performance Requirements for Multimedia



What sets the technology trend?

- NMOS → CMOS

  Cost up

- Bipolar → CMOS

  Speed down

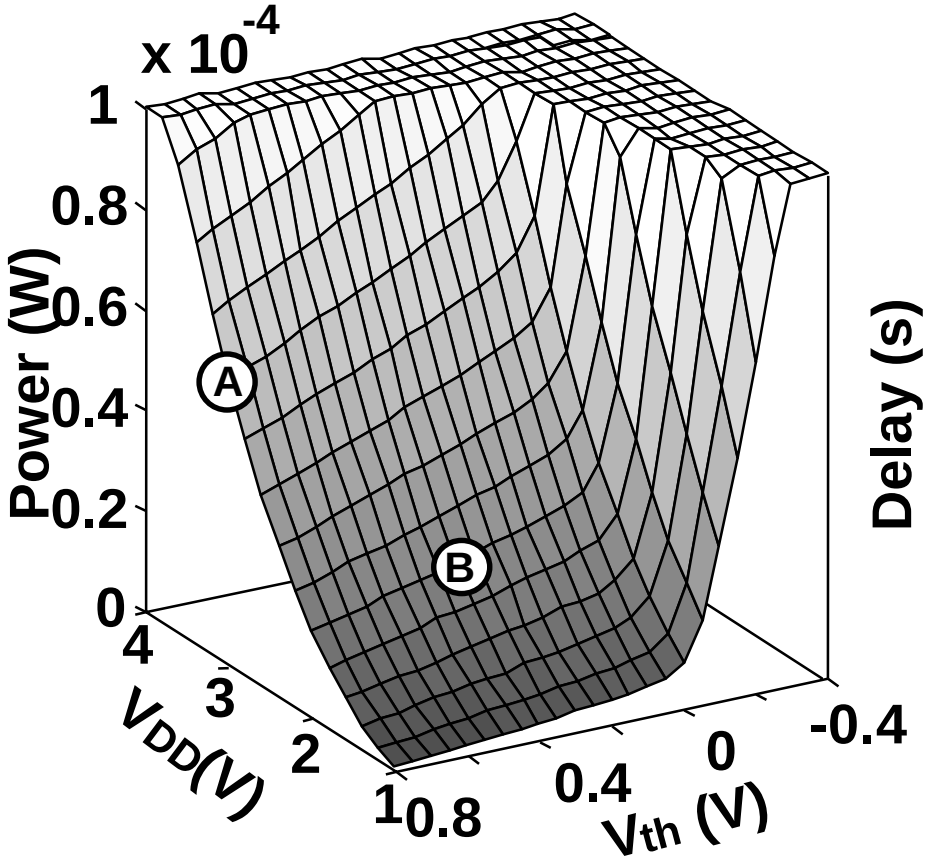
- Not cost nor speed but power set the technology trend.

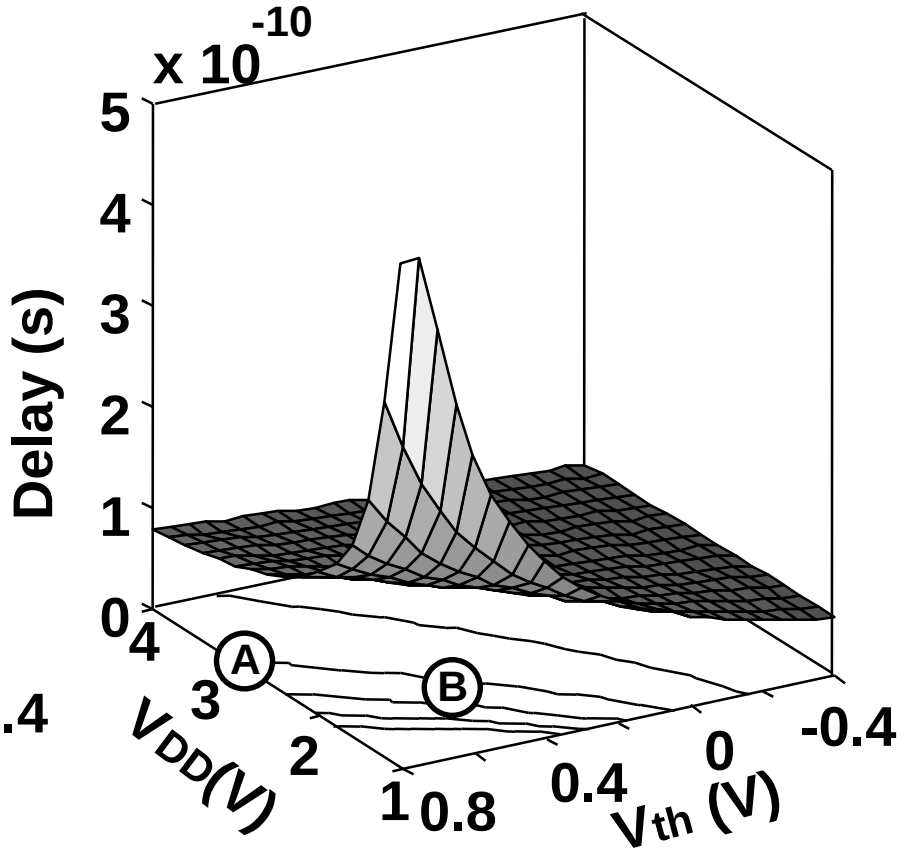
- Integration can achieve low cost and high speed as a system.

Power & Delay Dependence on V_{DD} & V_{TH}

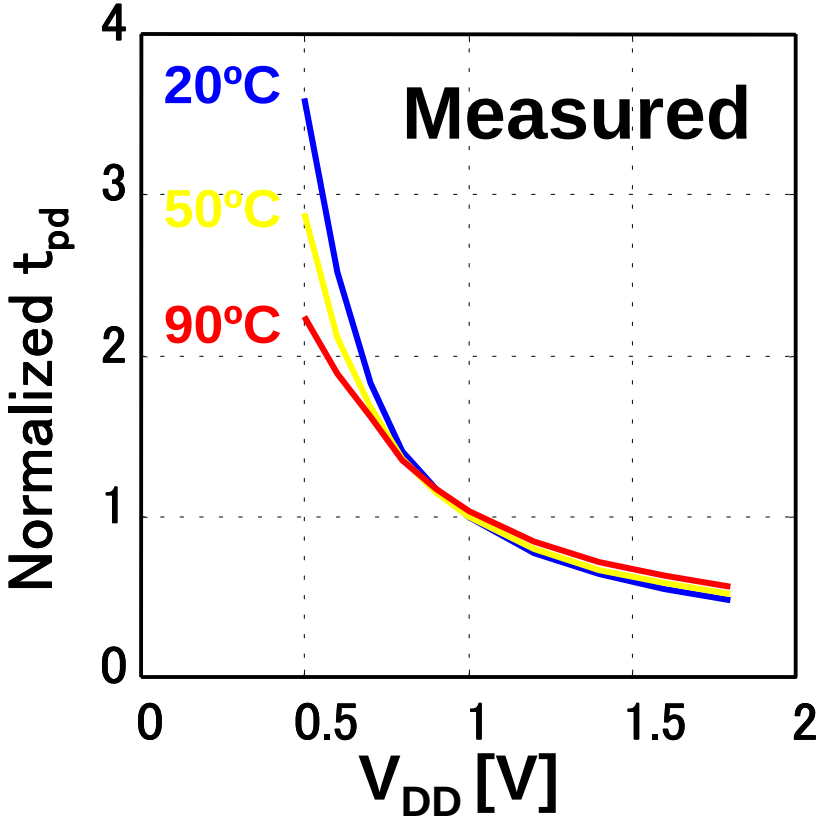
Power : $P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{th}}{S}} \cdot V_{DD}$

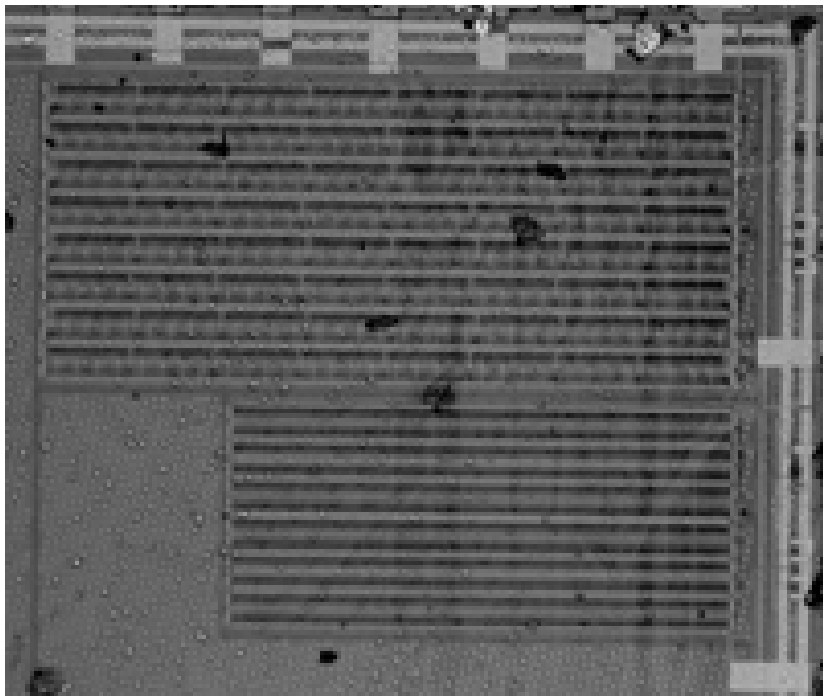
Delay $= \frac{k \bullet Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^{\alpha}}$ $(\alpha=1.3)$





Measurement of 32bit full adder



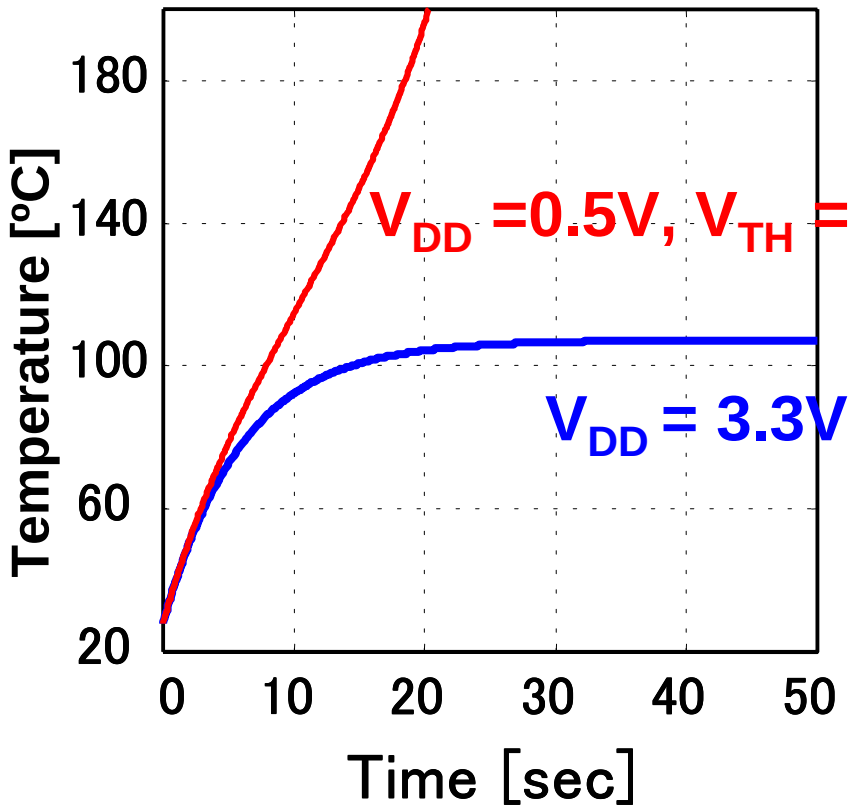


Photograph of 32bit FA

0.3μm CMOS

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

Transient response of chip temperature



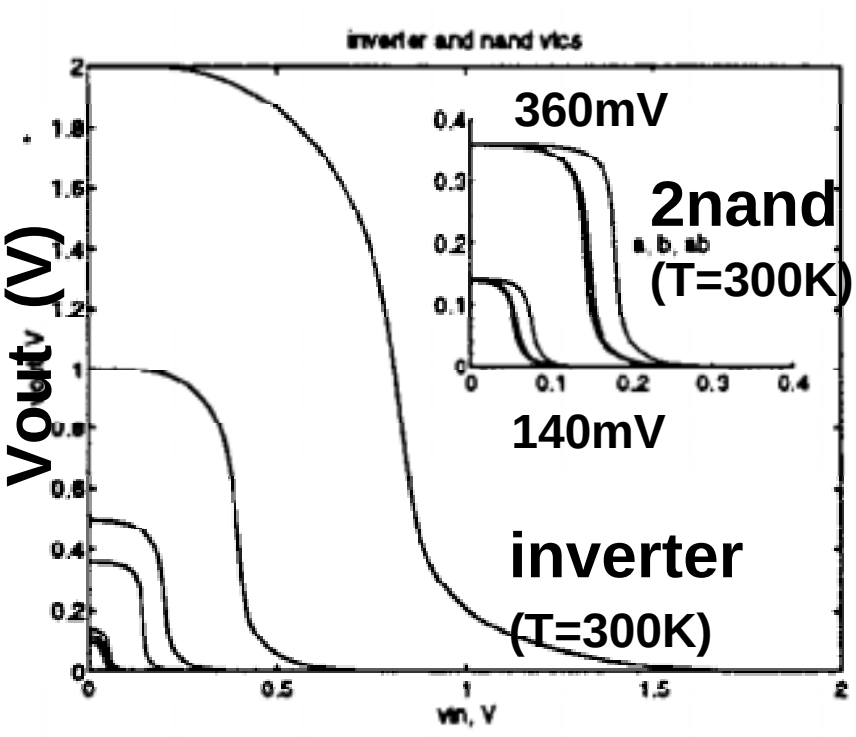
- Same package
- Same power at room temp.

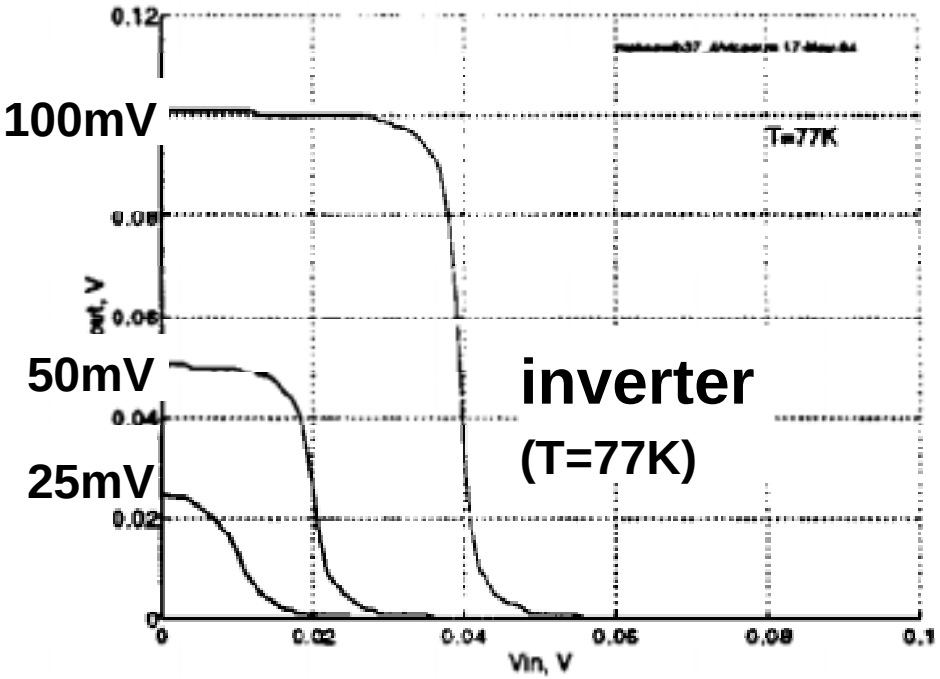
Better package is needed to avoid thermal runaway in low voltage.

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

Ultra Low-Voltage Operation

(Stanford Univ.)

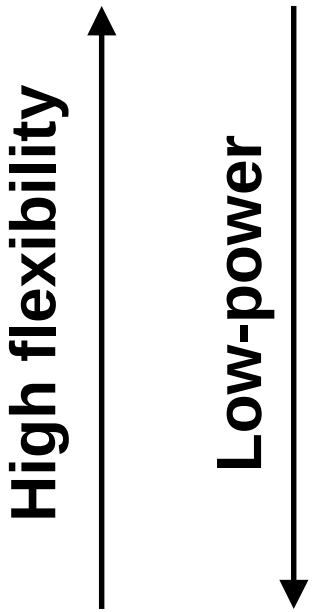




J.Burr&J.Shott,"A 200mV Self-Testing Encoder/Decoder using Stanford Ultra-Low-Power CMOS",ISSCC94, pp.84-85.

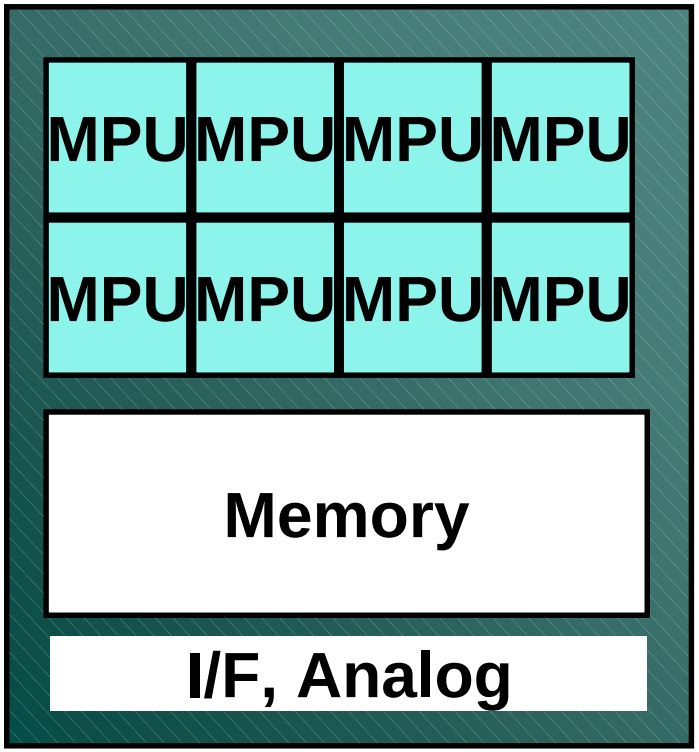
Approach to low-power LSI

Example of MPEG2 decoding



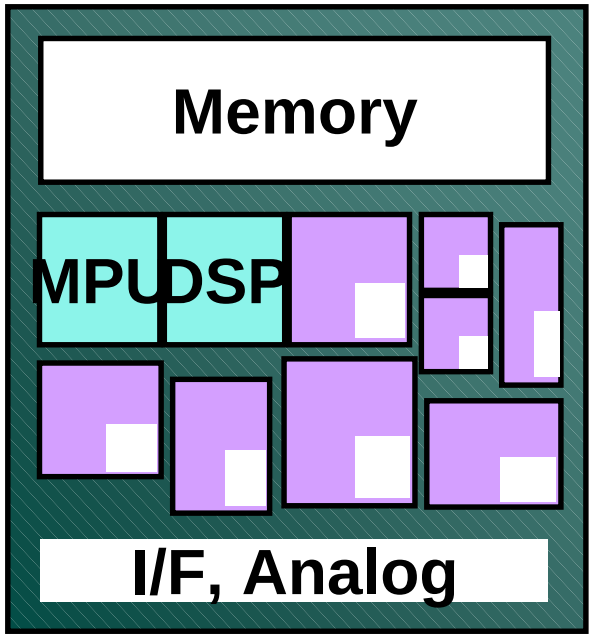
- Processor (software)
  ～25W
- DSP
  ～4W
- Dedicated sytem LSI (SW/HW)
  ～0.7W

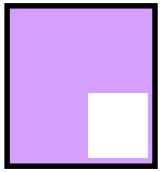
Homogeneous vs. Heterogeneous



Homogeneous Architecture

(High flexibility)



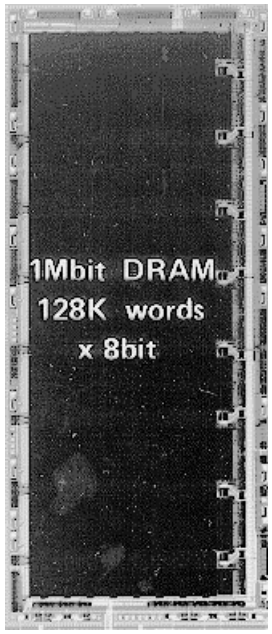


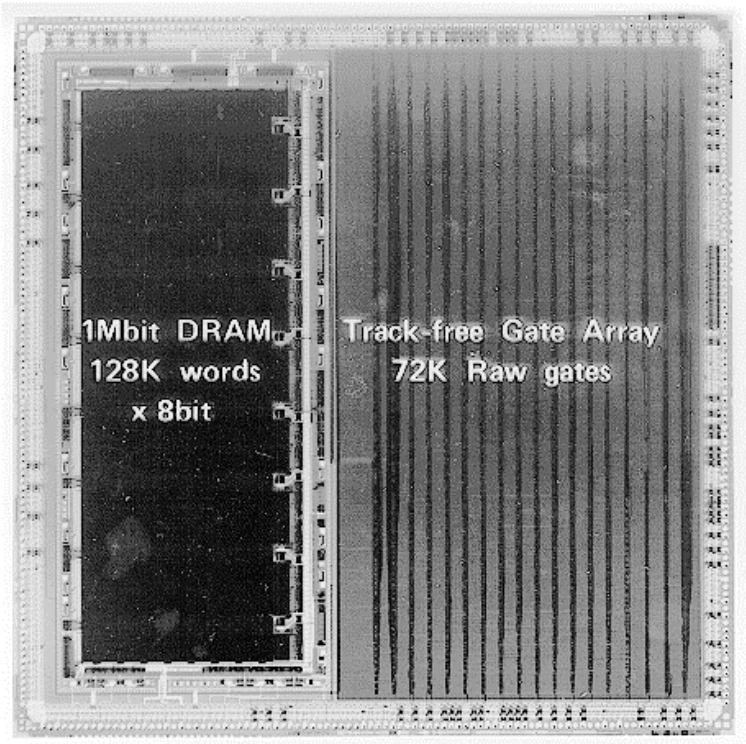
Special Engine

Heterogeneous Architecture (System LSI)

(Low-power, more efficient)

DRAM Embedding



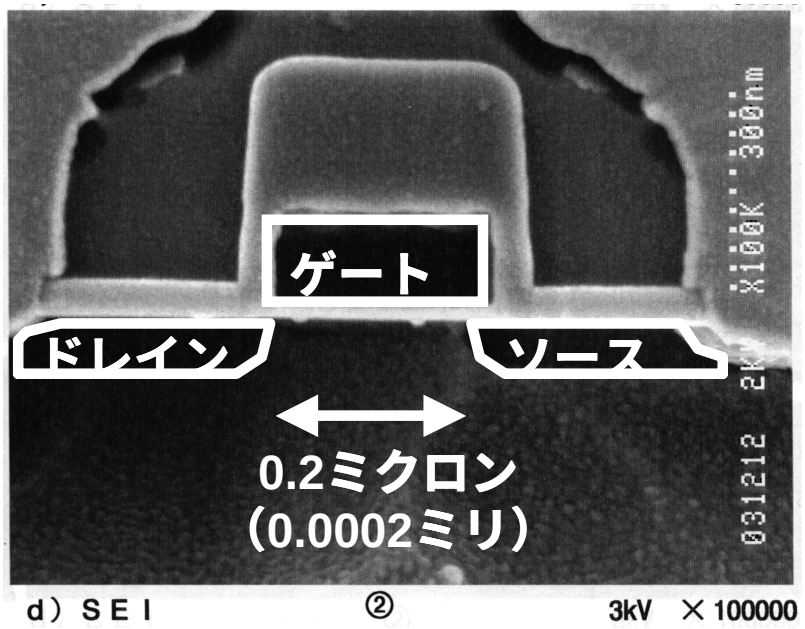


DRAM **Processor** **System LSI**

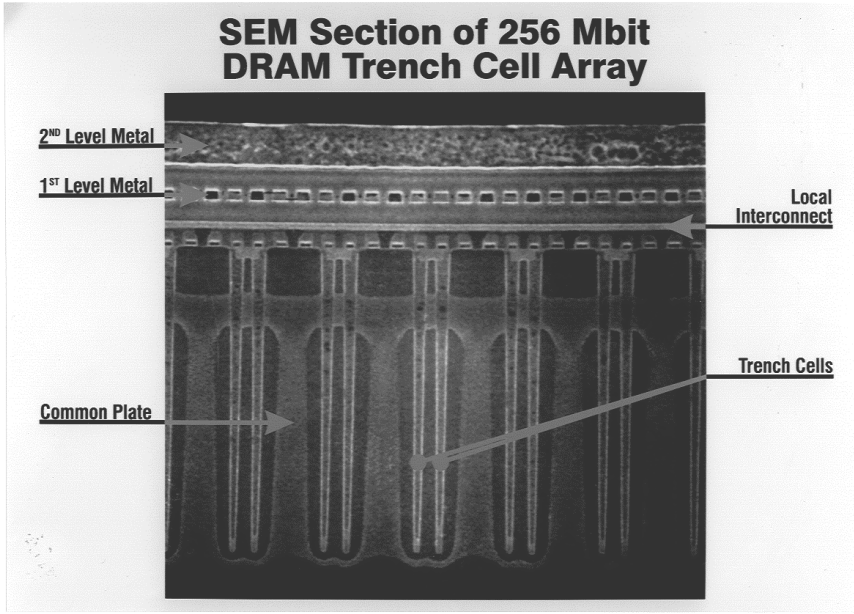
K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- **Two orders of magnitude improvement in bandwidth and power**

DRAM混載



トランジスタ

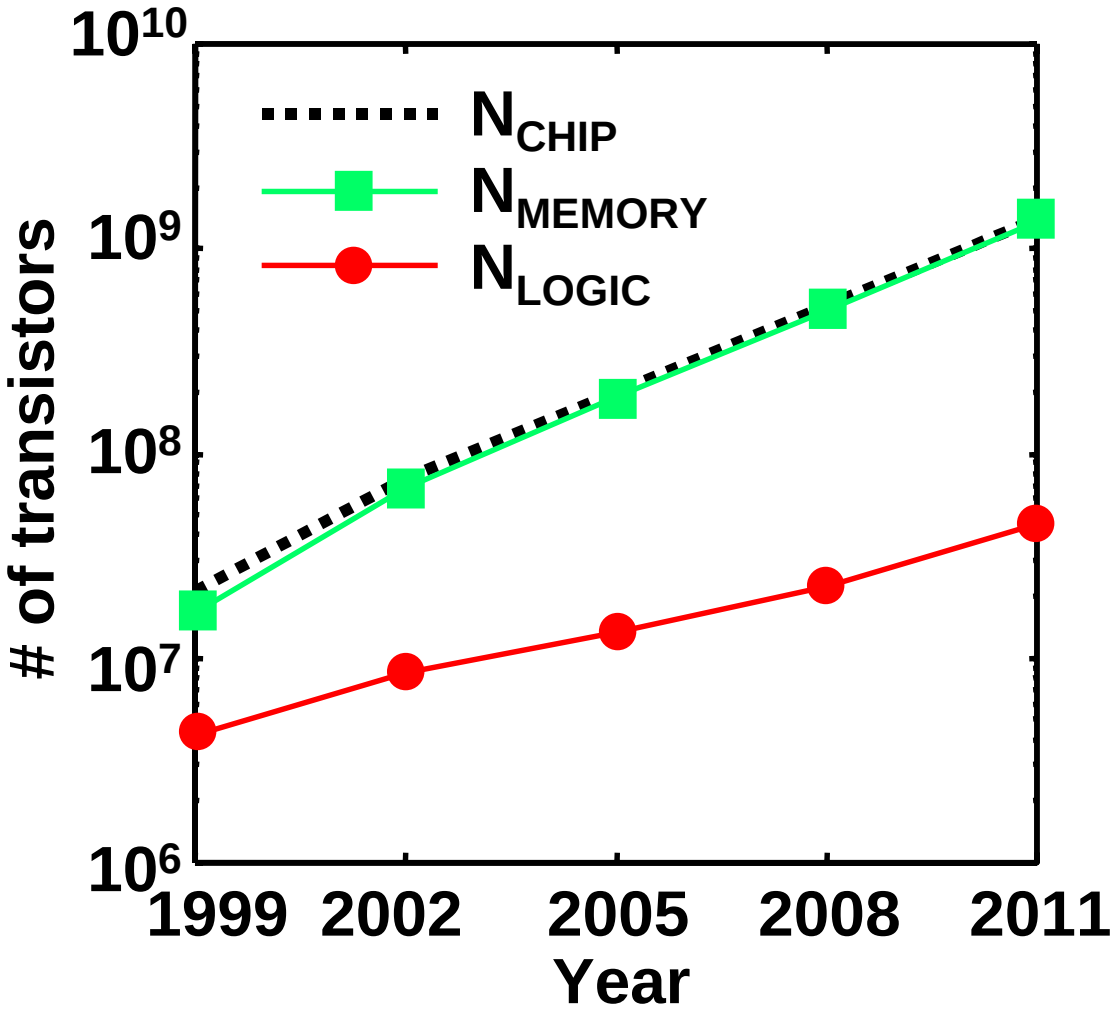


DRAMのメモリセル

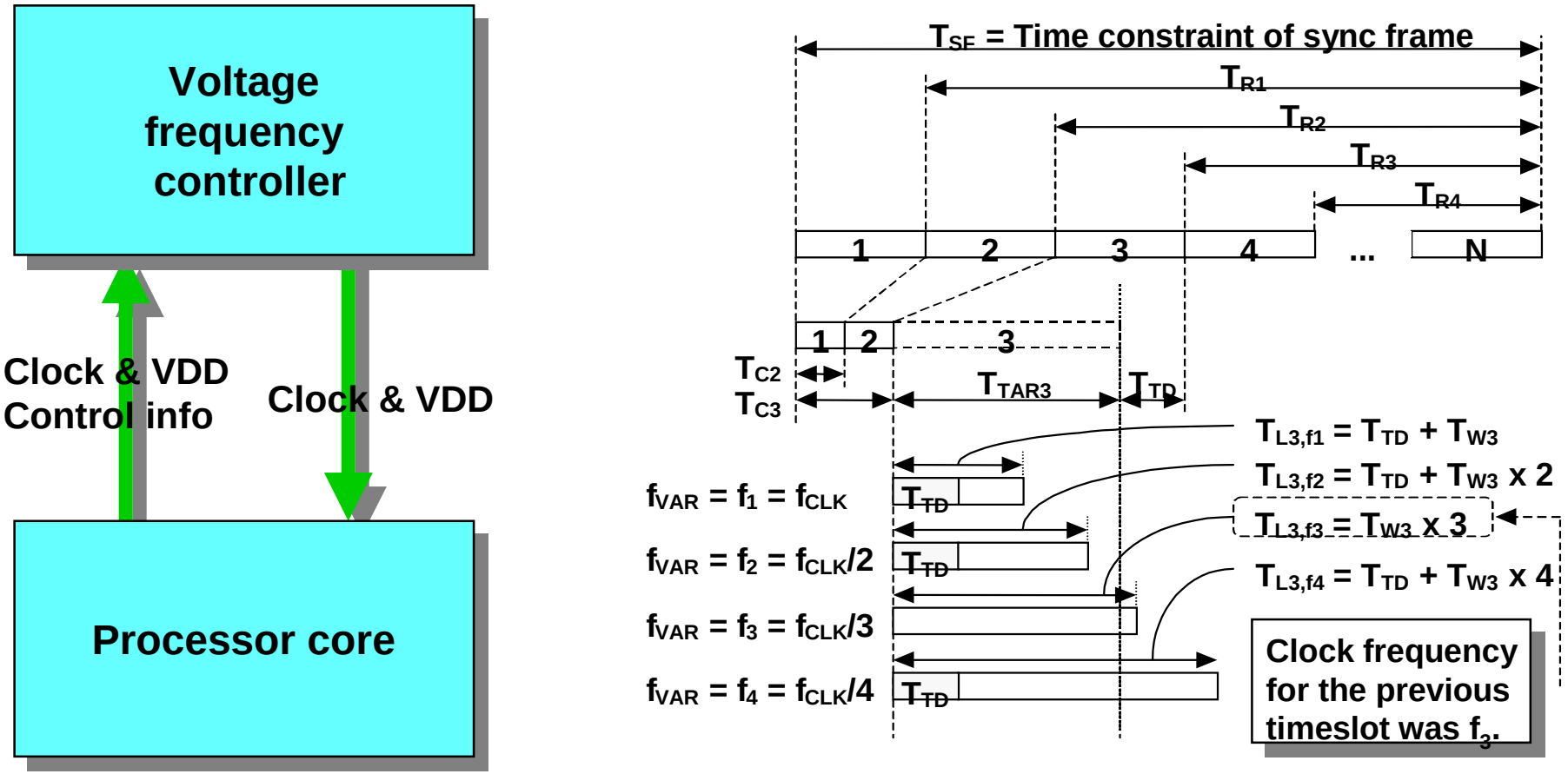
- 異なる技術を結合
- テストはBISTを活用
- 自動モジュールジェネレータ

Future trend of N_{LOGIC} and N_{MEMORY}

	1999	2011
$\frac{N_{LOGIC}}{N_{CHIP}}$	20%	3%
$\frac{N_{MEMORY}}{N_{CHIP}}$	80%	97%



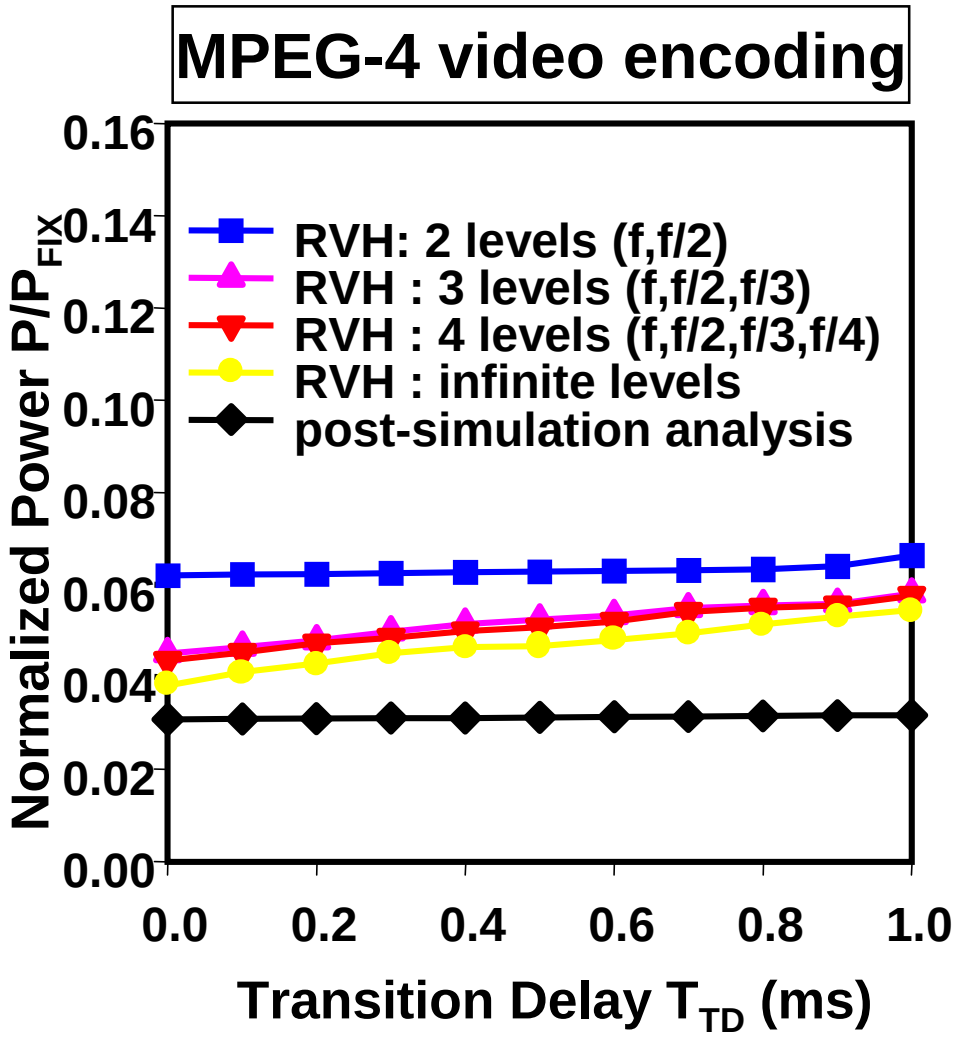
Application slicing and software feedback loop in Voltage Hopping

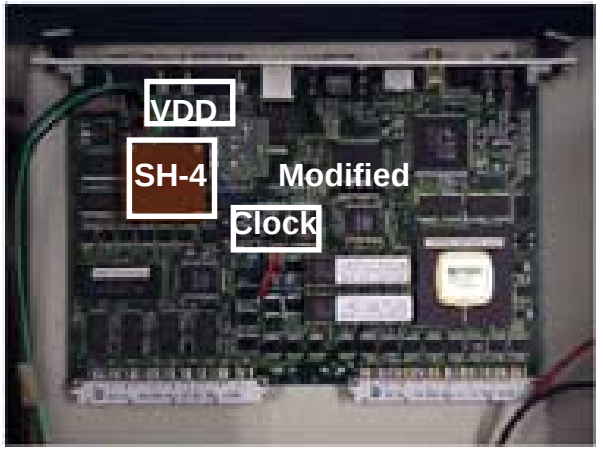


S.Lee and T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications,"ASPDAC'00, A5.2, pp.381~pp.386, Jan. 2000.

S.Lee and T.Sakurai, "Run-time Voltage Hopping for Low-power Real-time Systems," DAC'00, June 2000.

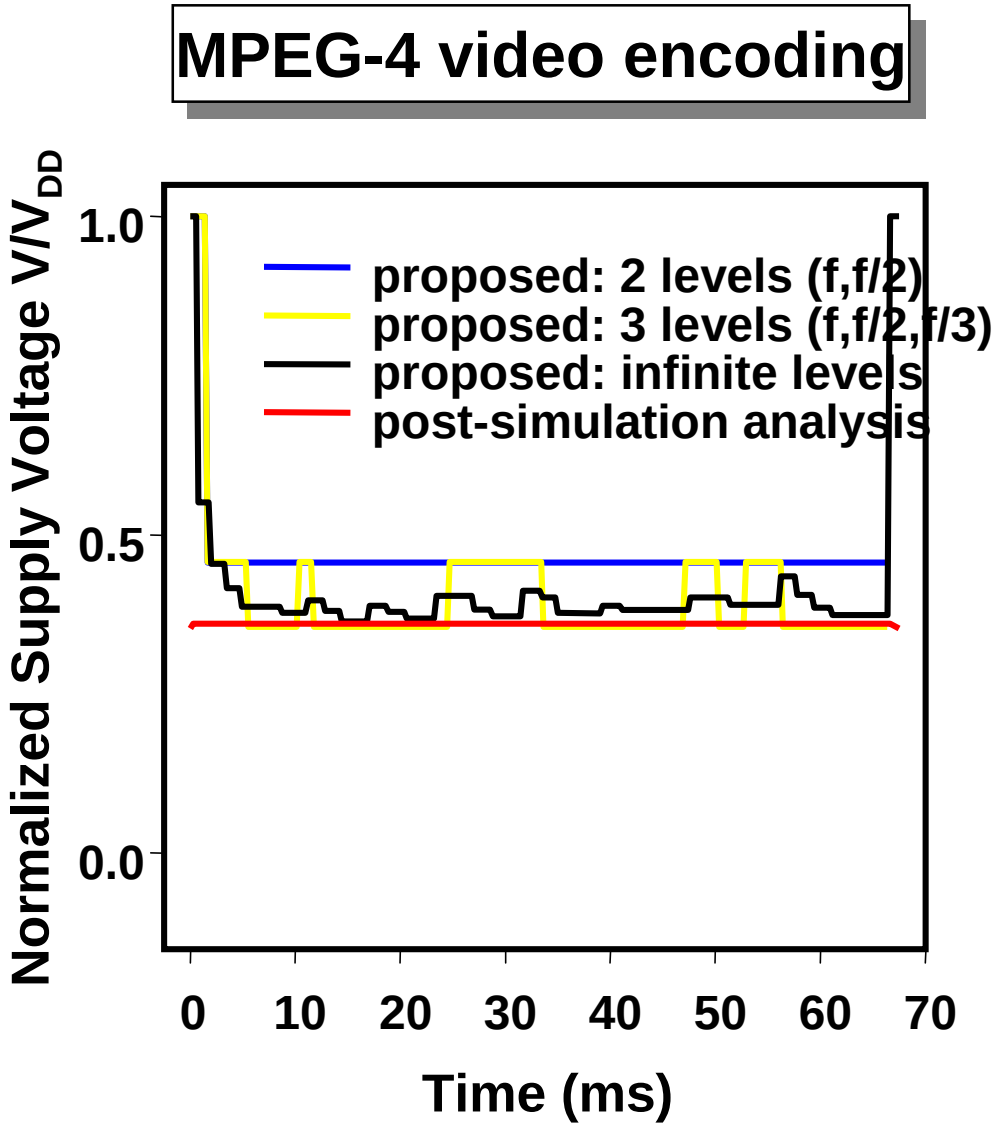
Run-time Voltage Hopping reduces power to less than 1/10





T.Sakurai

Transient voltage waveform



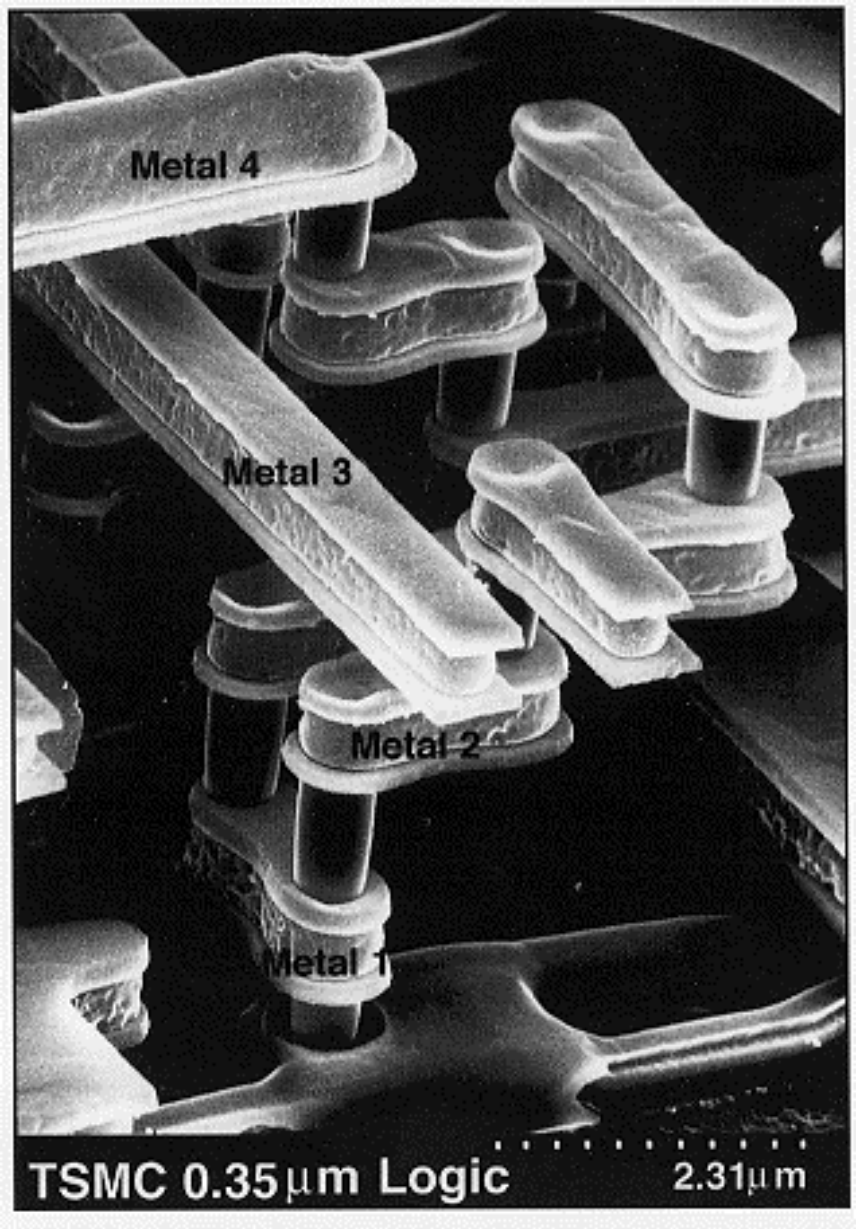
Simulation results

1 sync frame = 33 timeslots = 66.66667 ms

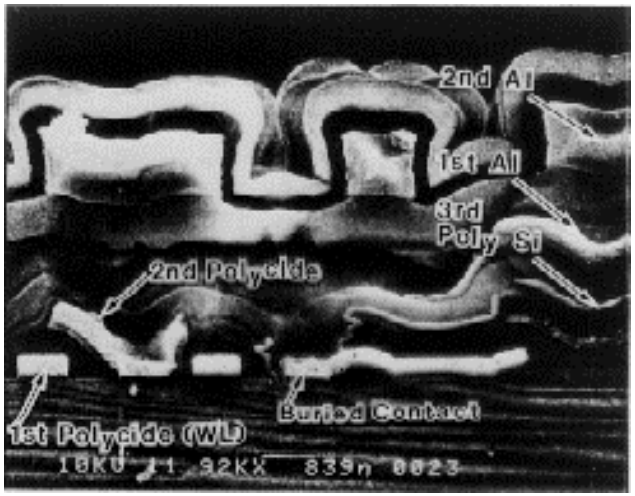
Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

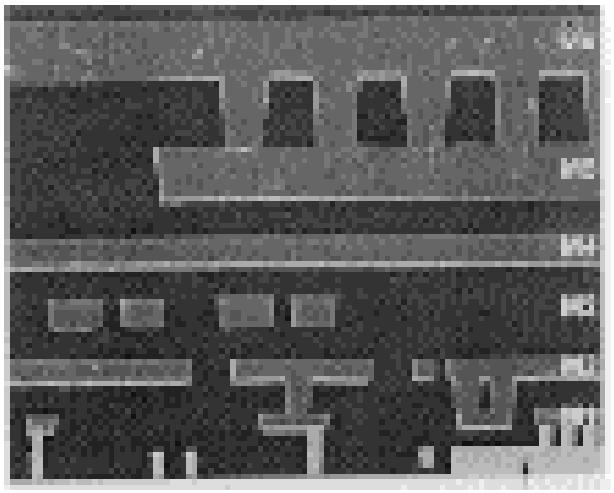
Complex interconnect



Advances in interconnection technology



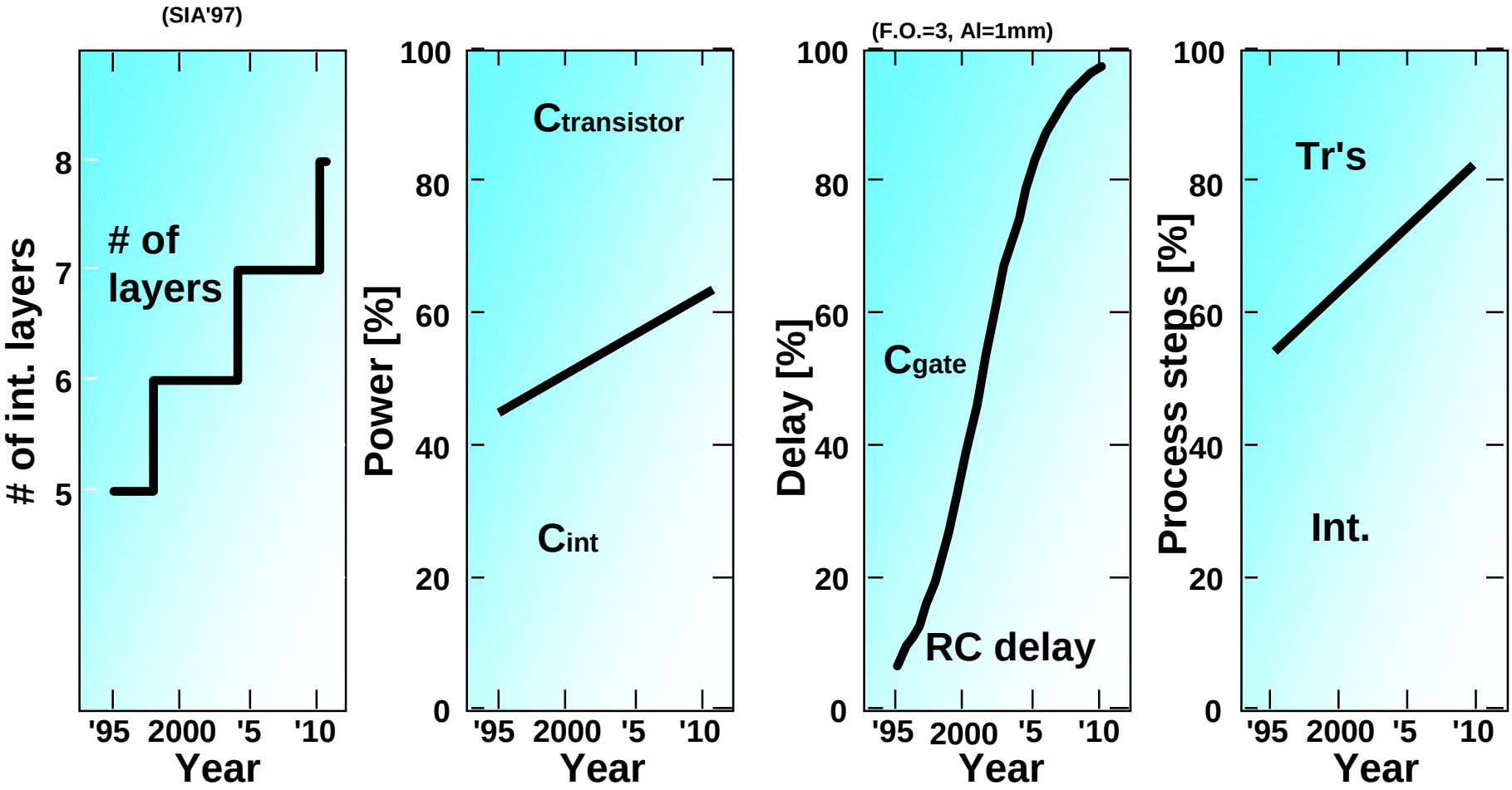
Interconnection in 1985



Interconnection in 1998

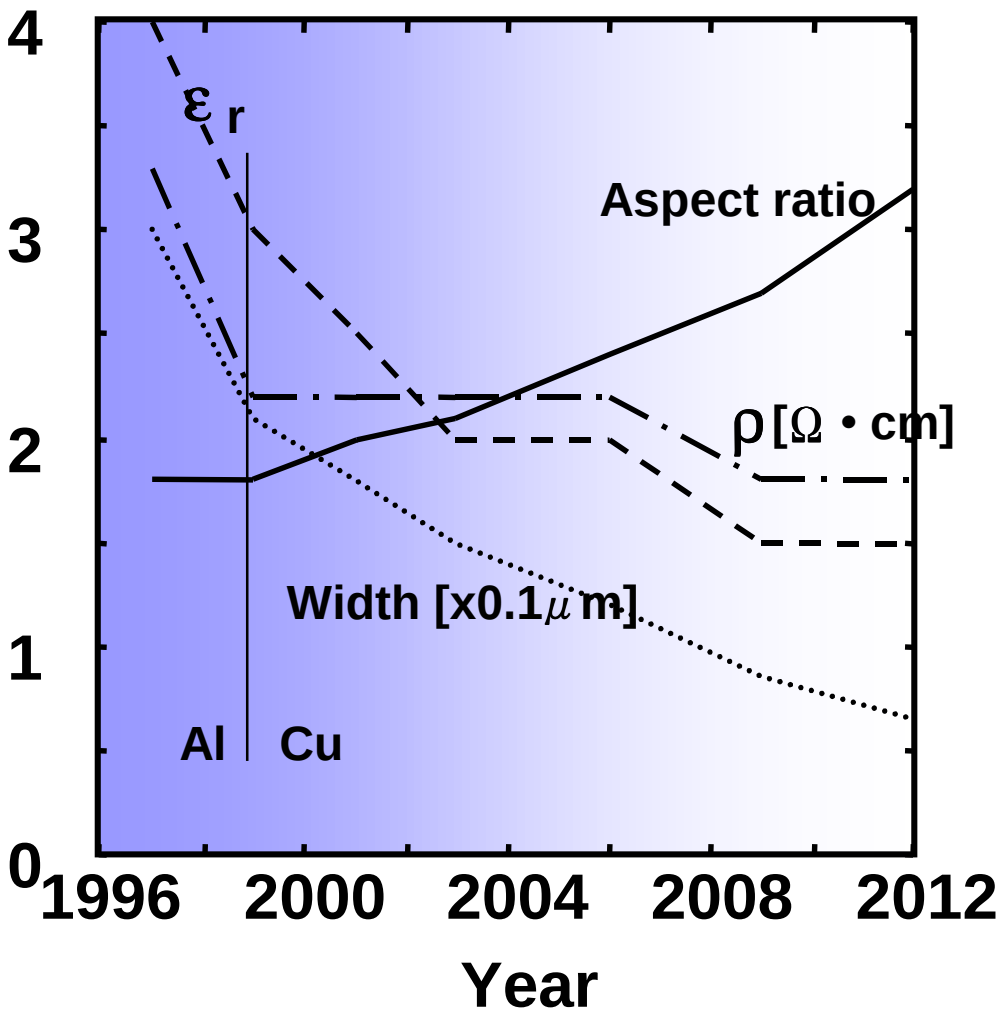
Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



T.Sakurai

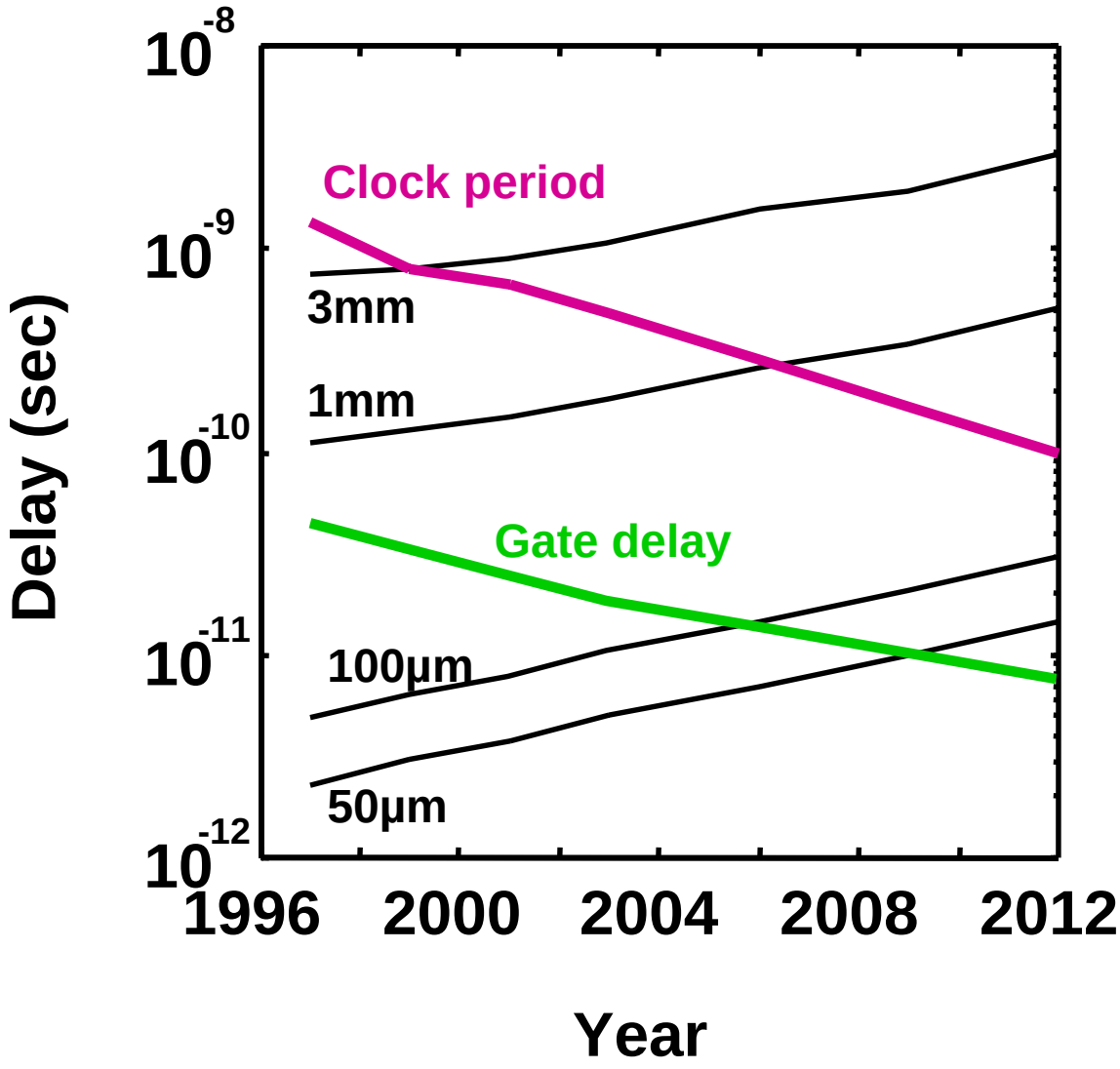
Interconnect parameters trend



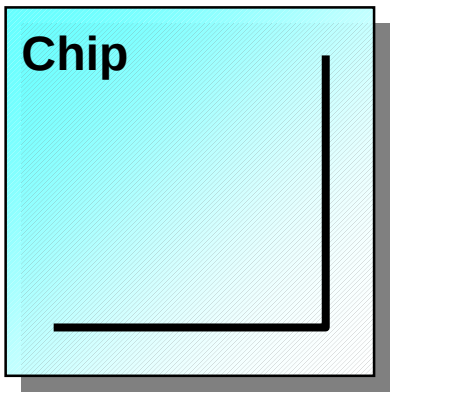
Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

T.Sakurai

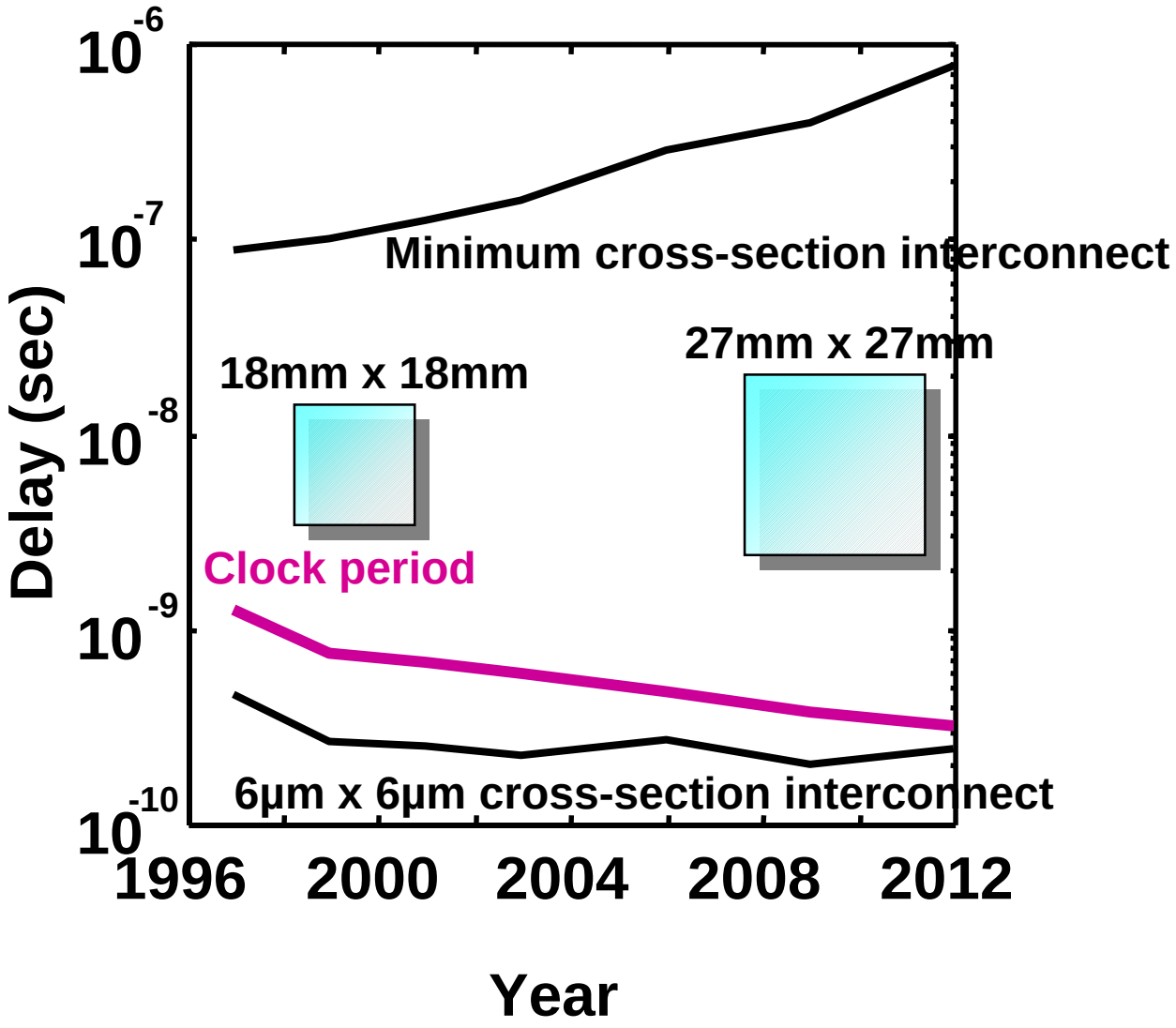
RC delay and gate delay



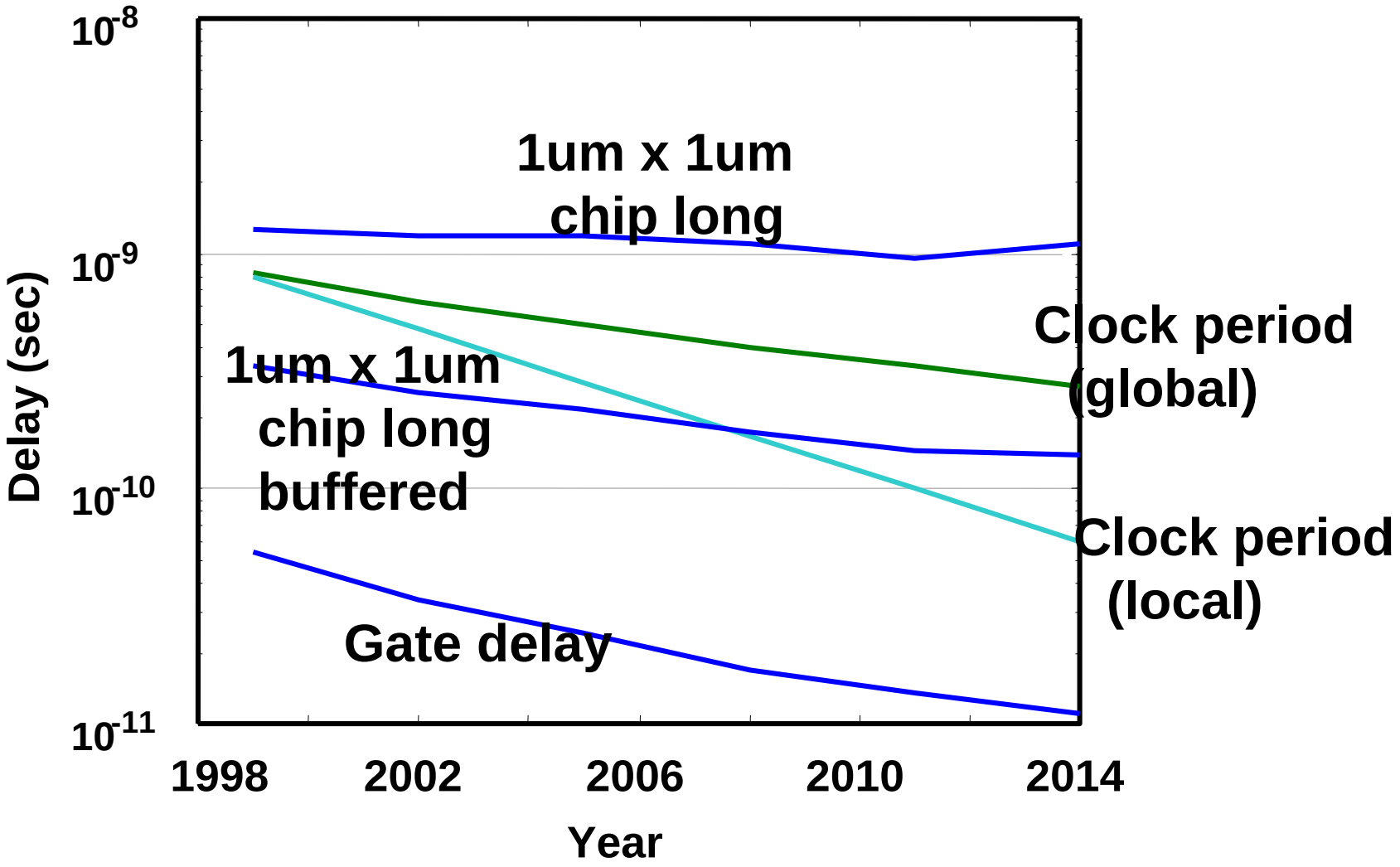
RC delay of global interconnections



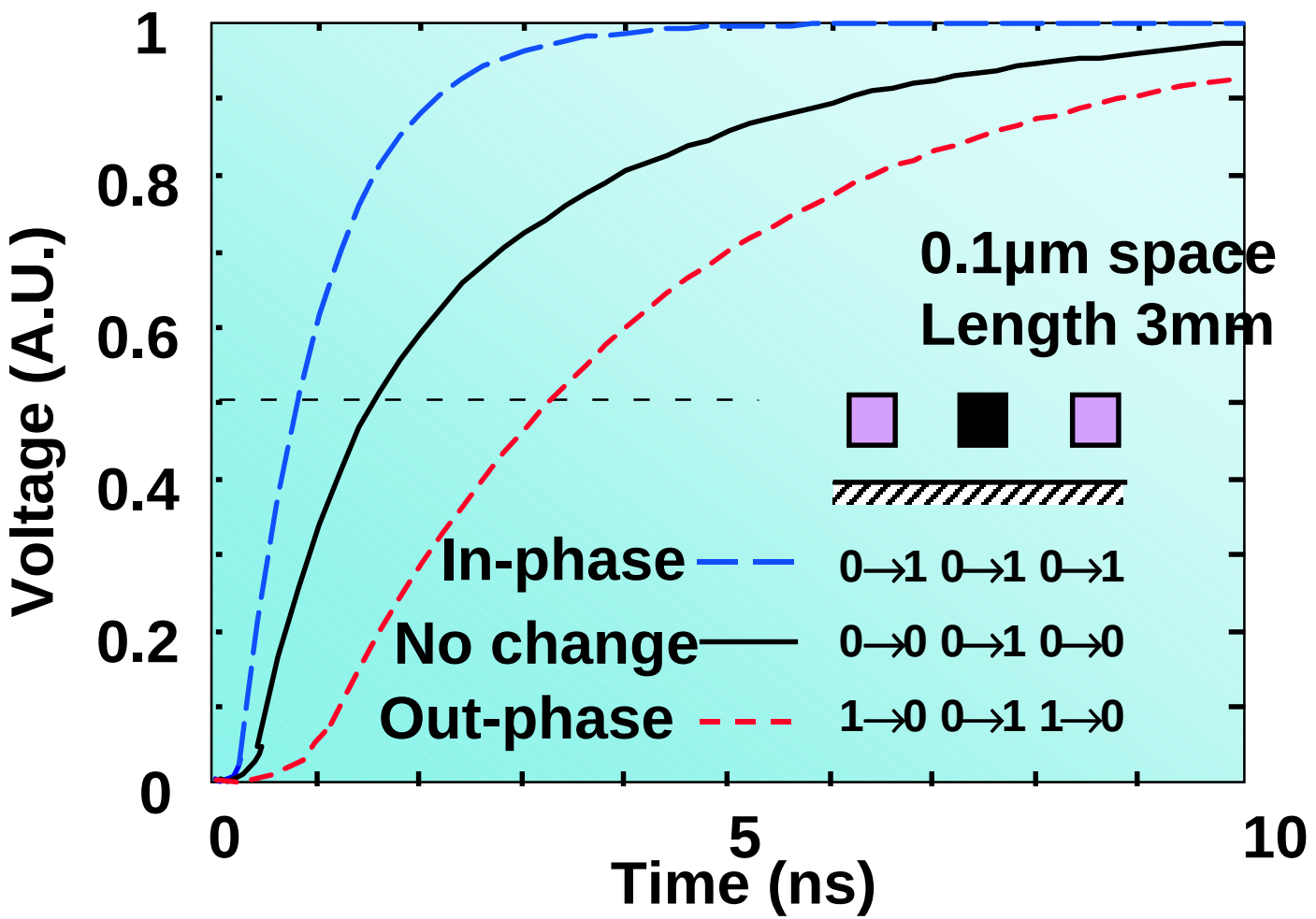
Global interconnect



Buffered interconnect delay



Coupling among Interconnection

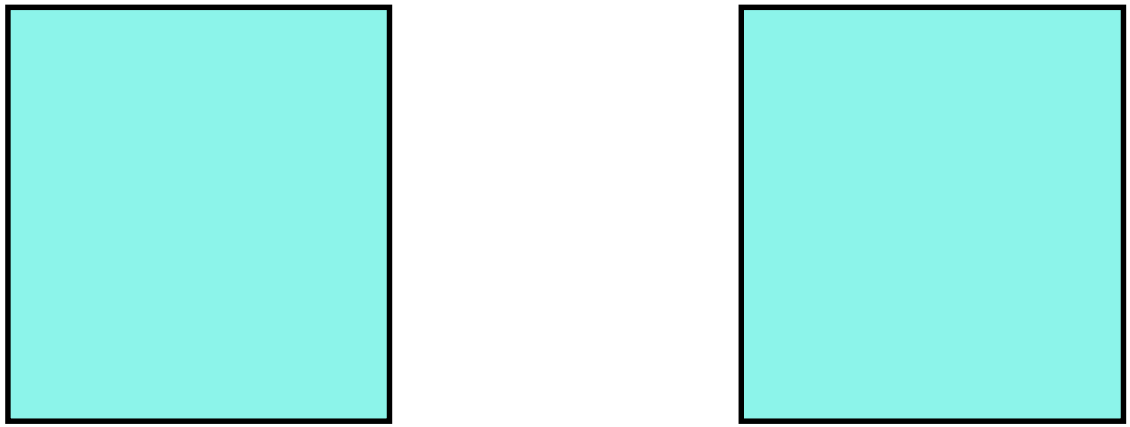


Difficulty in checking setup and hold time.

Interconnect Cross-Section and Noise

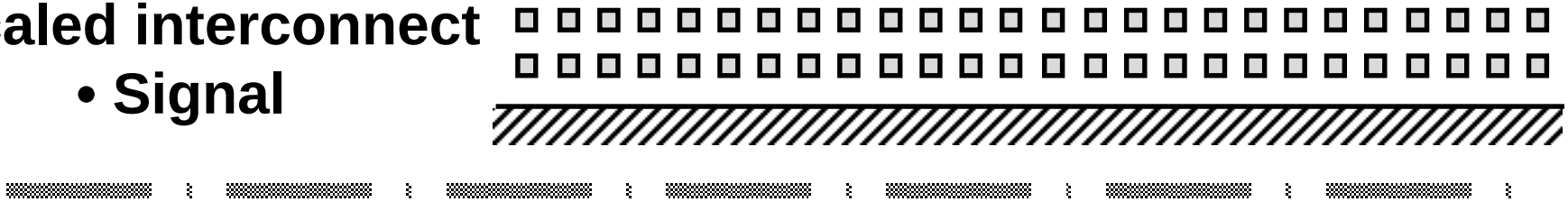
Unscaled / anti-scaled

- **Clock**
- **Long bus**
- **Power supply**



Scaled interconnect

- **Signal**



1V 50W -> 50A current

5% noise -> 0.05V noise -> 1mΩ sheet R -> 15μm thick Cu

Area pad + package, or thick layer on board is needed.

Three crises in VLSI designs

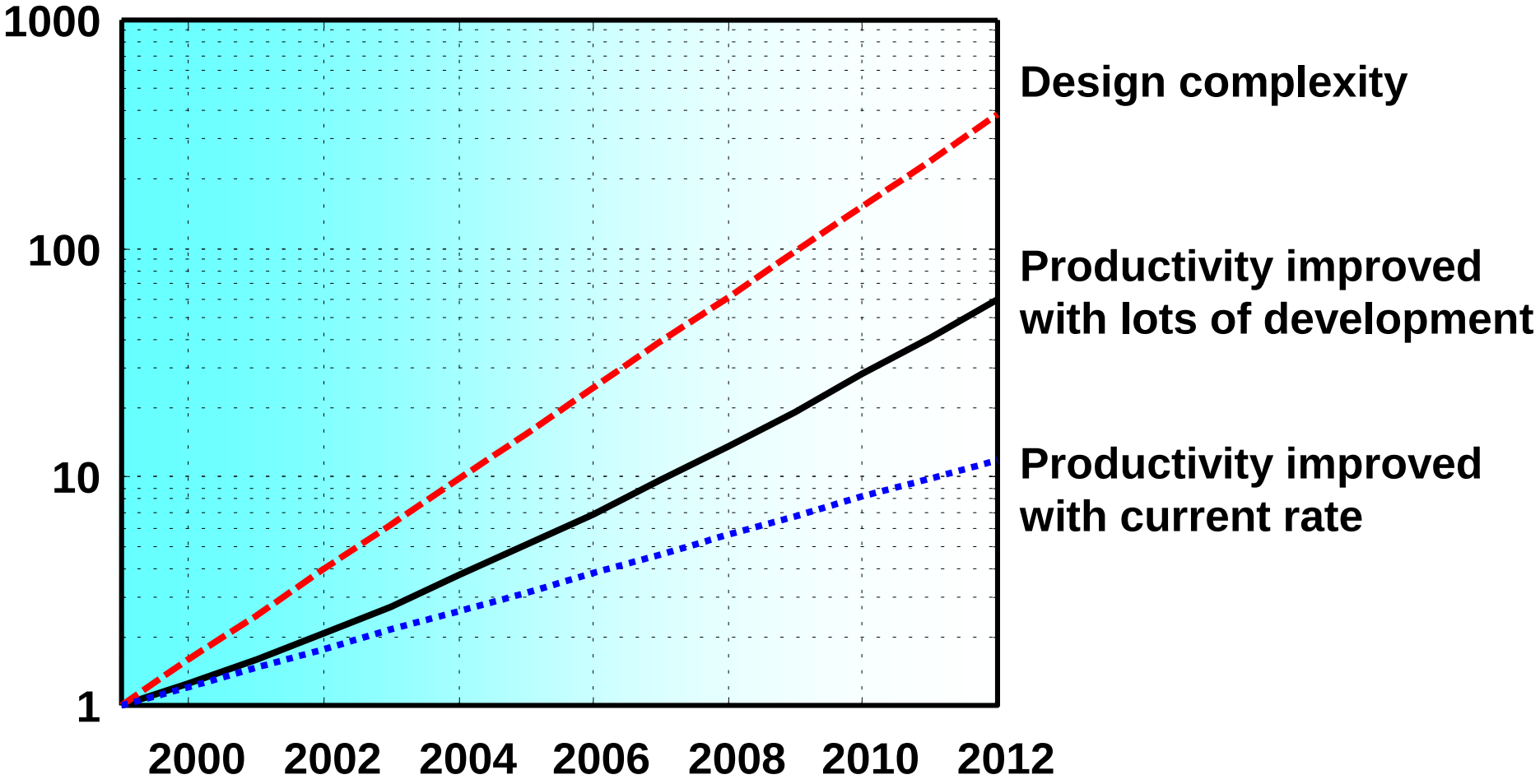
- Power crisis
- Interconnection crisis
- Complexity crisis

VLSI Design in 2010

Designing a map of 10m wide roads for a world atlas

T.Sakurai

Complexity vs. Productivity

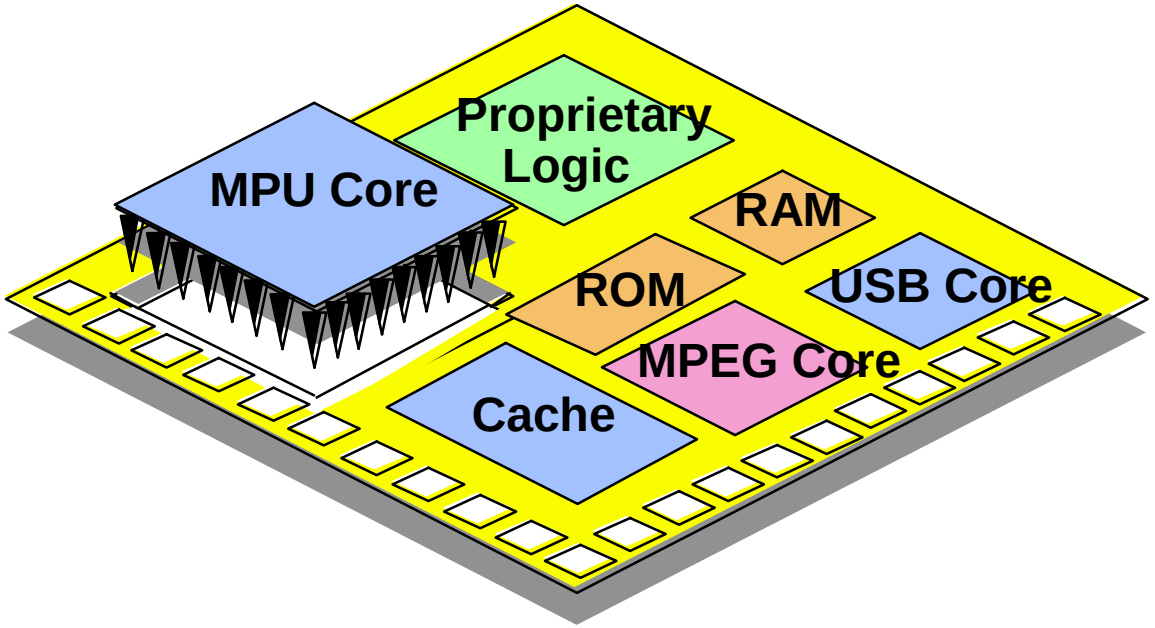


- System LSI design complexity increases faster than productivity. (http://notes.sematech.org/97melec.htm)

Overcome complexity crisis

- Re-use and sharing of design
- Design in higher abstraction

IP (A inc.)
IP (B univ.)
IP (C inst.)
IP (D semi.)

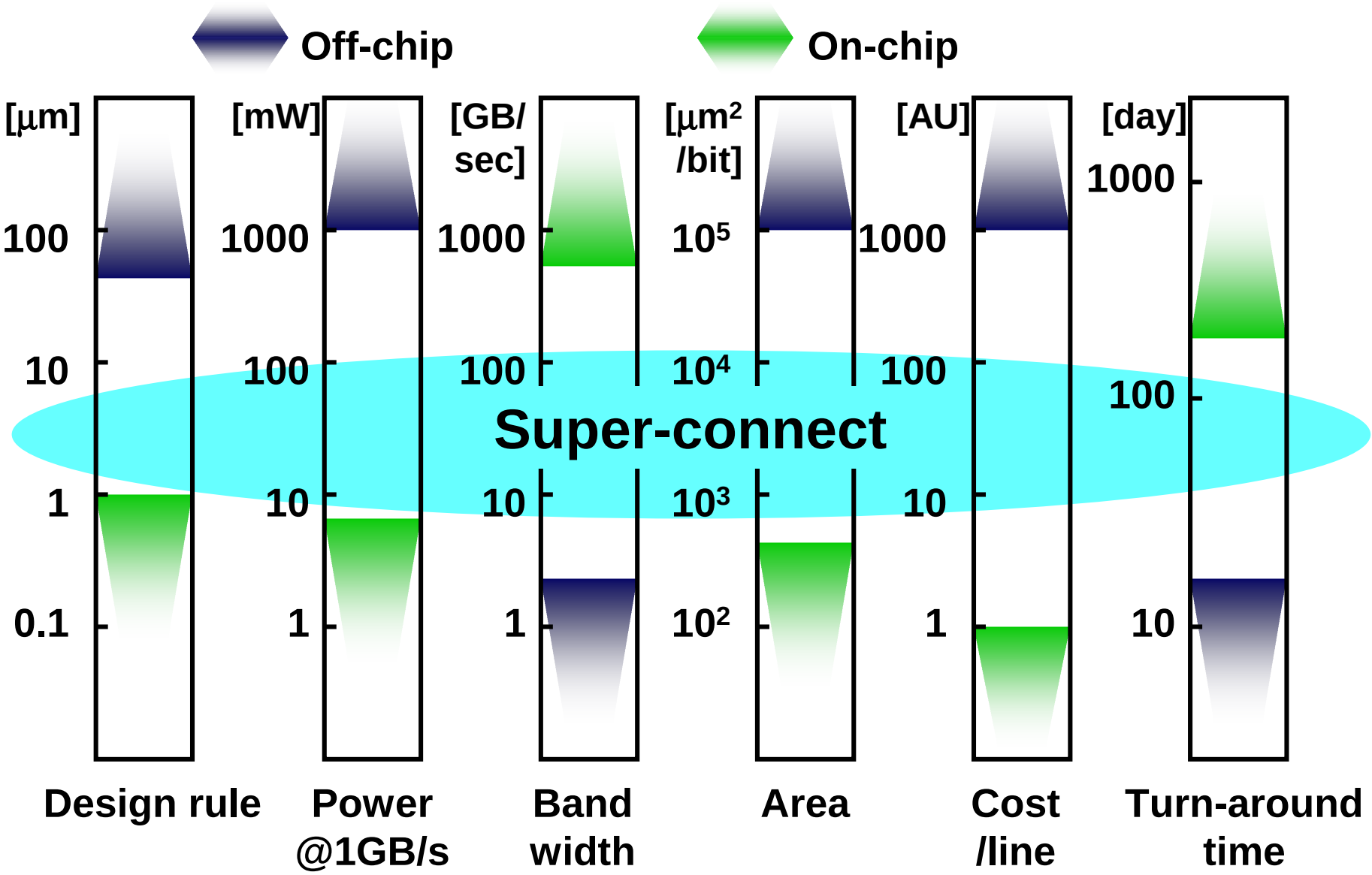


IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

Issues in System-on-Chip

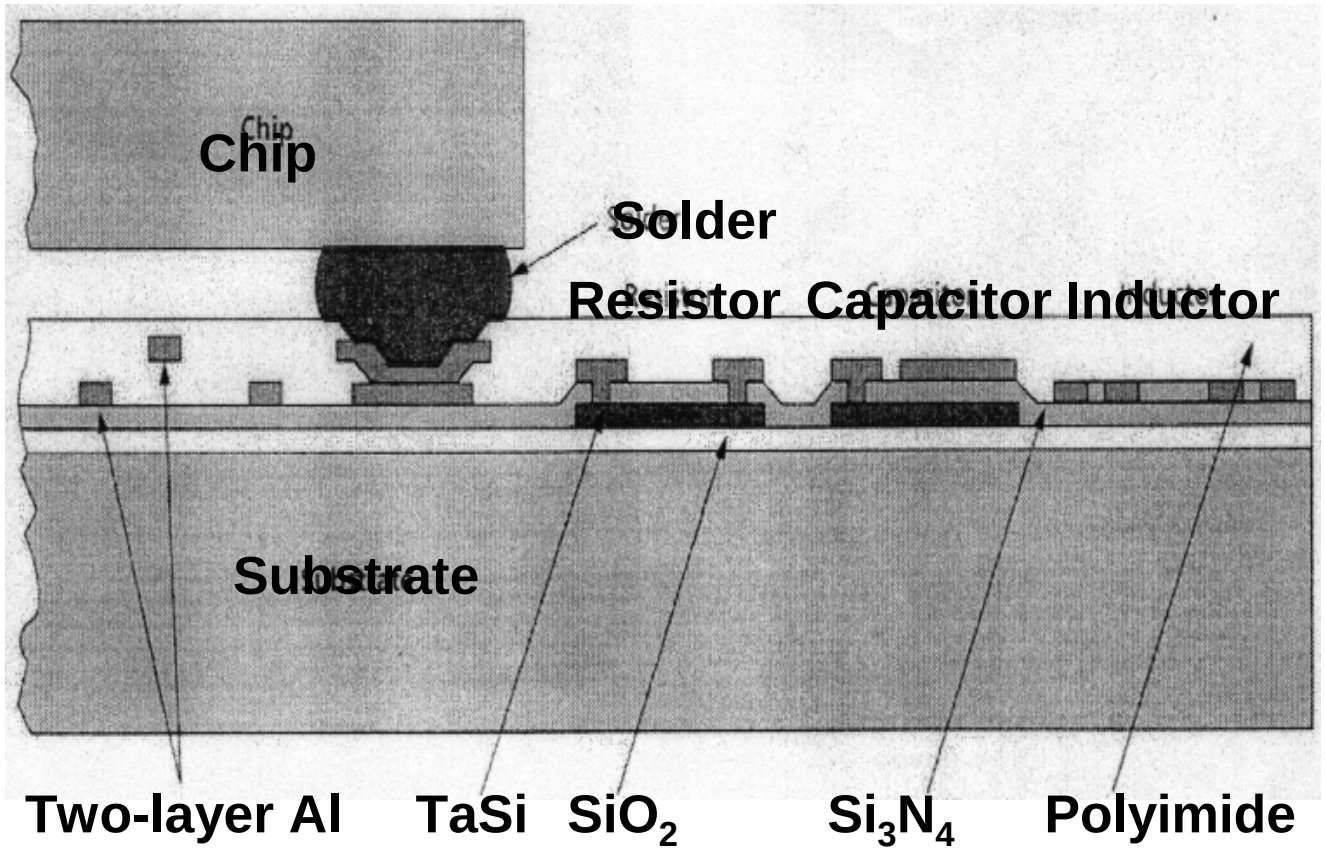
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

Super-connect



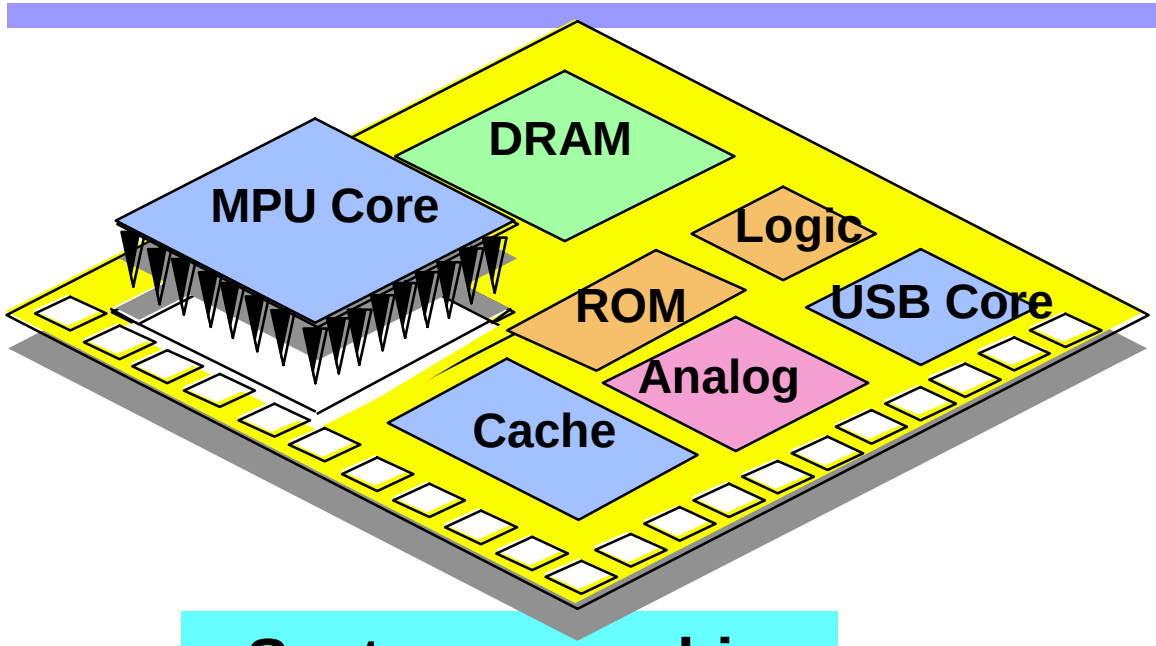
T.Sakurai

System-in-Package (SIP)

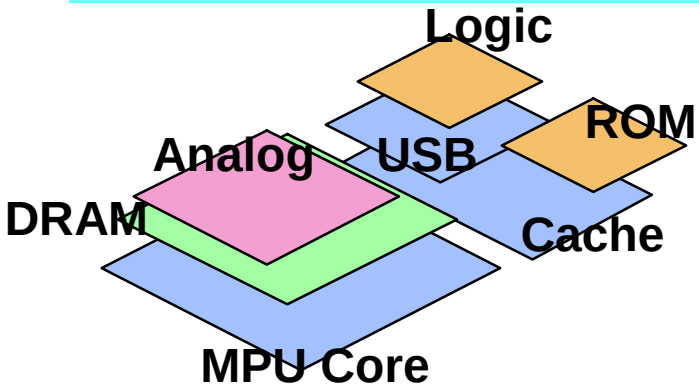


K.L.Tai, "System-In-Package (SIP): Challenges and Opportunities," ASPDAC, pp.191-196, Jan. 2000

3-Dimensional assembly



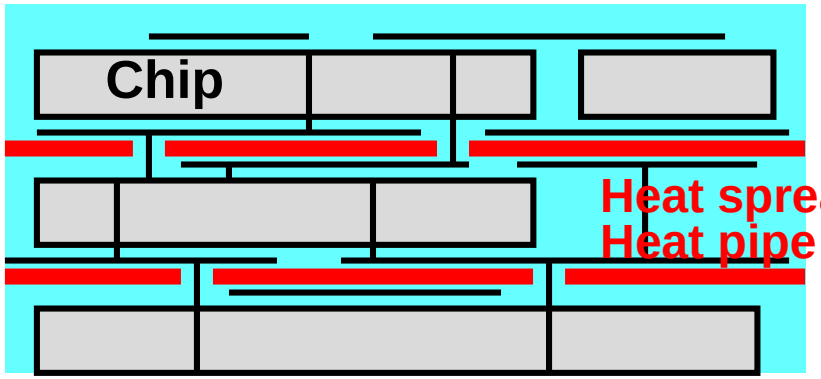
System on a chip



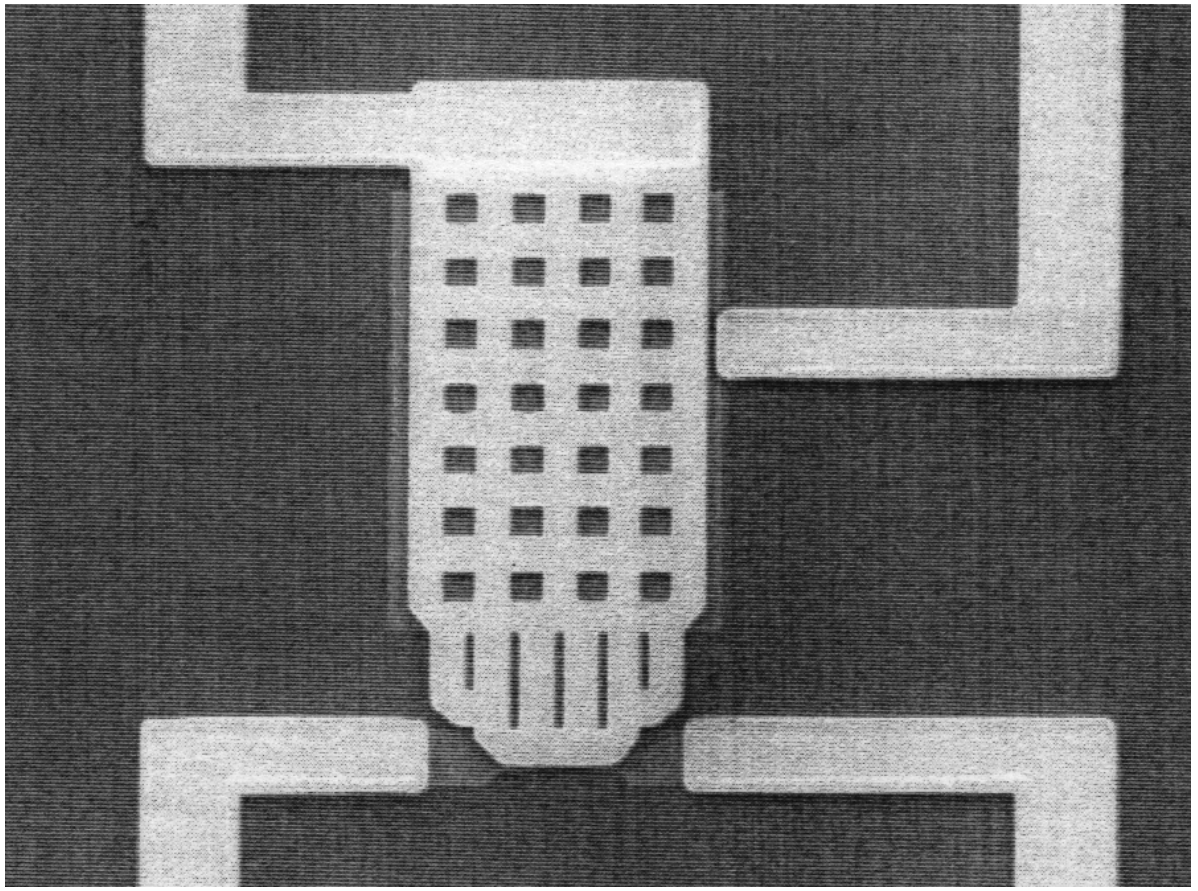
3-D assembly

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

- Heat dissipation is an issue

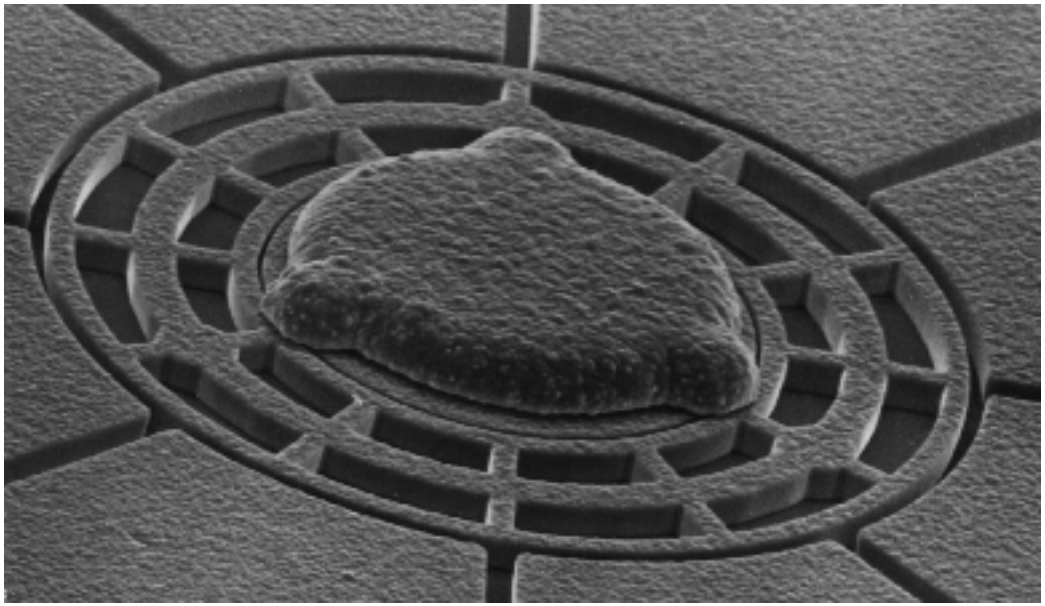


Micro-machined mechanical switch



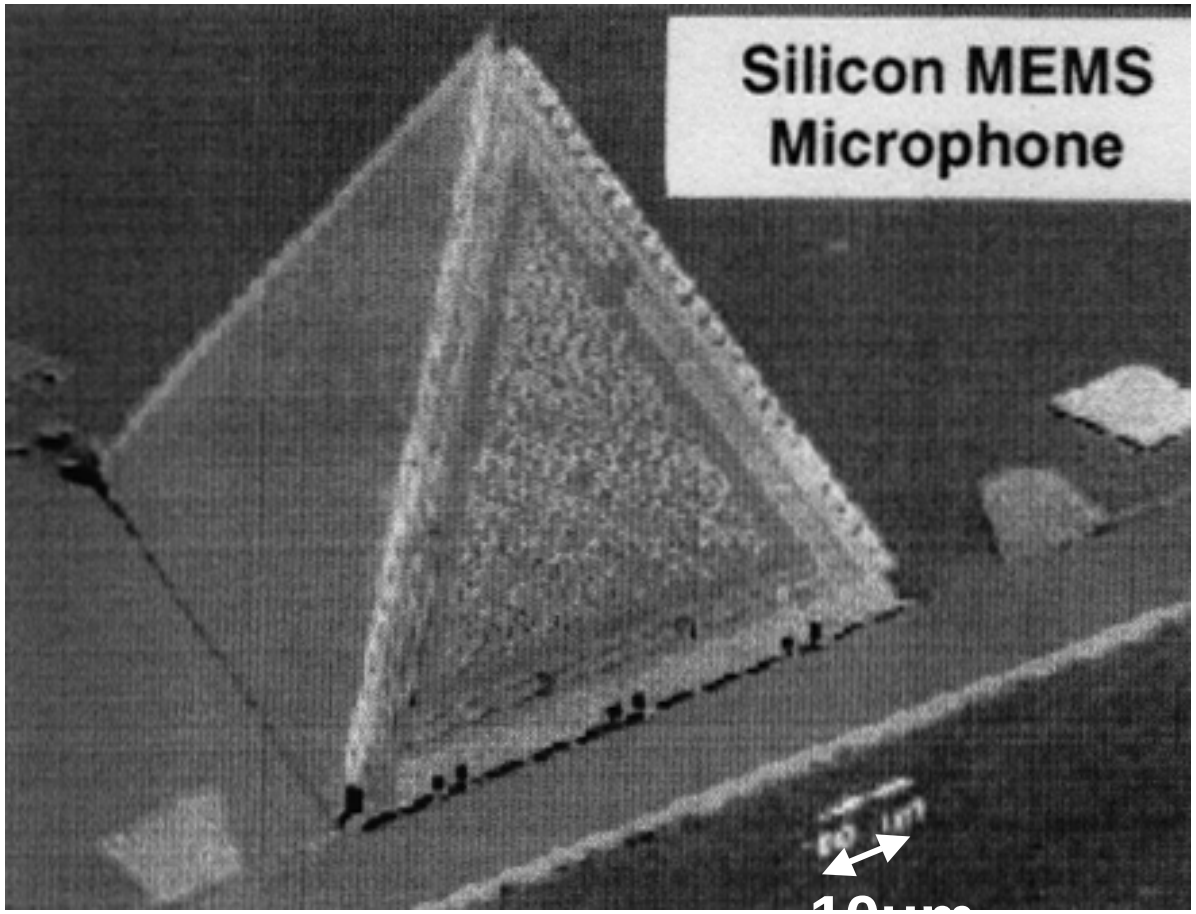
G.Weinberger, “The New Millennium: Wireless Technologies for a Truly Mobile Society,” ISSCC, pp.20-24, Feb. 2000.

Silicon MEMS motor



マイクロマシン技術で作った0.1ミリのモーター
東京大学、生産技術研究所、藤田博之教授提供

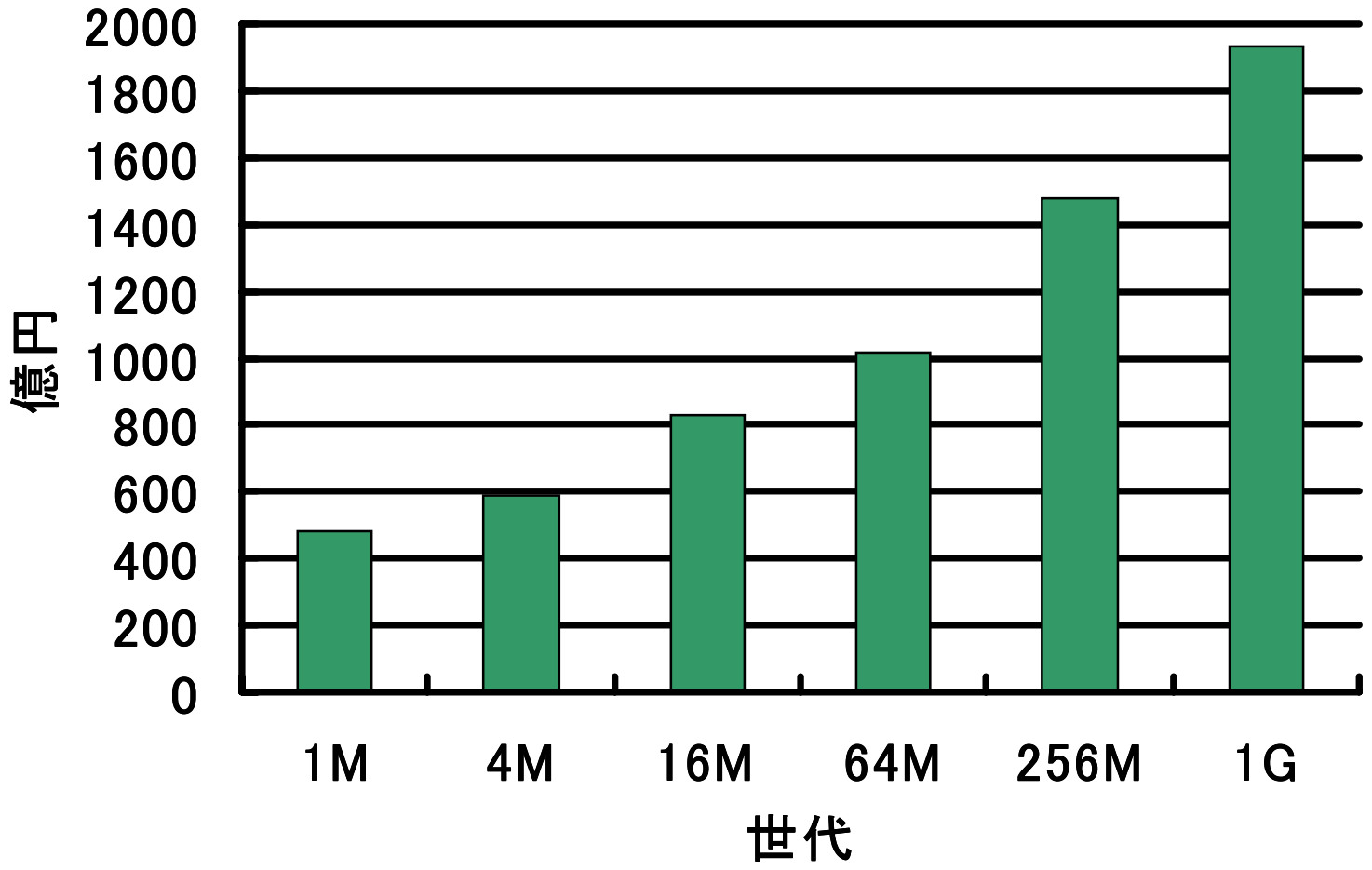
Silicon MEMS microphone



Will soon exceed the performance of the best commercial microphones, yet be inexpensive and potentially integrated with on-chip electronics.

M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

DRAM製造設備投資



資料：半導体産業研究所

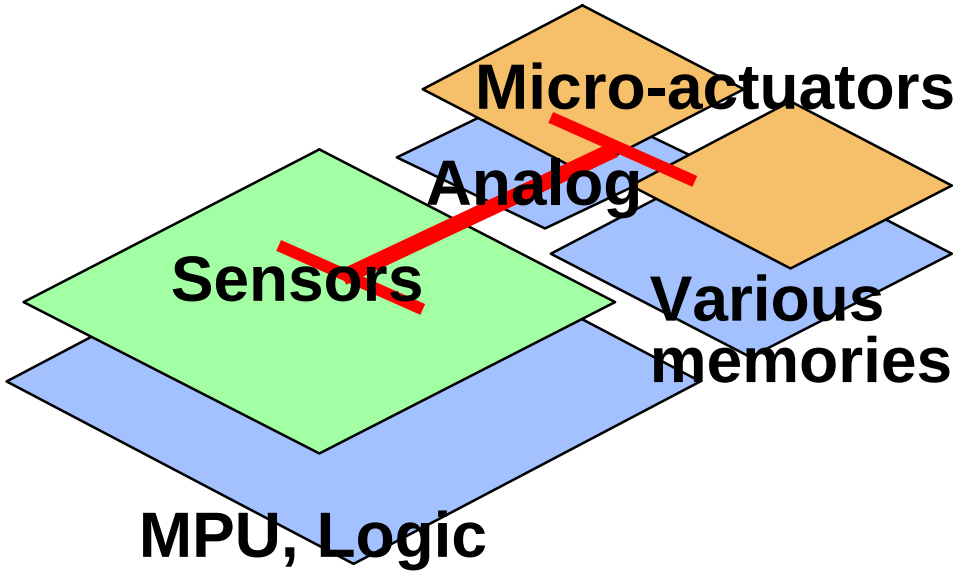
LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	μm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (μP)		21M	3.6G	170
DRAM capacity		1G	1T	256
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	μcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA) , International Technology Roadmap for Semiconductors: 1999 edition. Austin, TX:International SEMATECH, 1999.

T.Sakurai

Possible electronic system in 2014

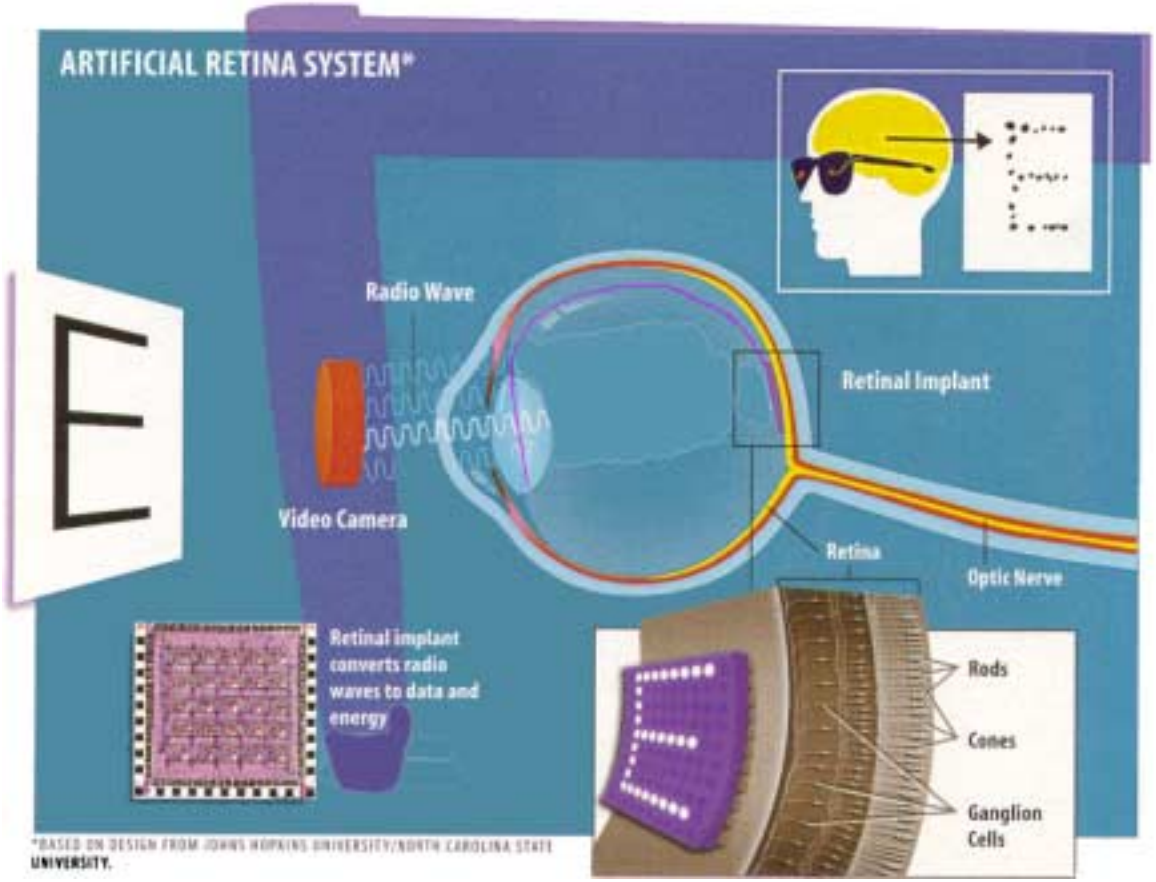


- Sensors/actutors
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)

Prosthesis - Dual Intraocular Units

NC STATE UNIVERSITY

Retinal Prosthesis

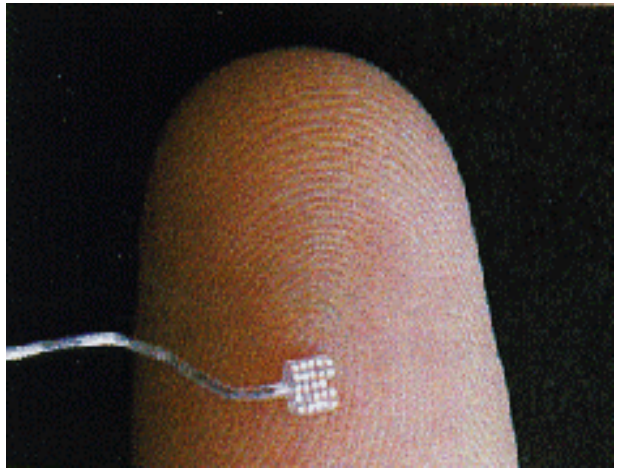


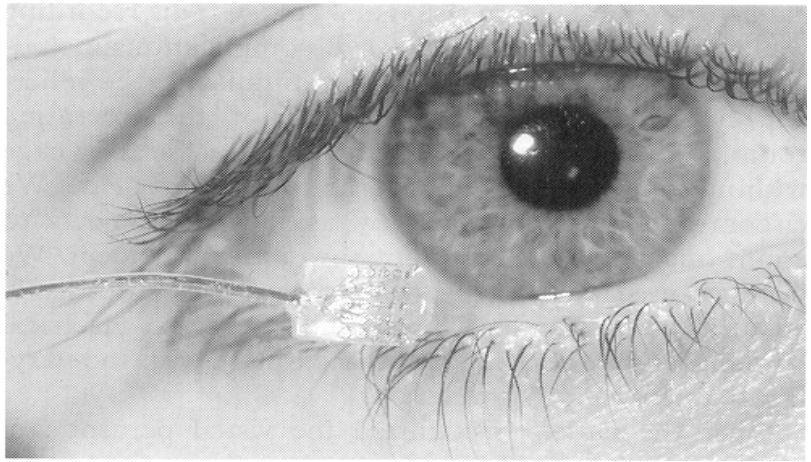
Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Electrodes Array

NC STATE UNIVERSITY

- Bio-Compatible - not toxic to neurons
- Large amount of current without causing irreversible electrochemical reactions
  - 400 uC/cm^2 for Platinum and 3 mC/ cm^2 for Iridium
- Not dissolve as a result of simulation
- Two metal meet the above demands - Platinum and Iridium
- Substrate for array - Silicone, Silicon, Polyimide, etc



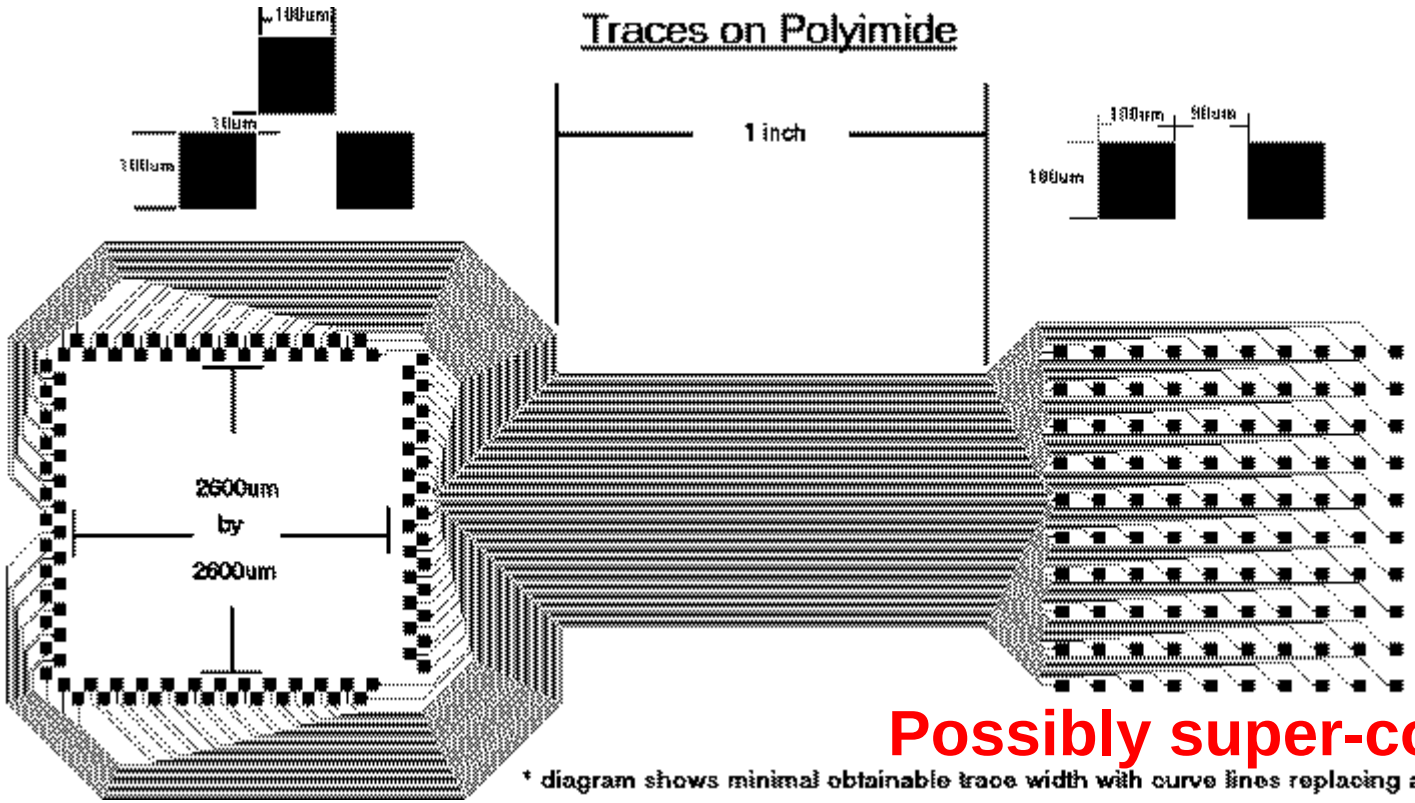


Platinum (5x5) on Silicone by Janusz

Retinal Prosthesis

Chip + Electrode Array on Polyimide

NC STATE UNIVERSITY



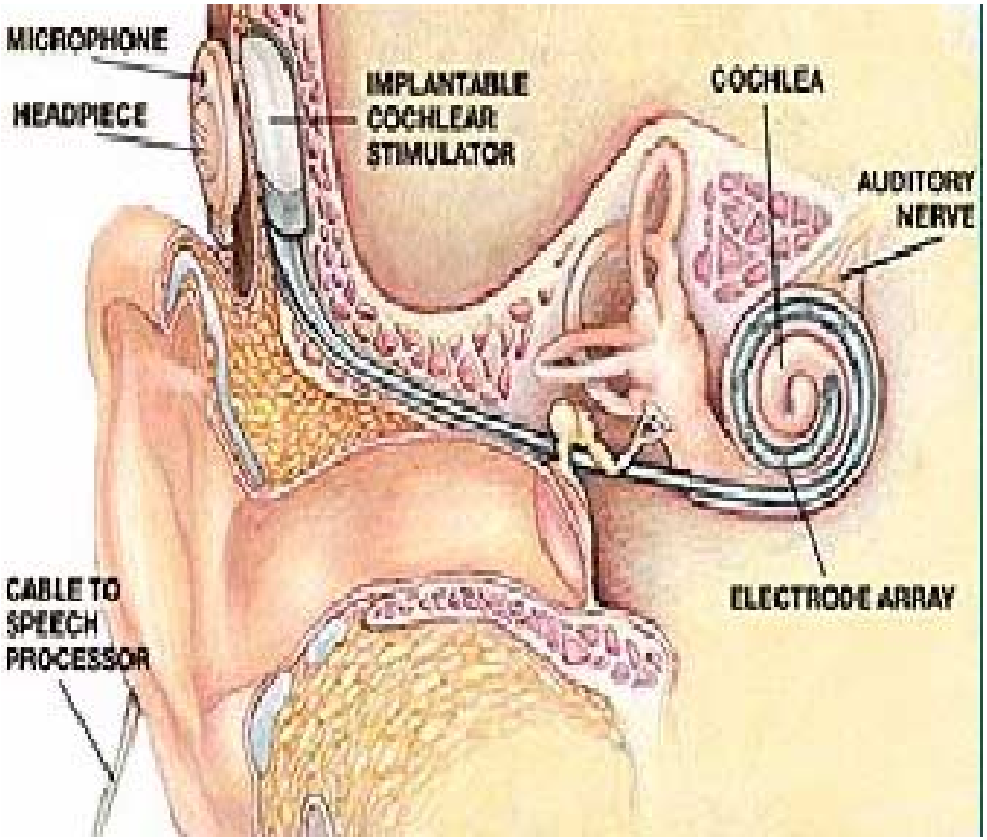
Possibly super-connect

Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Cochlear Implants

NC STATE UNIVERSITY

- 22 Electrodes
- Spatially Attached at Cochlear (low pitch sound at the apex)
- Power and Signals by Carrier Radio Frequency



Retinal Prosthesis