LSI の複雑化動向

Complexity issues in LSI's

桜井 貴康

Takayasu Sakurai

東京大学、国際・産学共同研究センター

Center for Collaborative Research, University of Tokyo

今後のシステム LSI は技術的には高集積化・微細化と混載化がその基礎となっている。従って、今後のシステム LSI 設計技術を整備するためには、高集積化・微細化と混載化に対しての対策を考えておく必要がある。高集積化・微細化あるいは混載化がはらむ設計上の問題点については半導体ロードマップとスケール則から、以下の問題が今後顕在化することが予測される。

1) 配線の問題

今後、配線が多層化、微細化され比較的多量な配線が LSI 中に存在することになるので、配線がコスト、信頼性、速度、消費電力を決める時代になる。トランジスタから配線へのパラダイムシフトである。特に、以下のような諸問題が新しい DSM (Deep Sub-Micron)配線系の問題として持ち上がってきている。すなわち、配線遅延の増大、配線間カップリングの増大によるシグナルインテグリティの低下、インダクタンスによるシグナルインテグリティの低下、信頼性の低下、IR ドロップの増大、EMI の増大などである。

2) 設計・テストにおける複雑さの問題

基本的に一世代で約 4 倍づつ増大する 1 チップ上のトランジスタ数に対し、設計、テストの生産性が追いつかないことから生ずるのが、複雑さの問題である。１億素子が搭載されたチップを１回のシリコン・ランで完全動作まで持ち込めるのか。この問題の解決には、設計資産の再利用・共有、大きな機能ブロックレベルで設計するいわゆる抽象度の高いレベルで設計すること、スーパーコネクトの利用などによるテスト済ハードウェアの mix and match 技術などが必須となる。テストも複雑になる。Built-In-Self-Test が現在よりも多用されることとなることが予想される。

3) 設計･製造のインタラクションの問題

DSM 設計では設計と製造のインタラクションが増大する。水平分業的な産業構造への変革が必要であることは当然としても、ソフトウェア、システム、回路、デバイス、アセンブリなどが有機的に結合した所に新しいソリューションが存在するようになる。すべての分野に関する経験および知見の蓄積があることを差別化要因ととらえ、このインタラクションの増大をチャンスととらえて設計インフラを構築できれば、大きな差別化になることが期待される。混載化などもこのような有機的な結合が生きる例である。

微細化された素子では、ゲート長、あるいはしきい値電圧など製造バラツキが比較的増大する。また、扱う素子数の増加もバラツキの問題を増大させる場合がある。動作マージンの低下などが深刻化する。低電圧化などもアナログなどの回路ブロックで製造バラツキの影響を出やすくさせる。Quality of design という言葉が使われるようになってきているが、バラツキのある環境下で如何に歩留まりの高い設計をするかが重要な観点となってくる。最近では、バラツキ問題の対策として製造後にパラメータを微調して回路性能を向上するといった観点でのアイデアも出てきている。

4) 消費電力の問題

スケール則の当然の帰結として、今後、消費電力は増大する。この問題は根深い。また、急ピッチで進行する IT 革命を下支えする、いつでもどこでも必要な情報を送受信できるモバイルな情報環境の実現には、集積回路の低消費電力化が必須である。また、消費電力の低減は環境問題、あるいは老齢化問題を解決するキーテクノロジーでもあり、重要性は高い。消費電力を押さえる技術はいくつか出てきている。多しきい値、可変しきい値、多電源、可変電源などがある。特に、回路とデバイス、ハードウェアとソフトウェアの協調による解決など分野を越えた協調に、大きな成果が現れてきた。

5) その他の複雑系設計の課題

設計環境を構築するときにリコンフィギュラブルなデバイスも考慮に入れる必要がある。また、当然のことな

がら、設計の効率化にインターネットの積極的利用を考慮すべきであろう。

Abstract（これは講演申込書に貼ってください）

今後のシステム LSI 設計技術を整備するためには、高集積化・微細化と混載化に対しての対策を考えておく必要がある。本講演では特に、配線の問題、設計・テストにおける複雑さの問題、設計･製造のインタラクションの問題、消費電力の問題の４つの問題について解説する。

電子情報通信学会ソサイエティ大会　’00/10

SoCの回路／フィジカル設計技術の研究開発動向と課題

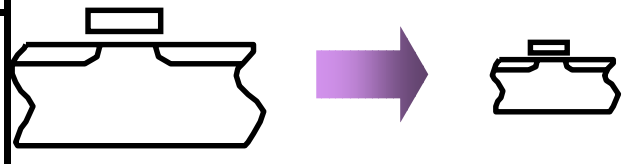
LSIの複雑化動向

Prof. Takayasu Sakurai
Center for Collaborative Research, and
Institute of Industrial Science,
University of Tokyo
E-mail:tsakurai@iis.u-tokyo.ac.jp

1　配線の問題
2　設計・テストにおける複雑さの問題
3　設計･製造のインタラクションの問題
4　消費電力の問題

Scaling Law

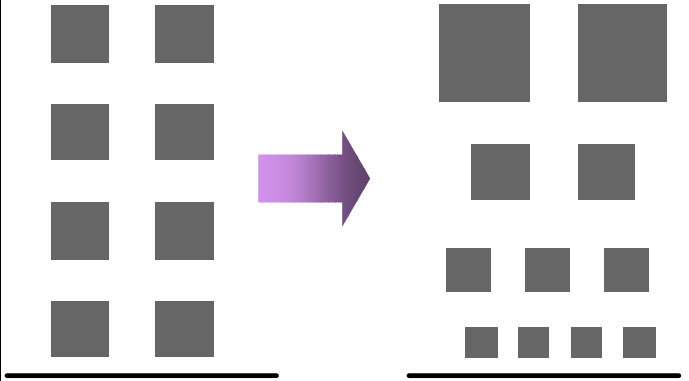
Transistors		Numbers are exponent to k	
Vdd	[V]	-1	
Tr. dimensions	[x]	-1	
Tr. current	[I~1/x x/x V^1.3]	-0.3	
Tr. capacitance	[C~1/x xx]	-1	
Tr. delay	[d~CV/I]	-1.7	
Tr. power	[P~VI~CVV/d]	-1.3	
Power density	**[p~P/x/x]**	**0.7**	
Tr. density	**[n~1/x/x]**	**2**	
Interconnections			
Type		**Local**	**Global**
Scaling scenario		**Scaled**	**Anti-scaled**
Line thickness	[T]	-1	1
Width	[W]	-1	1
Separation	[S]	-1	1
Oxide thickness	[H]	-1	0
Length	[L]	-1	0
Resistance	[Rint~L/W/T]	1	-2
Capacitance	[Cint~LW/H]	-1	1
RC delay/Tr. delay	**[D~RintCint/d]**	**1.7**	**–**
Current density	**[J~pWL/V /W/T]**	**–**	**0.7**
DC noise / Vdd	**[N~JWTR/V]**	**–**	**1.7**



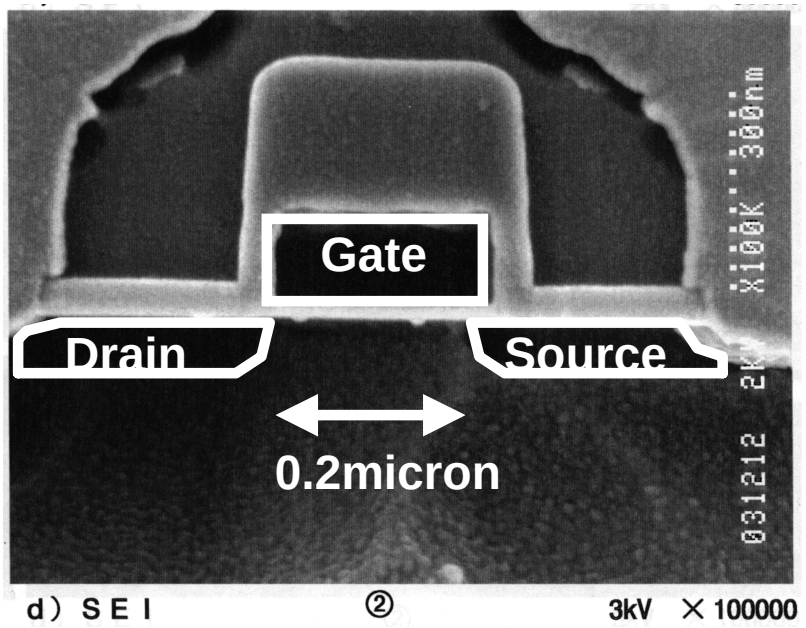
K=2

$$I_{DS} = \frac{\mu\varepsilon}{2t_{OX}} \frac{W}{L} (V_{GS} - V_{TH})^{\alpha} \approx [1/x\,x/x\,V^{1.3}]$$

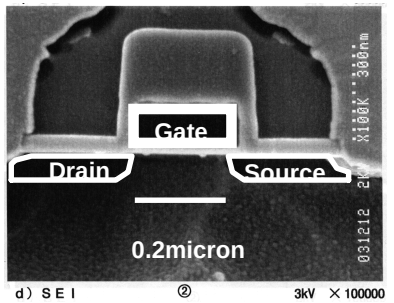
T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no,2, pp.584-594, Apr. 1990.



Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

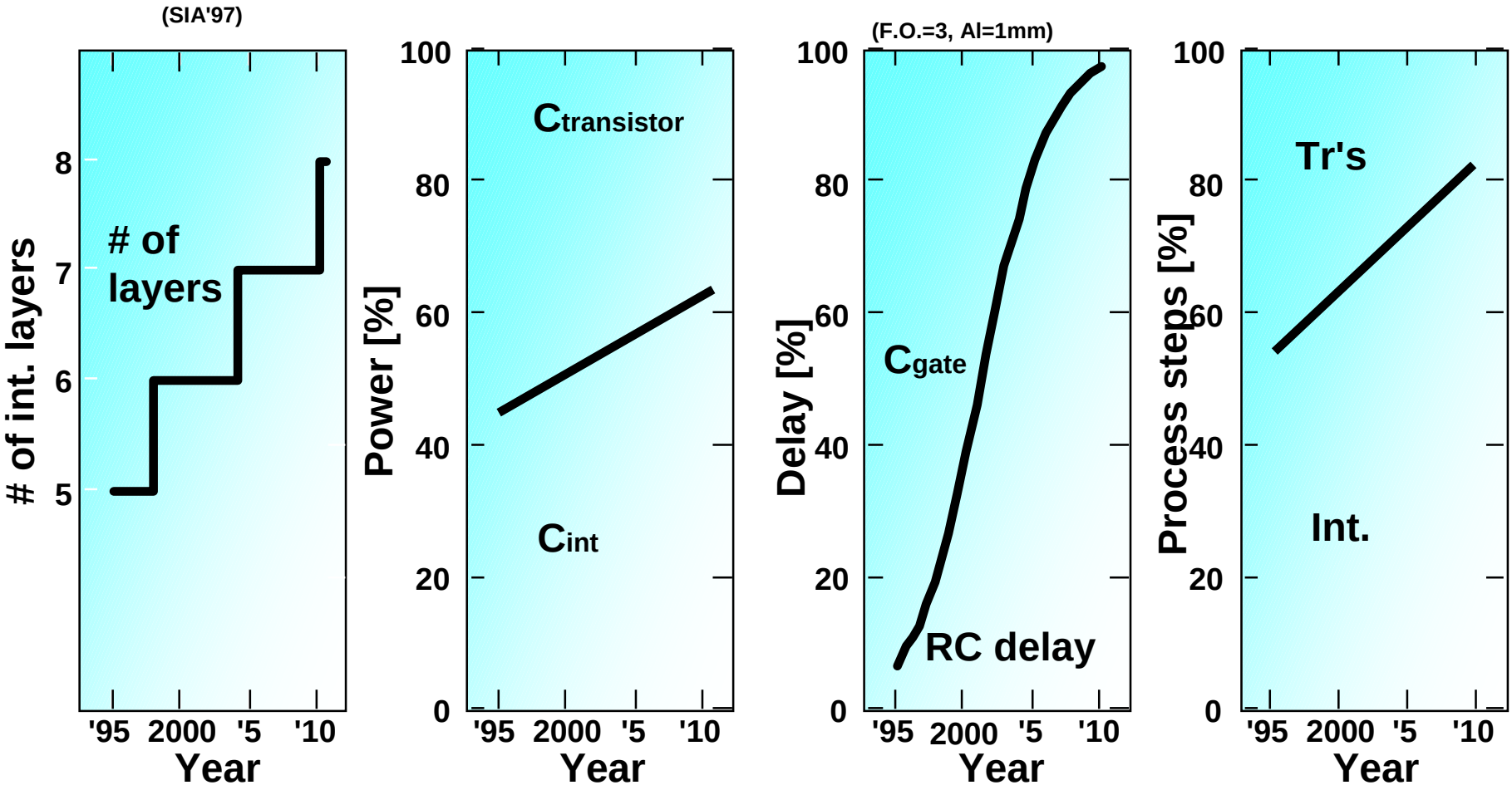
Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

T.Sakurai

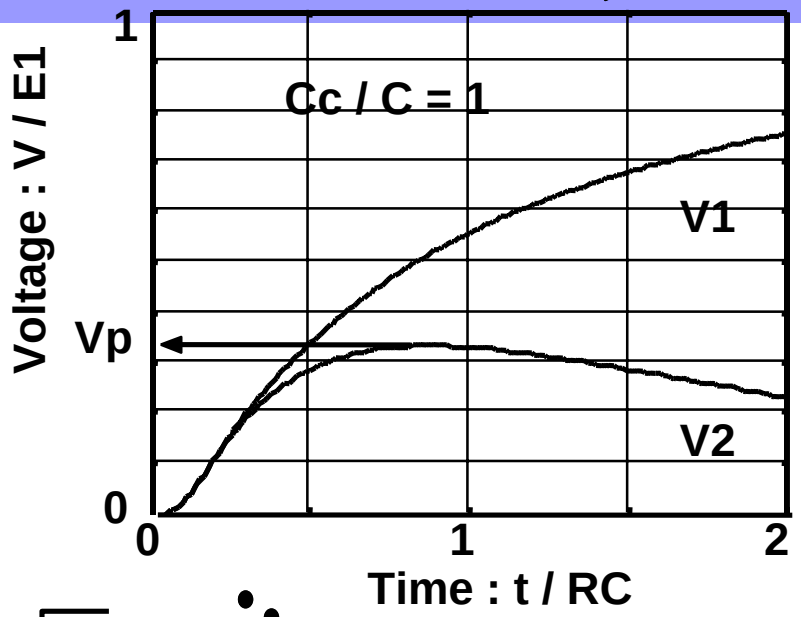
性能を配線が決める時代

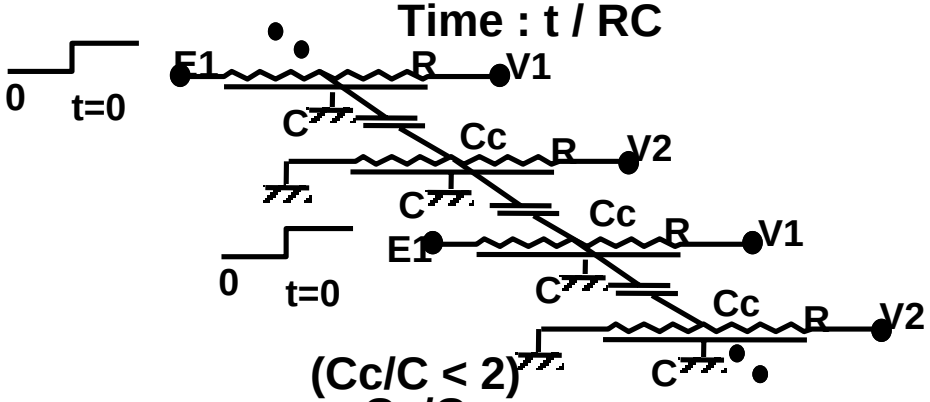
P: Power, D: Delay, A: Area, T:Turn-around



T.Sakurai

カップリングノイズ

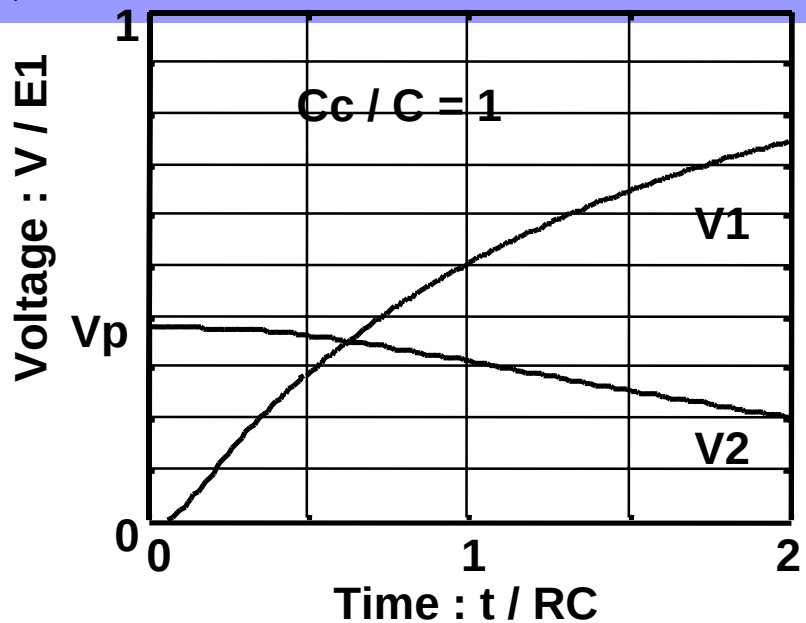


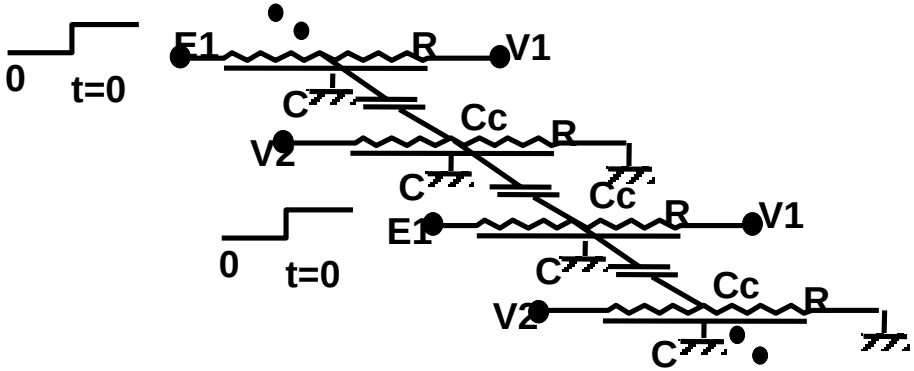


(Cc/C < 2)

$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$

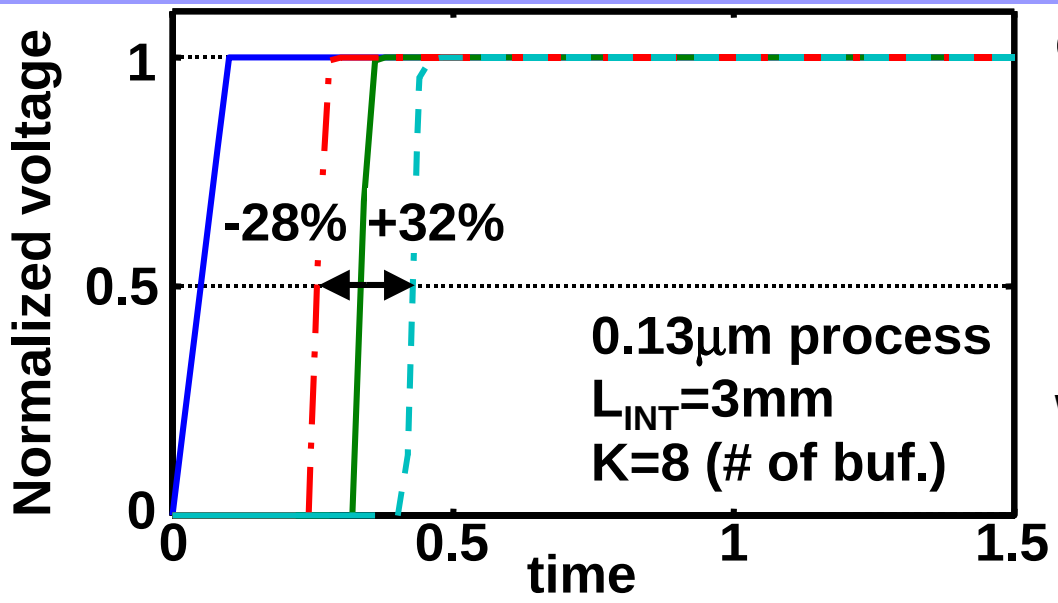


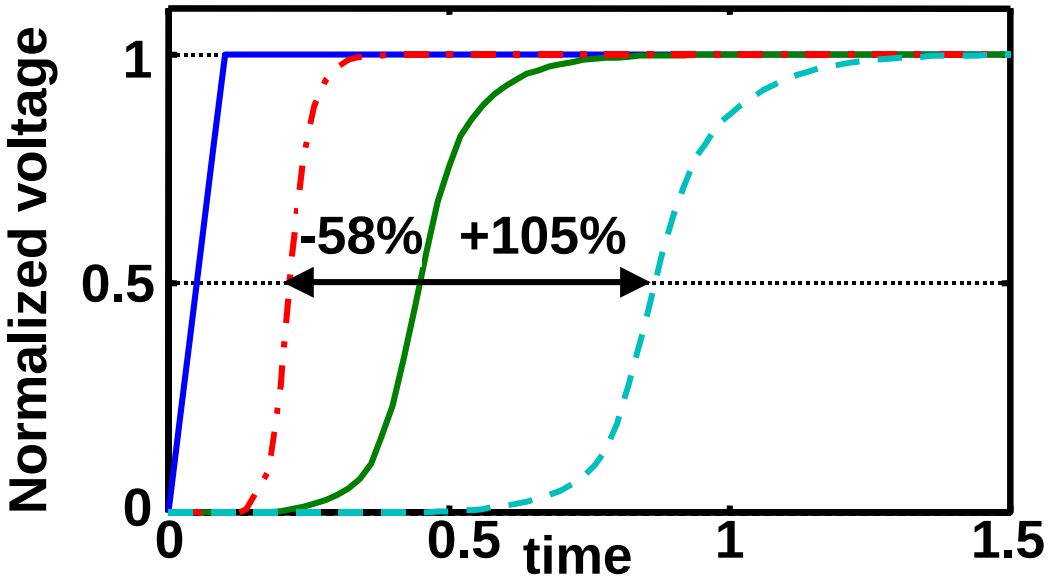


$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

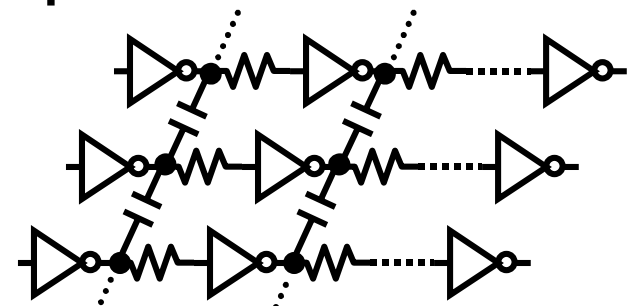
H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnections

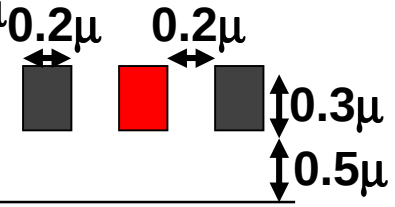


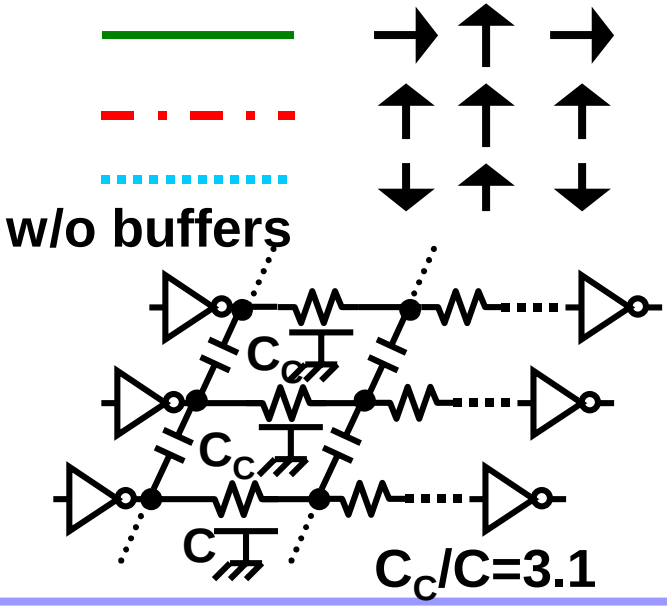


Optimized buffer insertion

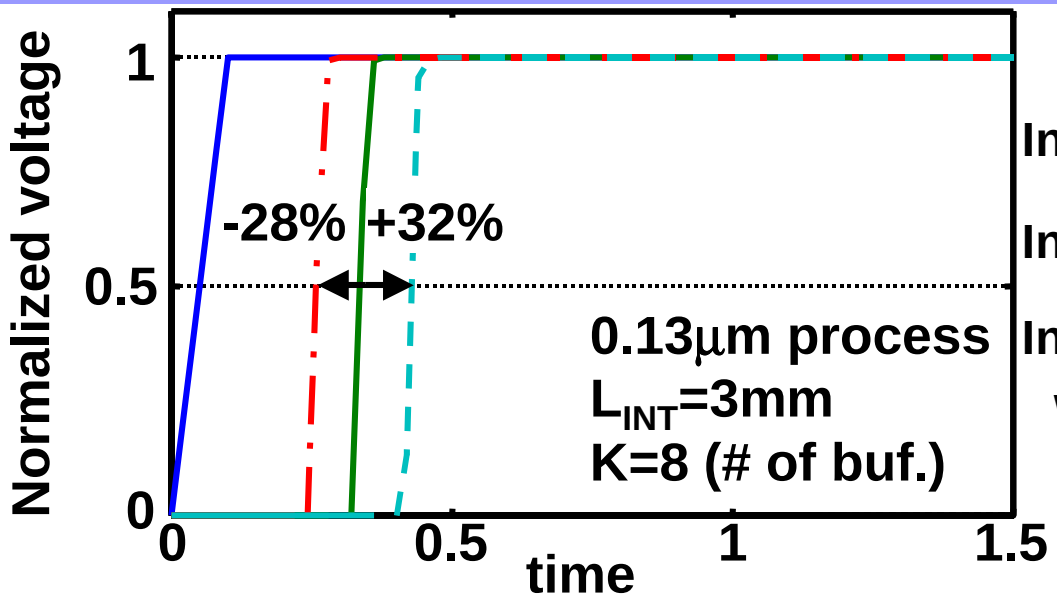


W_N/W_P=25μ/38μ

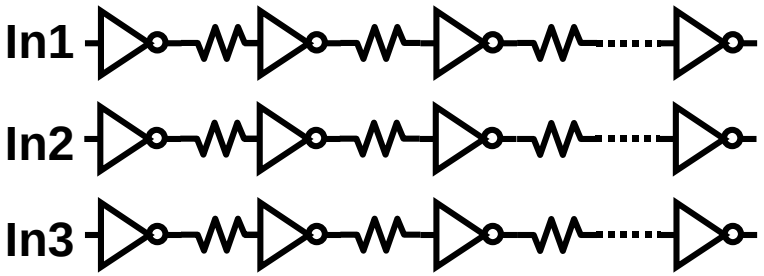




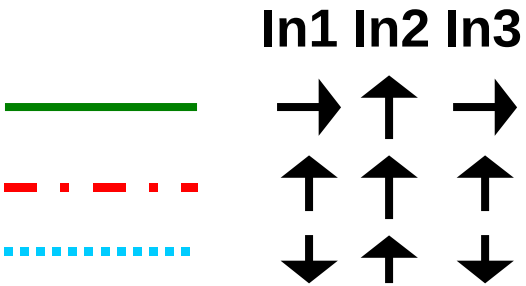
Coupling among Interconnections

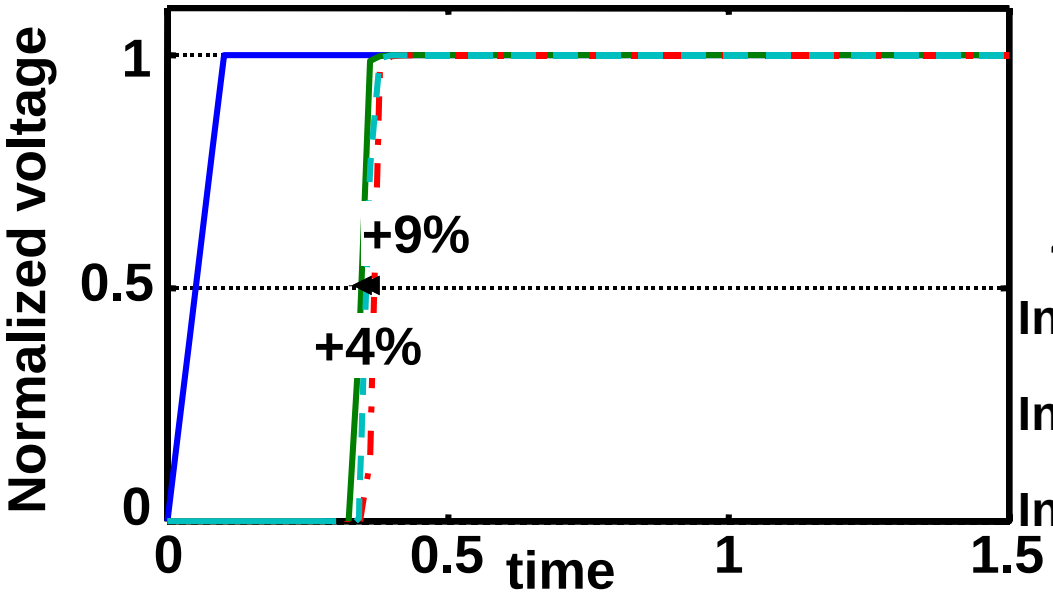


Normal buffer insertion

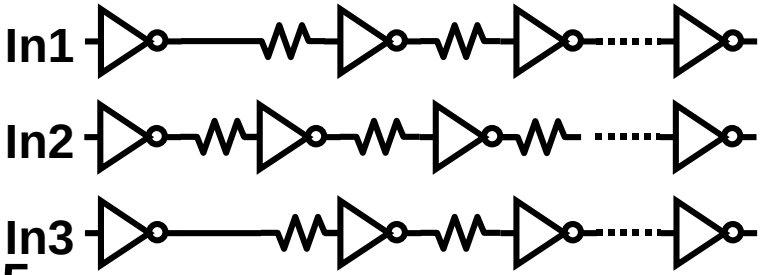


W_N/W_P=25μ/38μ

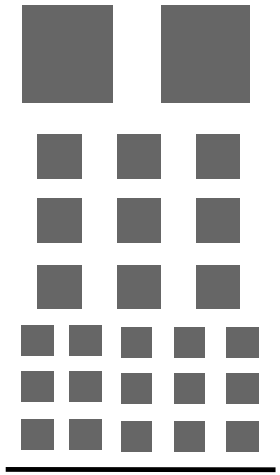


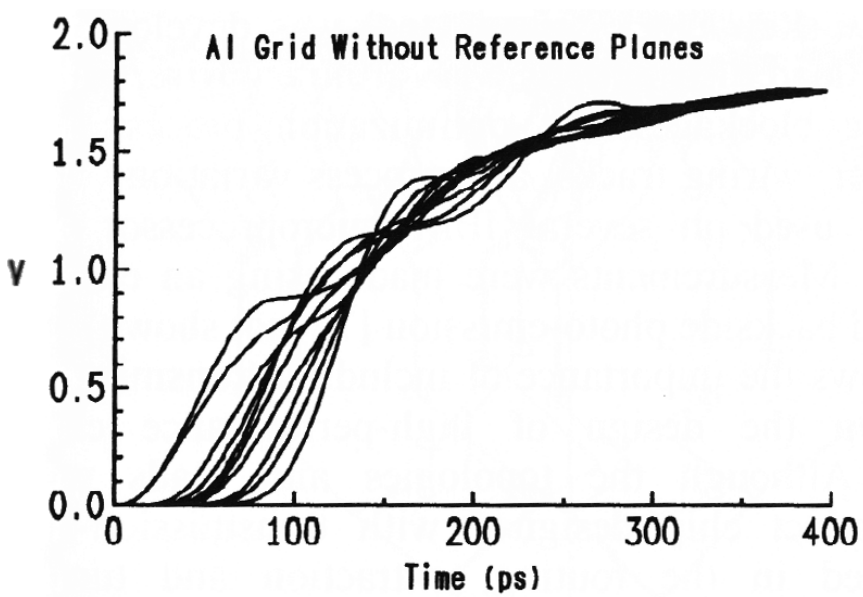


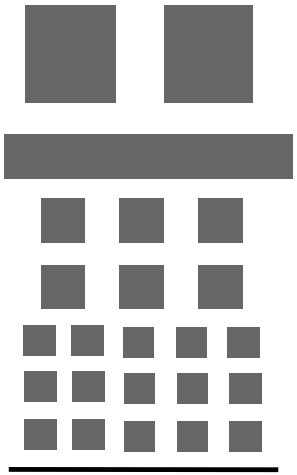
Zigzag buffer insertion

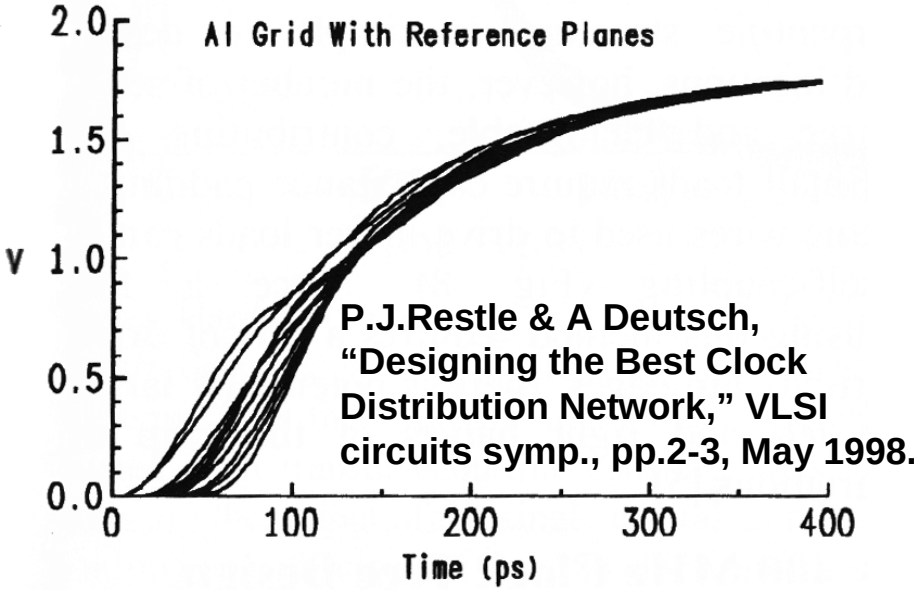


Inductive Effects in Clock Lines







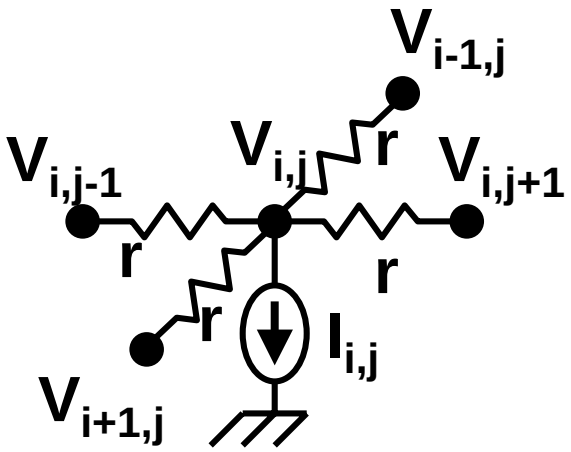


P.J.Restle & A Deutsch, "Designing the Best Clock Distribution Network," VLSI circuits symp., pp.2-3, May 1998.

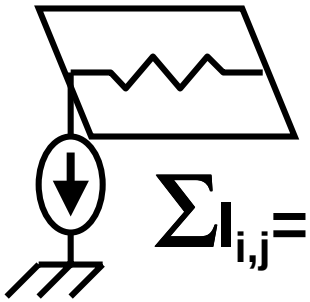
Board design practice is imported in LSI.

T.Sakurai

IR Drop

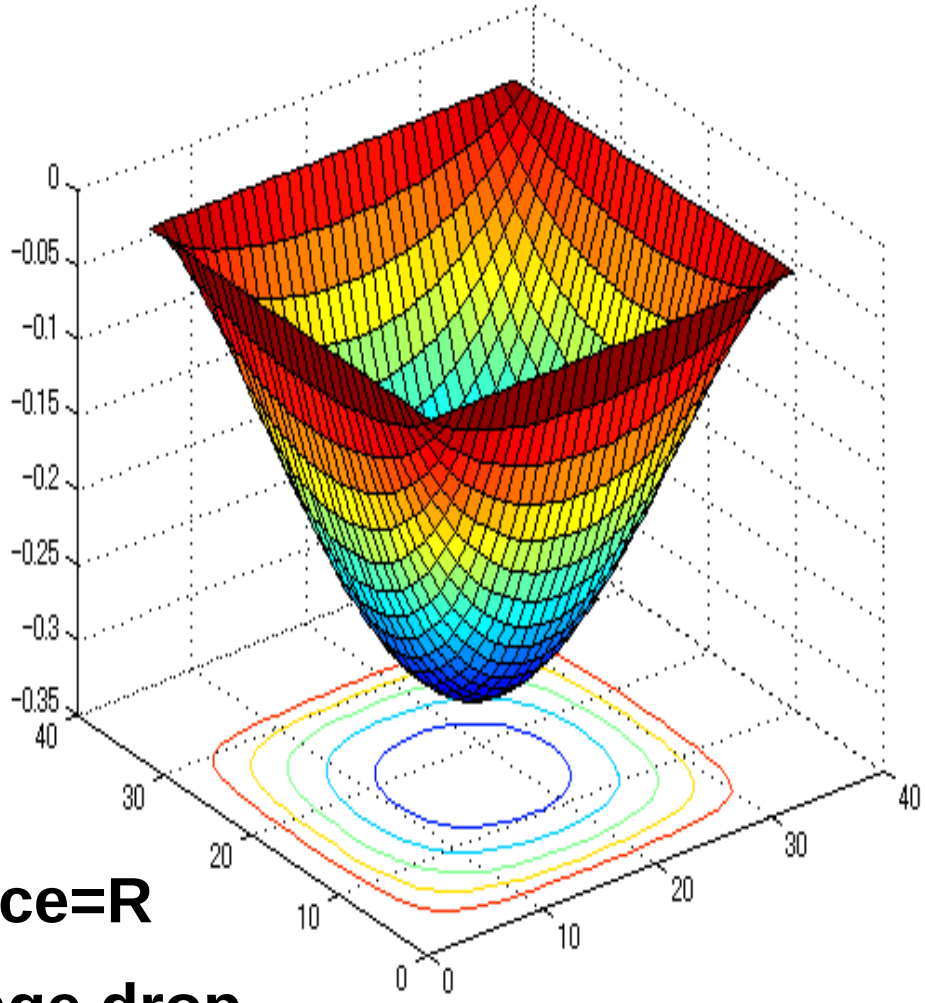


$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\,I_{i,j}$$



$\sum I_{i,j}=I$, Sheet resistance=R

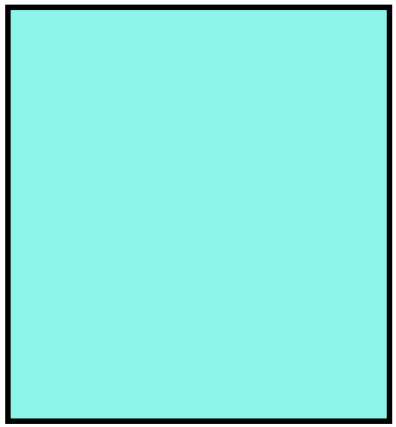
Take IR as unity voltage drop

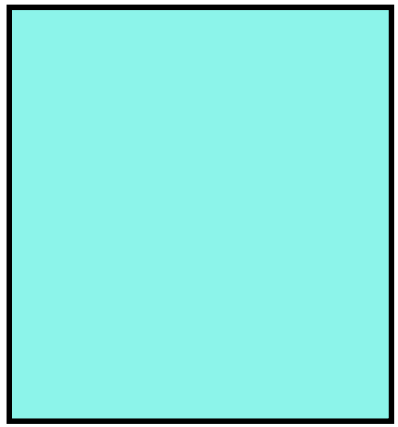


IRドロップ

Unscaled / anti-scaled

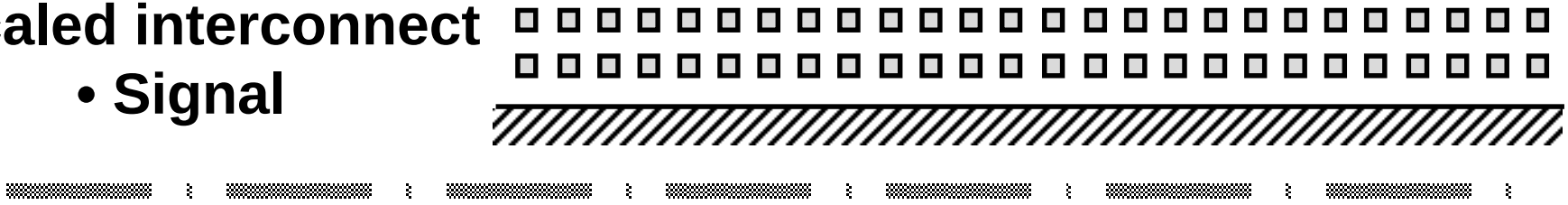
- **Clock**
- **Long bus**
- **Power supply**





Scaled interconnect

- **Signal**



1V 50W -> 50A current

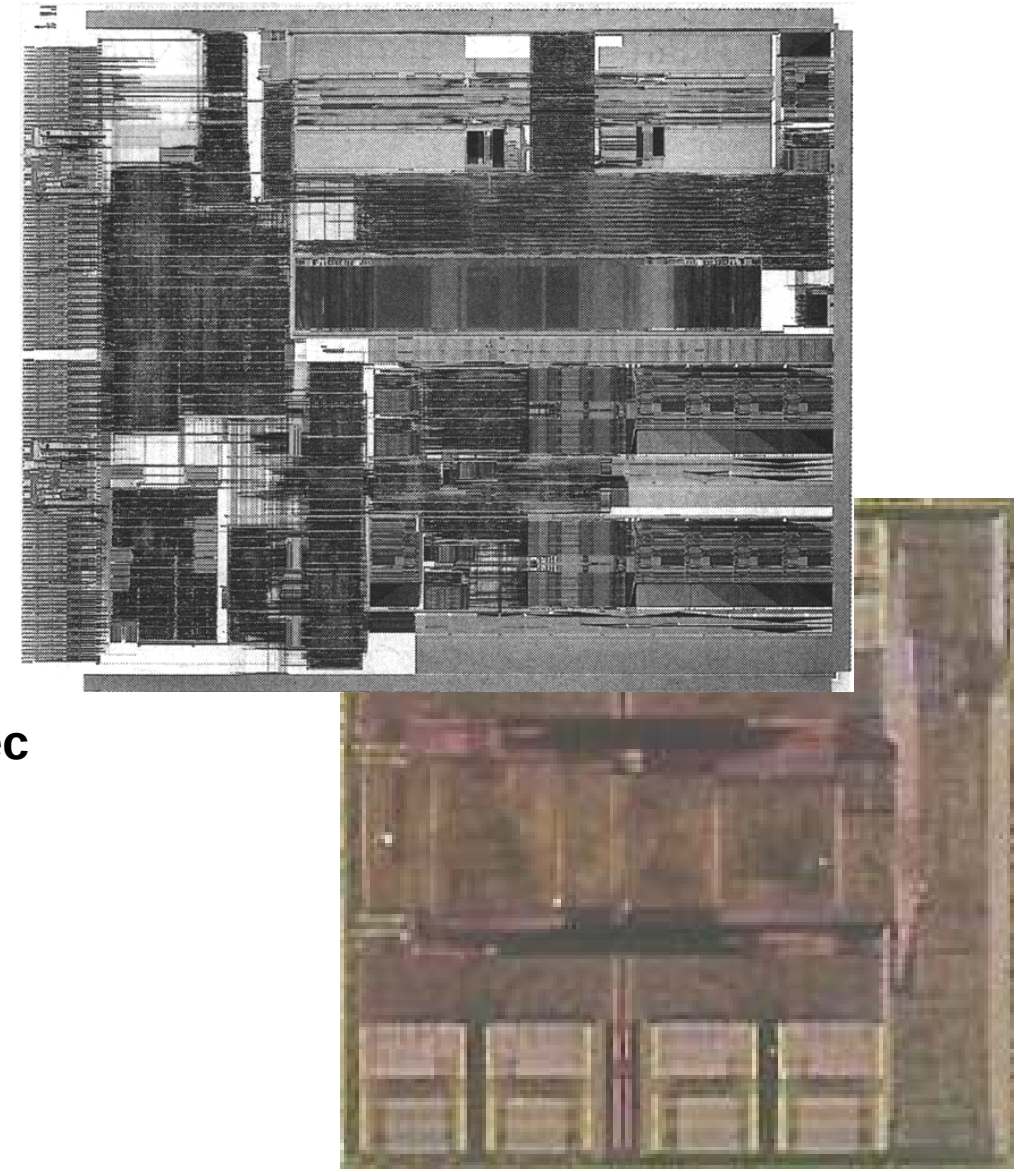
5% noise -> 0.05V noise -> 1mΩ sheet R -> 15μm thick Cu

Area pad + package, or thick layer on board is needed.

System LSI for Next Generation Games

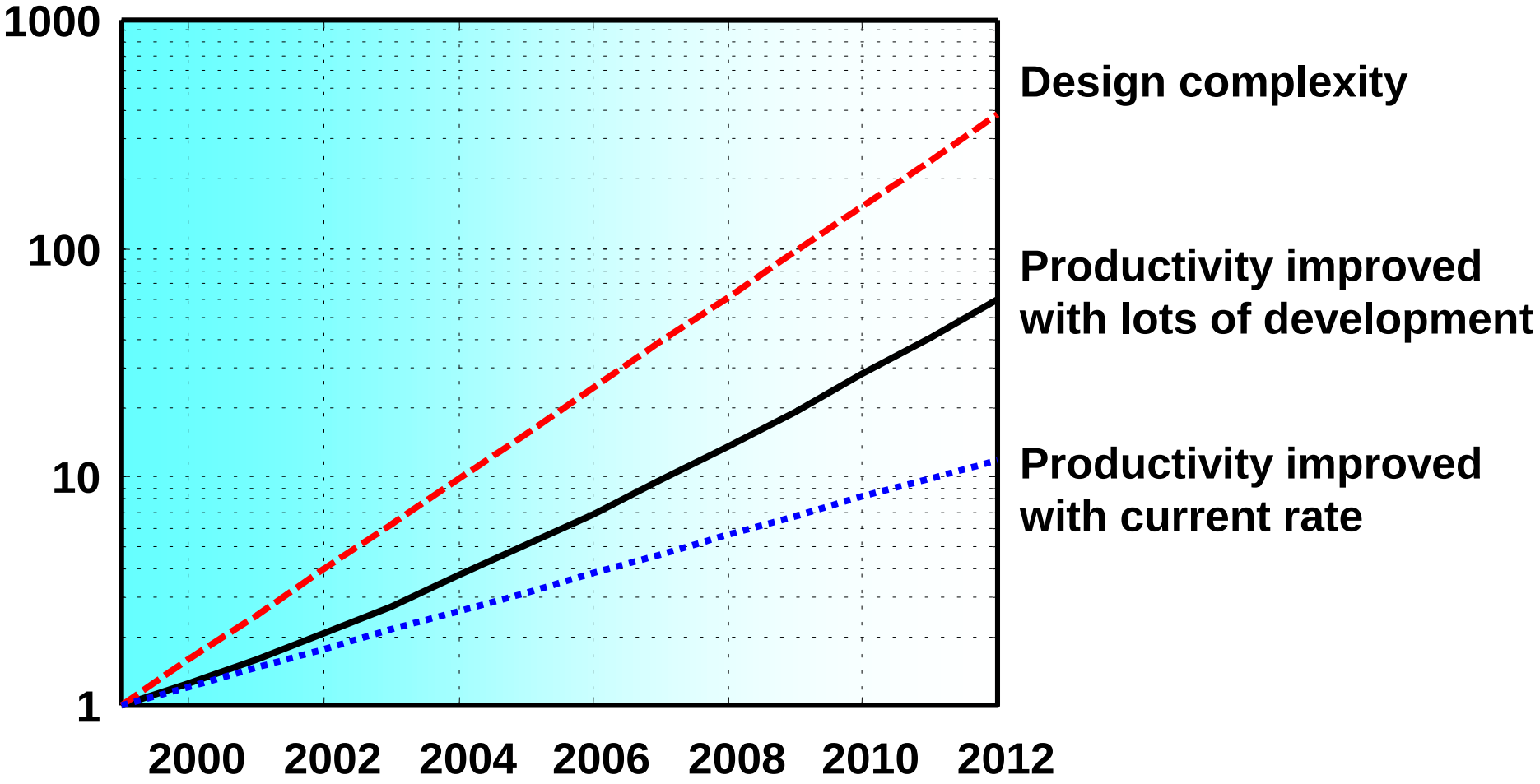
- Clock freq. 300MHz
- 10M transistors
- Graphics synthesizer integrate

  40M tr. With embedded DRAM
- Memory bandwidth 3.2GB/s
- Floating operation 6.2GFLOPS/sec
- 3D CG 6.6M polygon/sec
- MPEG2 decode



T.Sakurai

Complexity vs. Productivity

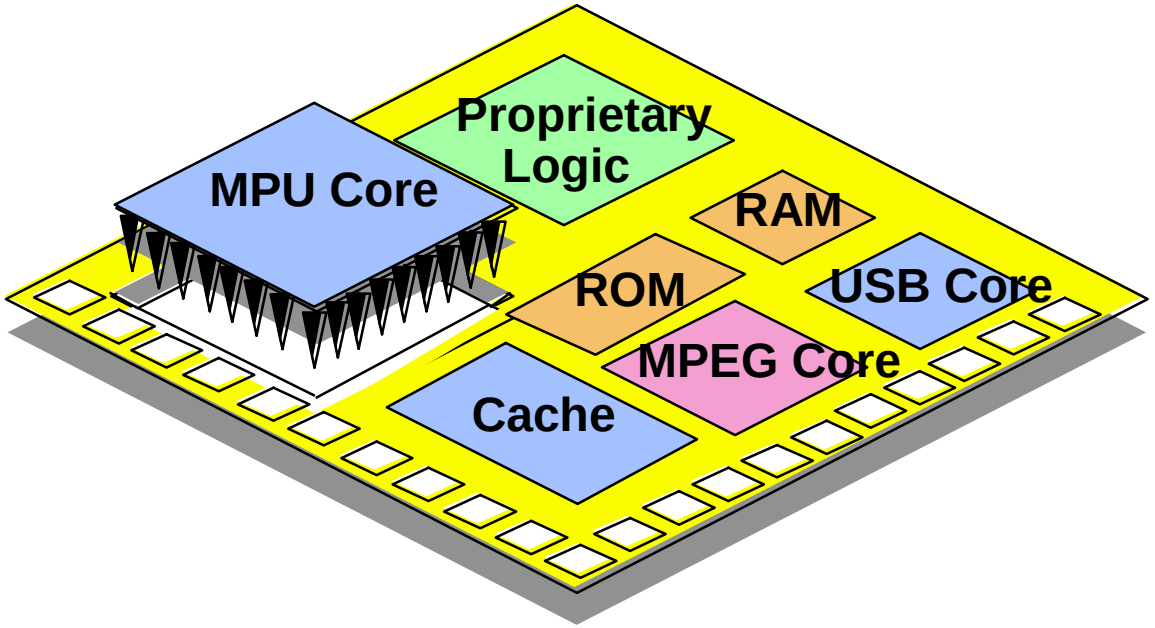


- System LSI design complexity increases faster than productivity. (http://notes.sematech.org/97melec.htm)

Overcome complexity crisis

- Re-use and sharing of design
- Design in higher abstraction

IP (A inc.)
IP (B univ.)
IP (C inst.)
IP (D semi.)



IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

System-in-Package

ELECTRONIC ENGINEERING
EE TIMES
eet.com The industry newspaper for engineers and technical management Monday November 8, 1999

Expanding role of packaging seen relegating SoC to niche status

System-chip may topple . . .

By Robert Ristelhueber

INDIAN WELLS, CALIF. – The wheels might be coming off the system-on-chip (SoC) bandwagon, if the chatter at last week's Dataquest Semiconductor conference is any barometer of industry sentiment. Heavyweights including IBM and Lucent Technologies indicated that costs may relegate SoC to niche status, with new packaging techniques stepping into the breach.

"A couple of years ago we really thought that the embedded DRAM model would be the panacea for many applications," said John Kelly, general manager of IBM Microelectronics. "It's not always the right thing. In many applications it still remains much cheaper to do it with multichip modules. It gives you satisfactory performance and often for lower cost."

"We have systems-on-chip now that are really 'system on chips,' " said John Dickson, president of Lucent Technologies' Microelectronics Group. "We do it that way because it's most cost-effective, and the customer will prefer it that way because it offers more flexibility."

The subject was broached at the conference here by a Dataquest analyst who claimed that SoC designs will increasingly be supplanted in coming years by multichip packaging as higher mask costs squeeze SoC profitability.

Chip designers have often been willing to add mask steps

▸CONTINUED ON PAGE 6

IBM's Kelly: 'In many apps, cheaper to do it with multichip modules.'

. . . as industry grapples with impact of cores mode

By Peter Clarke and Brian Fuller

EDINBURGH, SCOTLAND – Intellectual property cores were a hot topic last week, both here at the IP99 Europe conference and at Dataquest Inc.'s annual semiconductor conference in Indian Wells, Calif. But as the industry struggles with new business models, new customer-supplier relationships and fast-moving technology, there was scant agreement on either side of the Atlantic on how the cores market will unfold.

On one thing there was agreement: IP cores and design reus

In some apps, multichip modules do the job more cheaply, conference told

'System-in-package' could make SoC a niche

▸CONTINUED FROM PAGE 1

and complexity to their logic devices in order to place analog and memory functions onto chips. "But when we get below 0.2 micron we get a cost shock, and the [return on investment] will be diminished or even eliminated in many cases," said Clark Fuhs, vice president and director of Dataquest's Semiconductor Manufacturing Programs.

Mask costs will dramatically rise at deep submicron because of the use of phase-shift and optical proximity correction techniques as well as more expensive, 193-nm lithography equipment, putting low-volume SoC at a cost disadvantage, Fuhs said.

Militating against SoC designs for many applications is the wide disparity in revenue per square inch among the various blocks in the chip, Fuhs said. "The DSP or microprocessor block can be getting $150 or $200 per square inch, the FPGA about $120, the analog block about $35, the memory block about $50 to $60 . . . You're basically diluting your high-value logic pieces with all these other low-value pieces, yet you're adding cost because you're adding mask levels."

An alternative is to fabricate the different blocks as discrete chips, placed close together using chip-scale packaging, Fuhs said. "This enables you to build the pieces in fabs that are optimized for those pieces. You can build analog in a 0.7-micron fab, standard logic can be done in 0.35 or even 0.5 micron, and for the memory you can buy a wafer from somebody and break it up. The package is more expensive, but the overall system cost is going to be substantially less.

"The concept here is to take some level of interconnect . . . and simply move [it] from the chip into the package."

Fuhs noted that Intel's Pentium III is actually an 11-level-metal device—six levels of aluminum inside the chip and five levels of copper outside. And he showed a photograph of a Sony digital Handycam, which he said contains 20 chip-scale devices, "so this technology is here, it's real."

National's Halla touts 'integrated disintegration.'

In the not-too-distant future, he said, wafer foundries will give customers a choice of implementing a design either as a system-on-chip or as several discrete devices using chip-scale packaging.

To survive, the SoC must evolve to fit a more standard-product model that would allow it to increase volume and become more cost-efficient, Fuhs said. He predicted that within five years, multichip packaging will be growing faster than SoC designs.

That view has its detractors. "Mask sets cost in excess of a couple hundred thousand dollars, whether you do small chips or large chips," said National Semiconductor Corp. chief executive officer Brian Halla, who has championed the notion of an information appliance-on-a-chip. "I can get tremendously more performance out of the same square inches of silicon by having it all together instead of having it two inches apart on a board.

"SoC isn't a marketing crusade anymore; it's something you can do because the technology allows it," Halla added. "A very small die can contain an awful lot of functionality."

Halla noted that Intel used to say graphics shouldn't be combined with the microprocessor, because the pace of innovation differs between those parts; but Intel's upcoming Timna processor, he said, combines both functions.

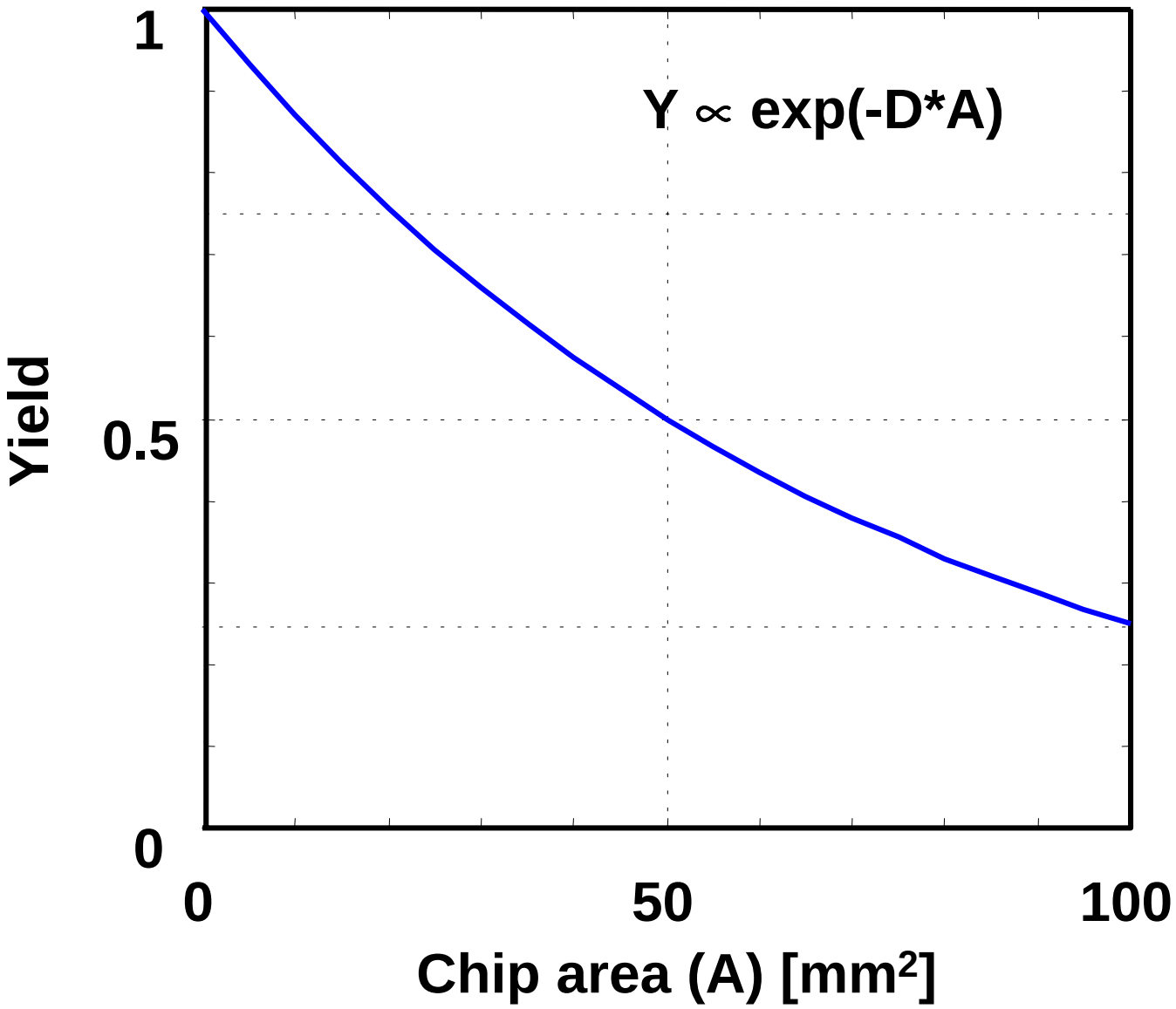
"Having said all that, there are cases where we agree [about putting a system on a package]," he said. "There is a substrategy of ours called integrated disintegration, which means there are analog functions you can pull off the chip because they are such a tiny portion of the overall chip, and yet they are the most difficult thing to port to the next-generation [process] technology."

IBM's Kelly said that "SoC integration has to be done se-

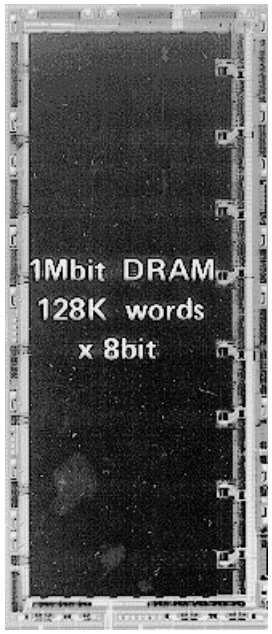
Issues in System-on-Chip

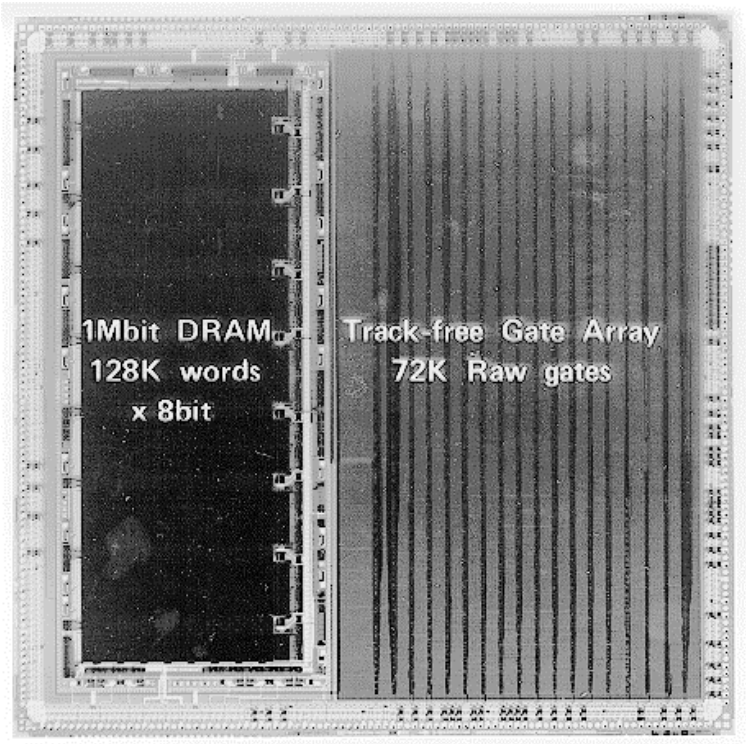
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

Yield



DRAM embedding





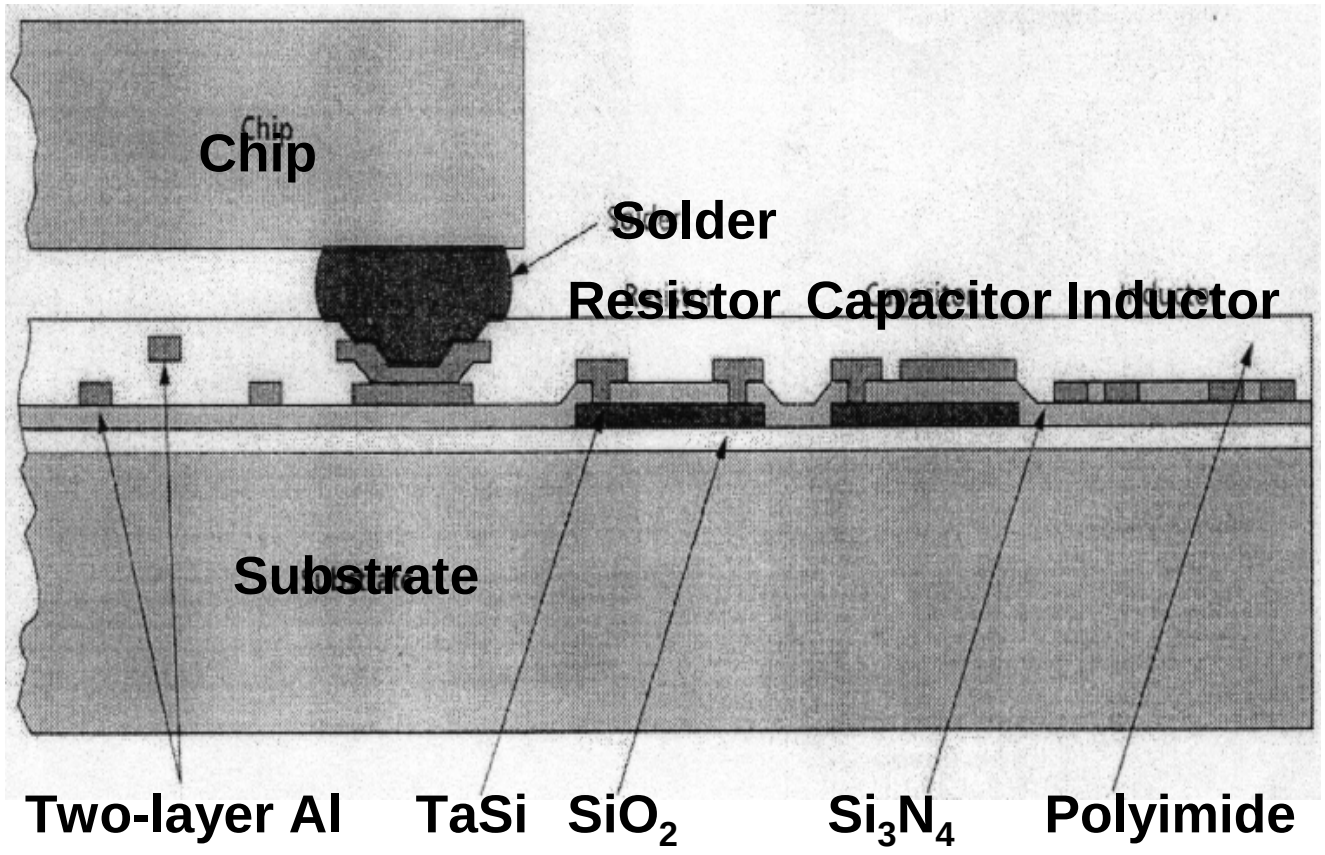
DRAM **Processor** **System LSI**

K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- **Two orders of magnitude improvement in bandwidth and power**

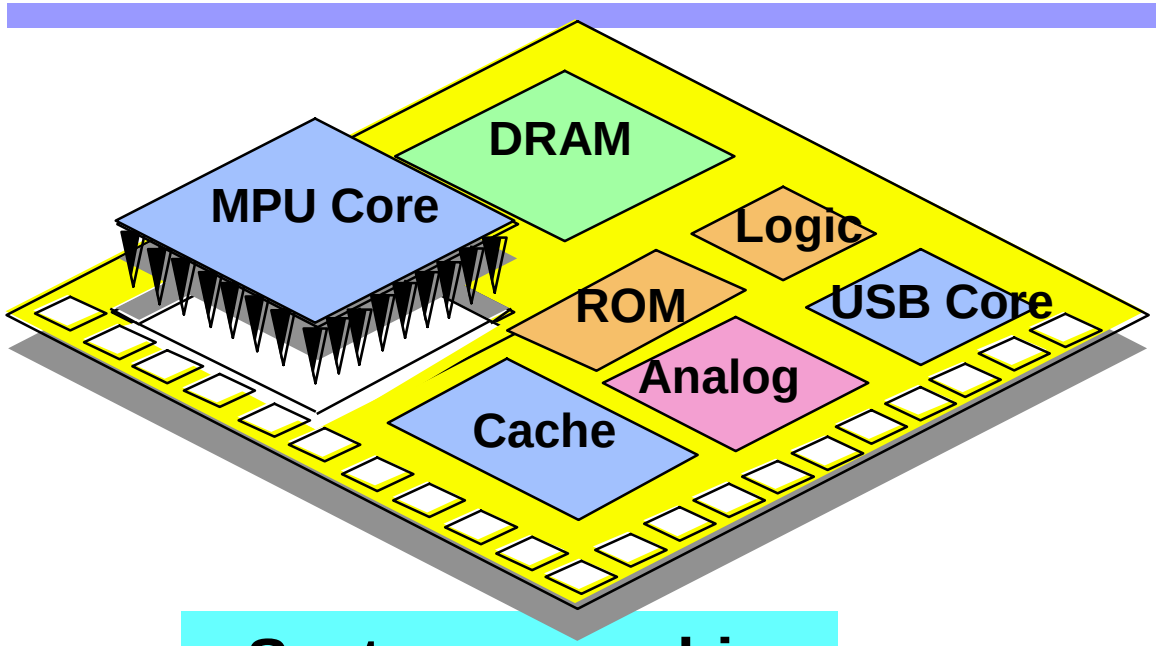
BUT EXPENSIVE!

System-in-Package (SIP)

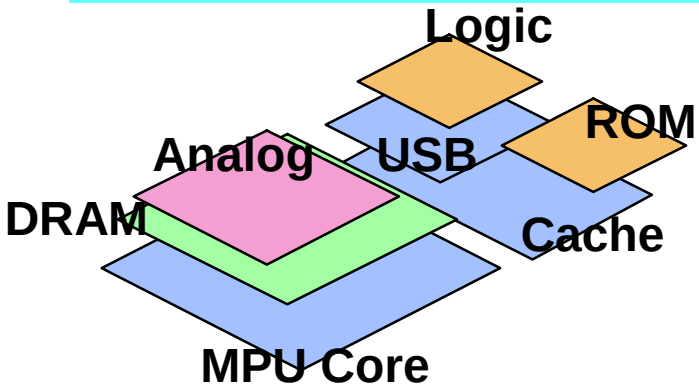


K.L.Tai, "System-In-Package (SIP): Challenges and Opportunities," ASPDAC, pp.191-196, Jan. 2000

3-Dimensional assembly



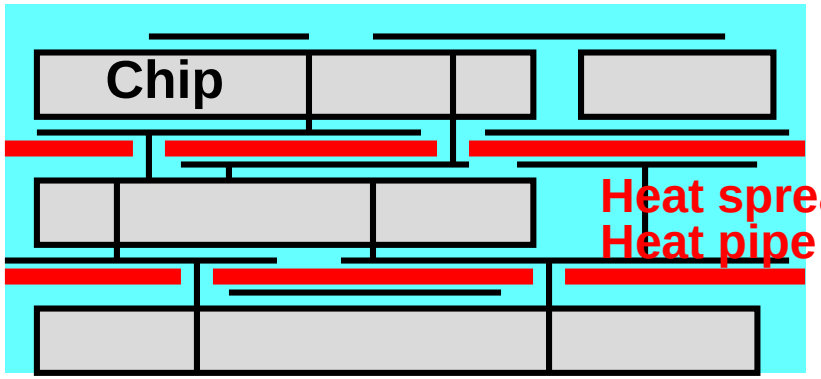
System on a chip



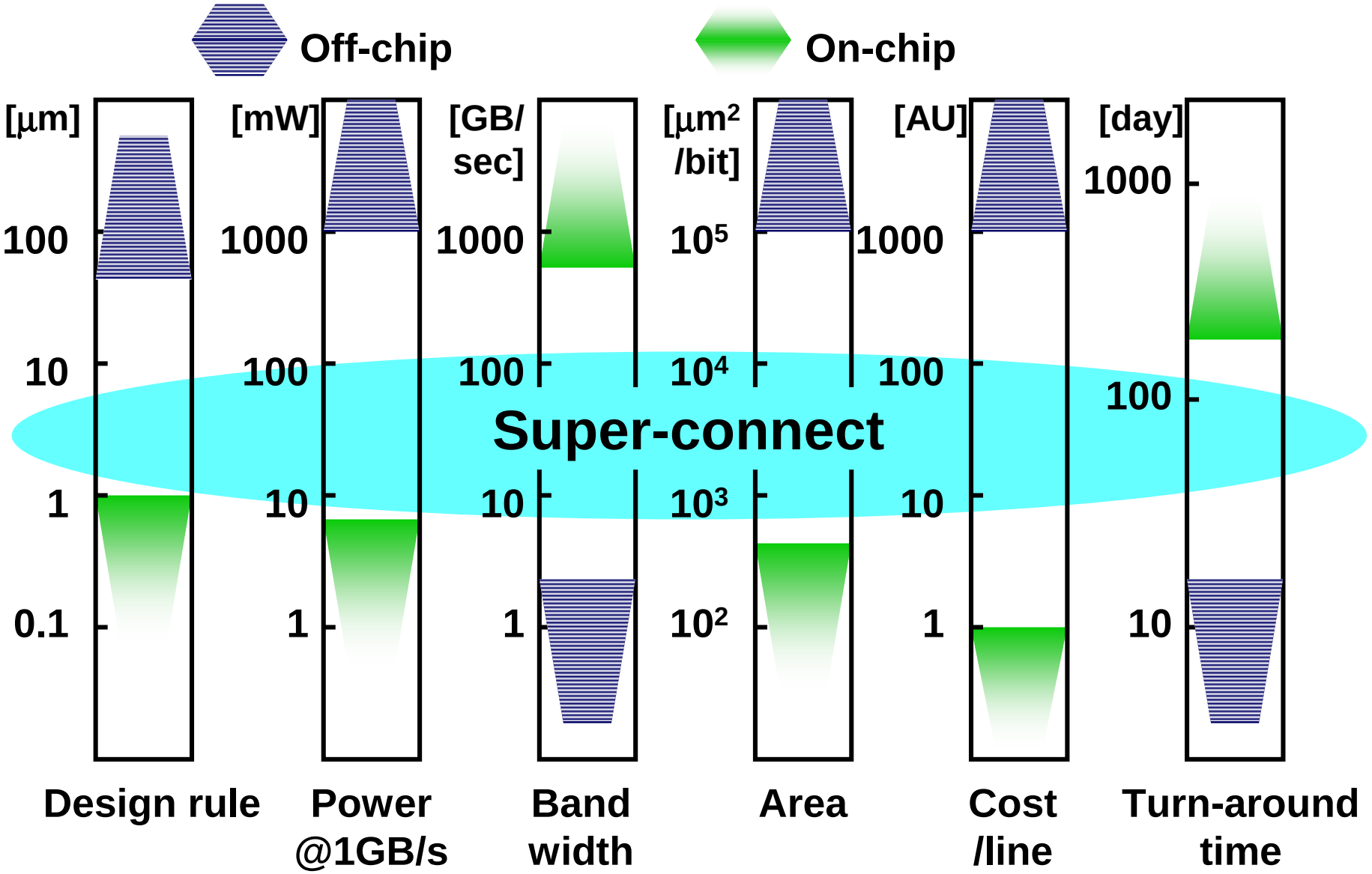
3-D assembly

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

- Heat dissipation is an issue



Super-connect

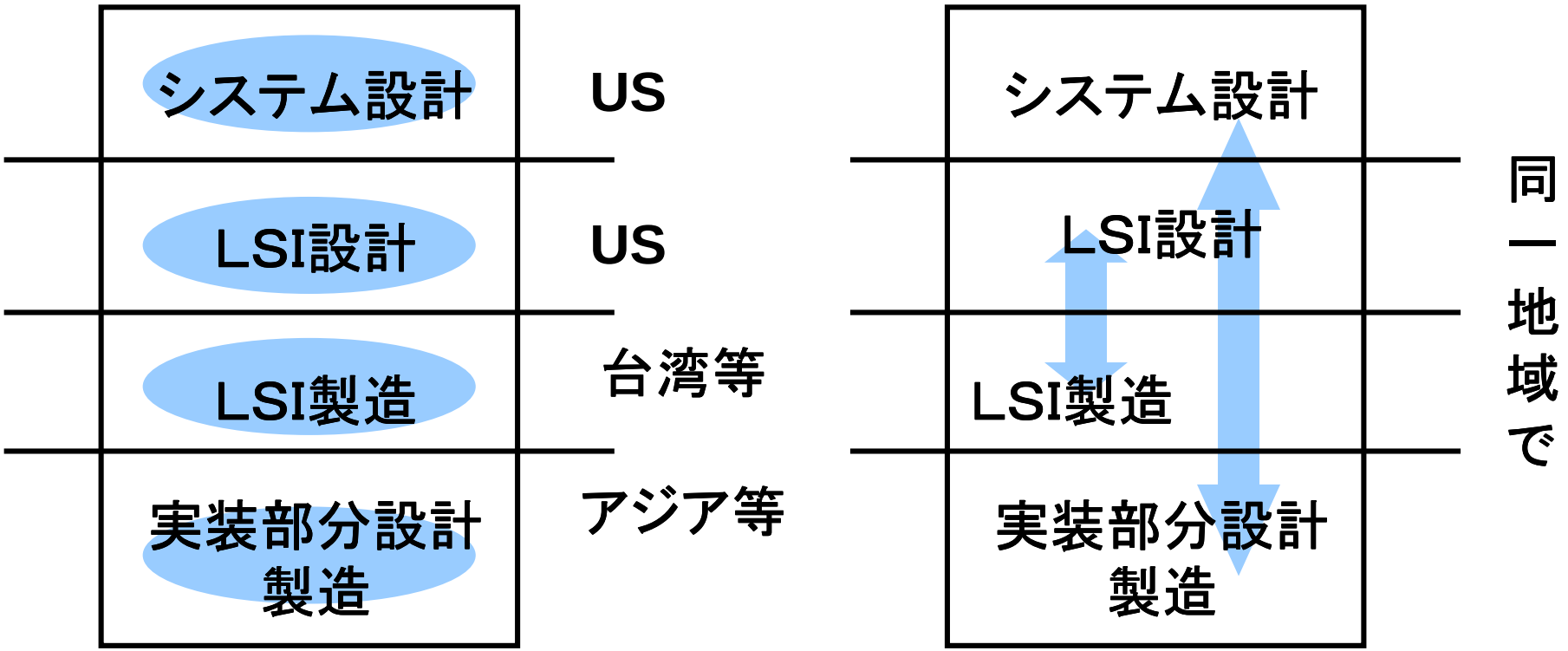


T.Sakurai

System-in-Packageの課題

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

水平分業と垂直統合



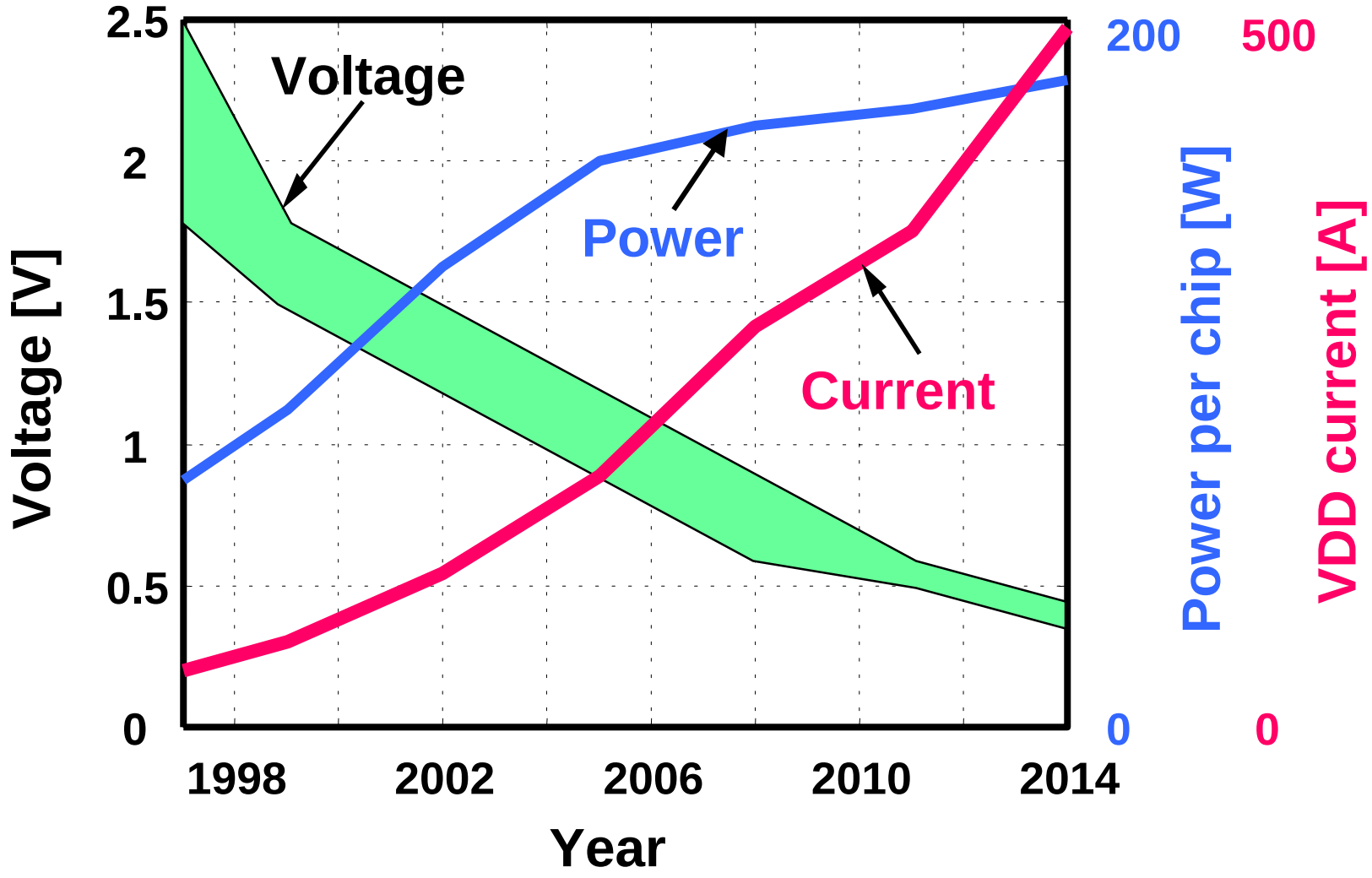
ASIC、デジタル、SoC

メモリ
アナログ
CPU

SoC

SiP

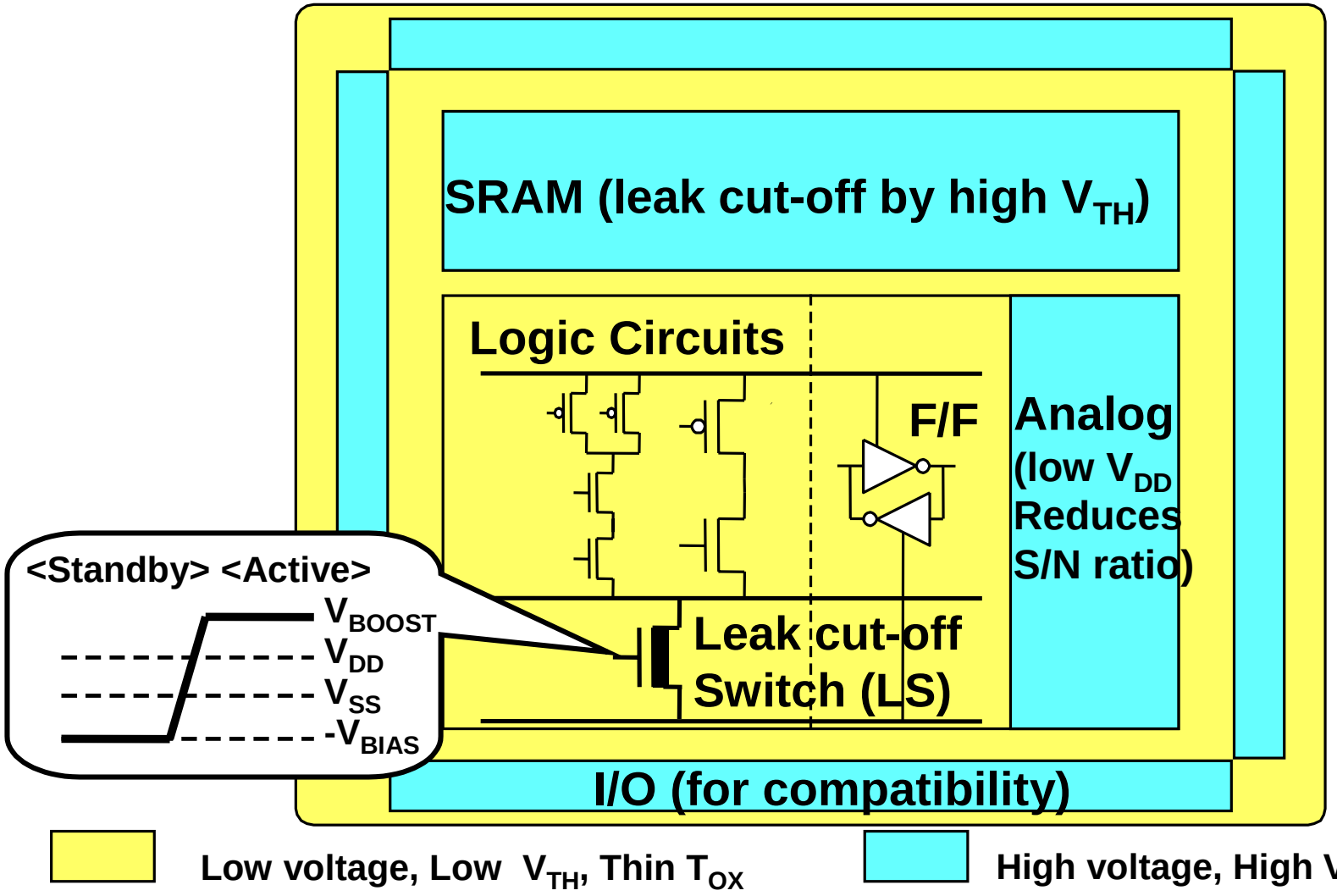
VDD, Power and Current Trend



International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

T.Sakurai

GSI's in deep-submicron era

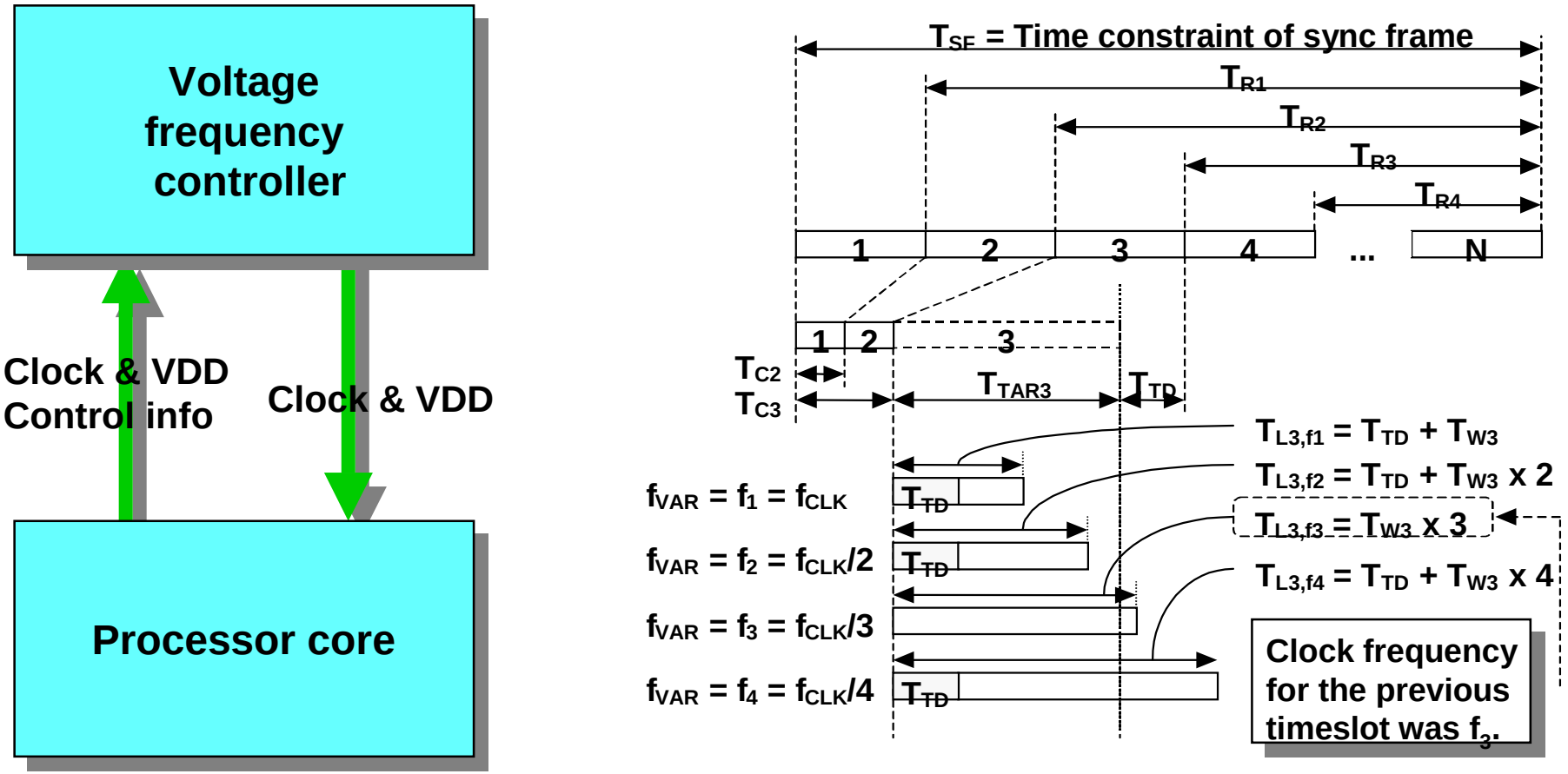


Low voltage, Low V_{TH}, Thin T_{OX}

High voltage, High V_{TH}, Thick T_{OX}

T.Inukai, M.Takamiya, K.Nose, H.Kawaguchi, T.Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC'00, p.409, May 2000.

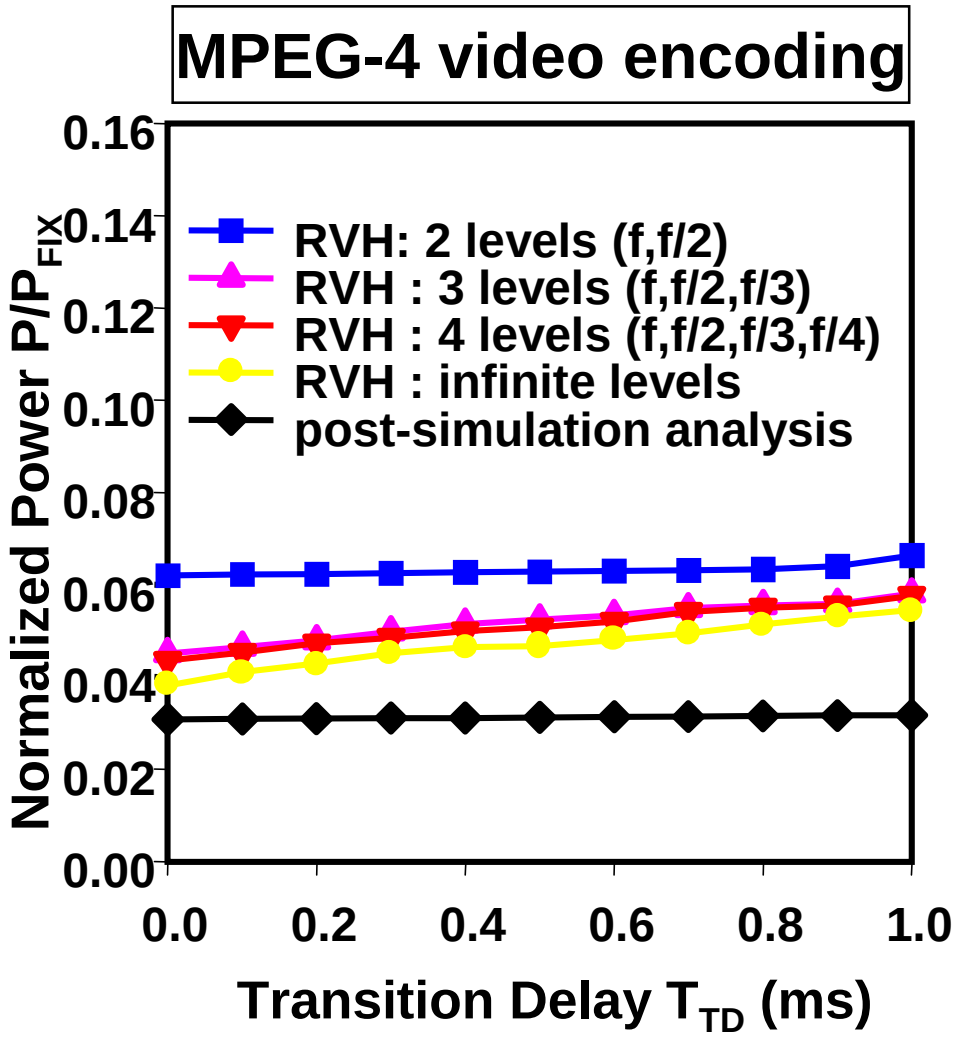
Application slicing and software feedback loop in Voltage Hopping

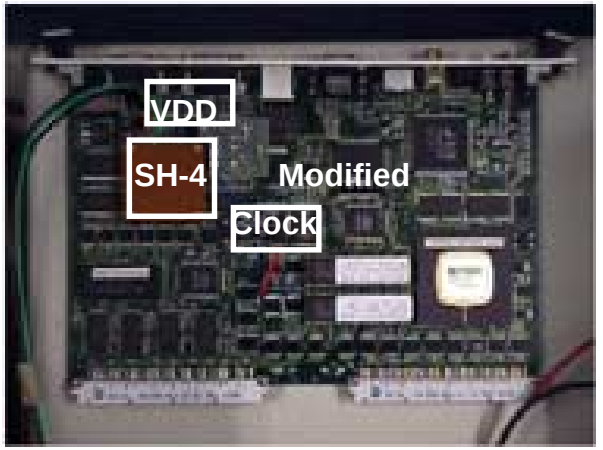


S.Lee and T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications,"ASPDAC'00, A5.2, pp.381~pp.386, Jan. 2000.

S.Lee and T.Sakurai, "Run-time Voltage Hopping for Low-power Real-time Systems," DAC'00, June 2000.

Run-time Voltage Hopping reduces power to less than 1/10

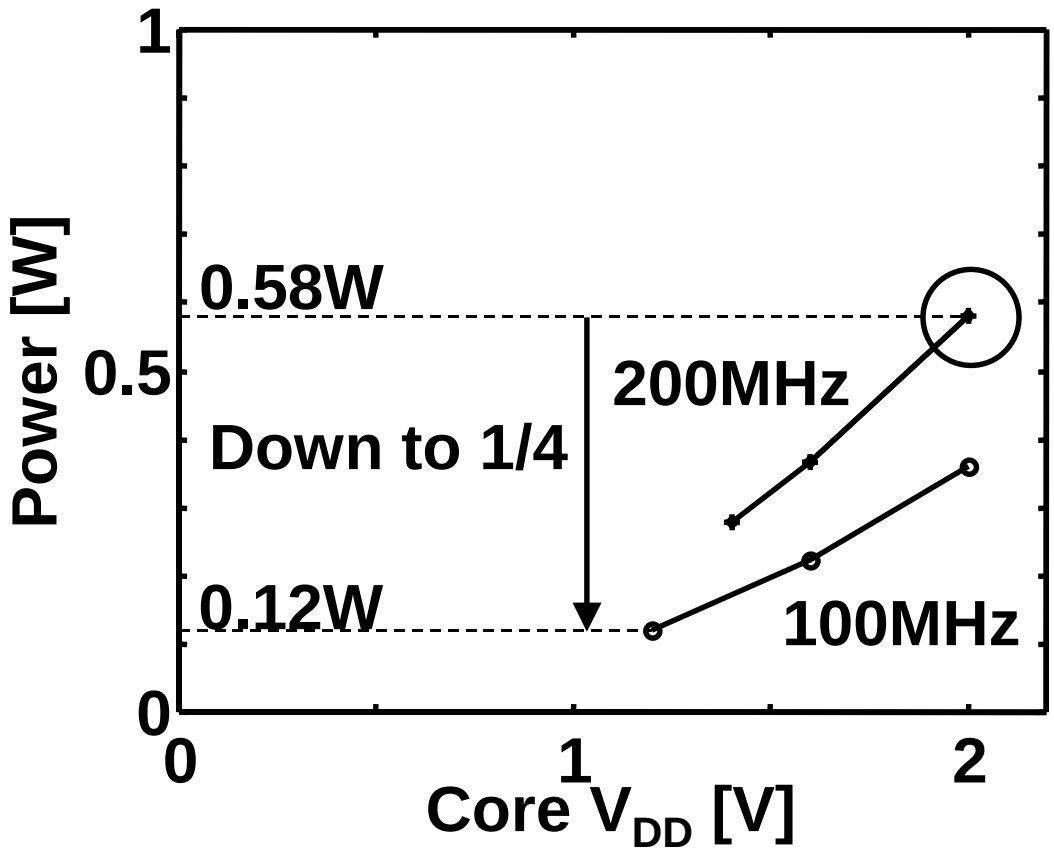




T.Sakurai

Measured power characteristics

Total power = 0.58 x 0.02 + 0.12 x 0.98 = 0.13W!



Just for 2% of Whole Period

RPC can cut down power consumption to 1/4

ロードマップによる将来予想

Year	Unit	1999	2014	Factor
Design rule	μm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (μP)		21M	3.6G	170
DRAM capacity		1G	1T	256
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	μcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

T.Sakurai

電子情報通信学会ソサイエティ大会パネル討論　’00/10

LSIの配線設計とシグナルインテグリティ

GSI配線の設計課題と解決策の模索

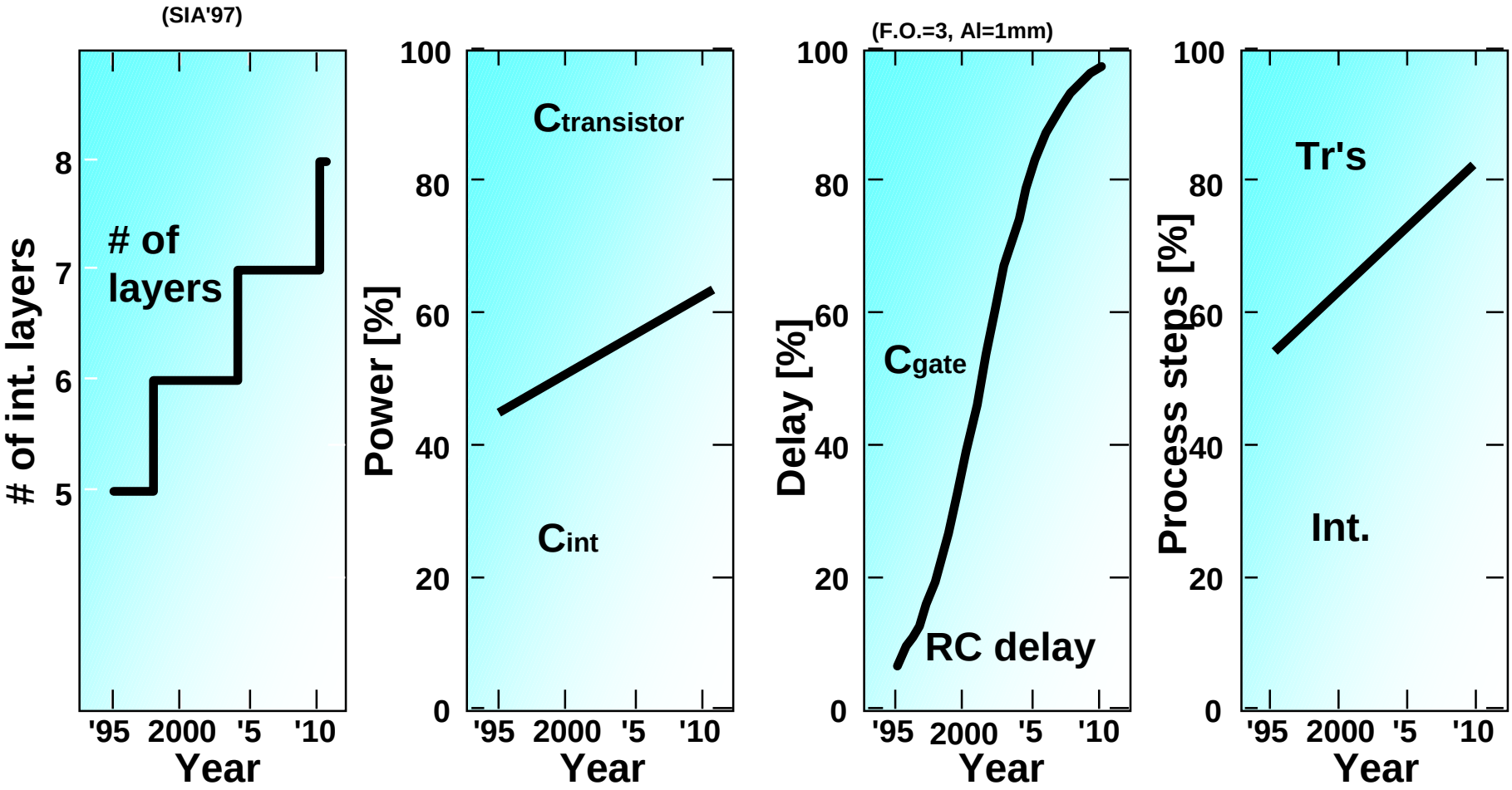
Prof. Takayasu Sakurai
Center for Collaborative Research, and
Institute of Industrial Science,
University of Tokyo
E-mail:tsakurai@iis.u-tokyo.ac.jp

DSM配線の課題

- 配線遅延の増大
- 配線間カップリングの増大によるシグナルインテグリティの低下
- インダクタンスによるシグナルインテグリティの低下
- IRドロップの増大
- 電流密度増大による信頼性の低下
- EMIの増大

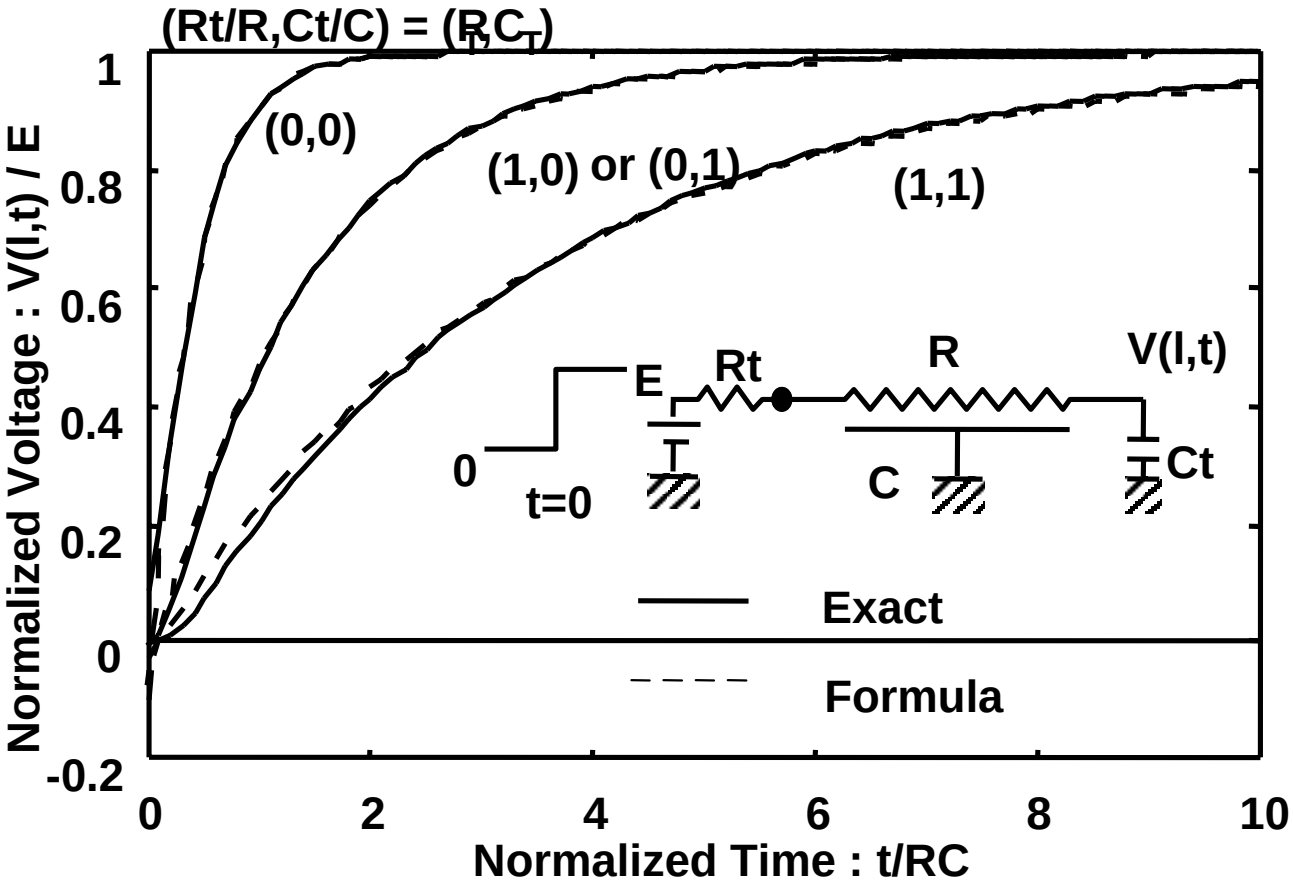
Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



T.Sakurai

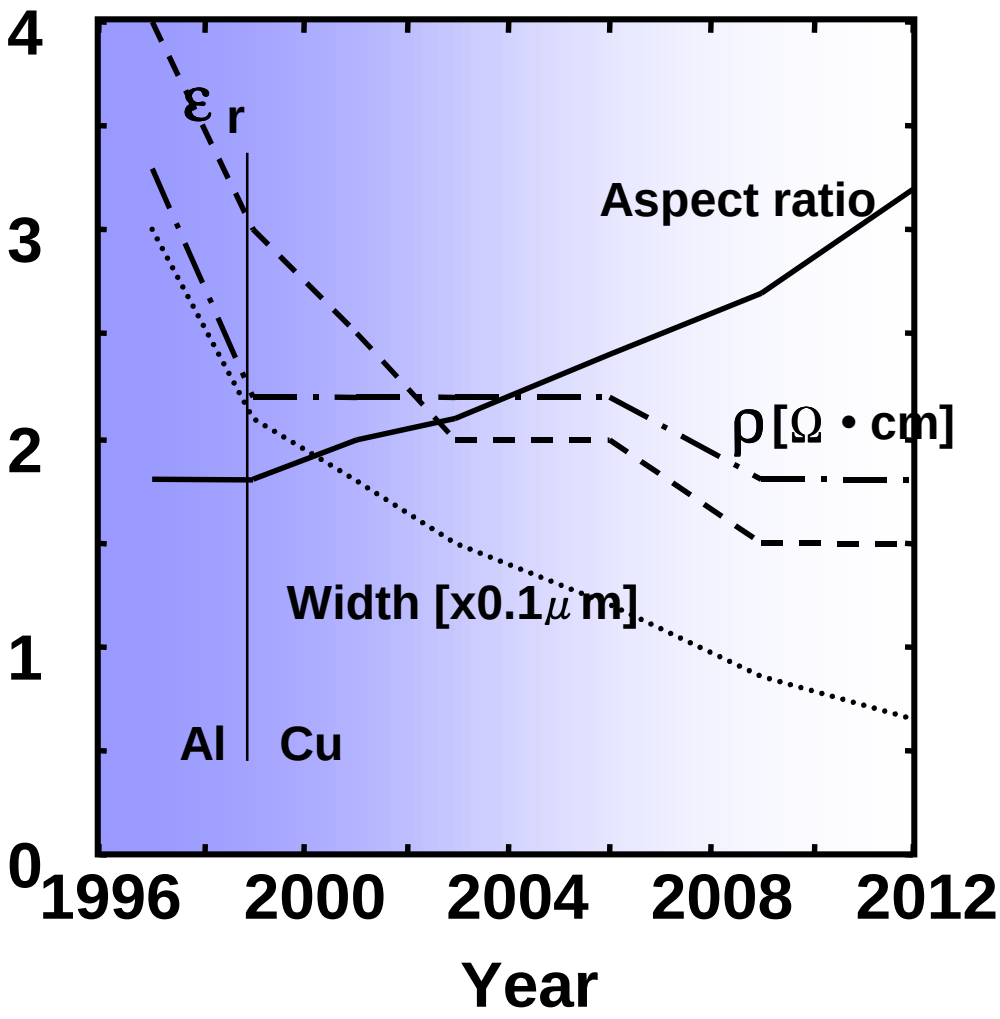
Voltage waveforms of a distributed RC line



$$\frac{V(l,t)}{E} \approx 1 - \exp\left(-\frac{t/RC - 0.1}{R_T C_T + R_T + C_T + 0.4}\right)$$

T.Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling and Crosstalk in VLSI's," IEEE Trans. on ED, Vol.40, No.1, pp.118-124, Jan.1993.

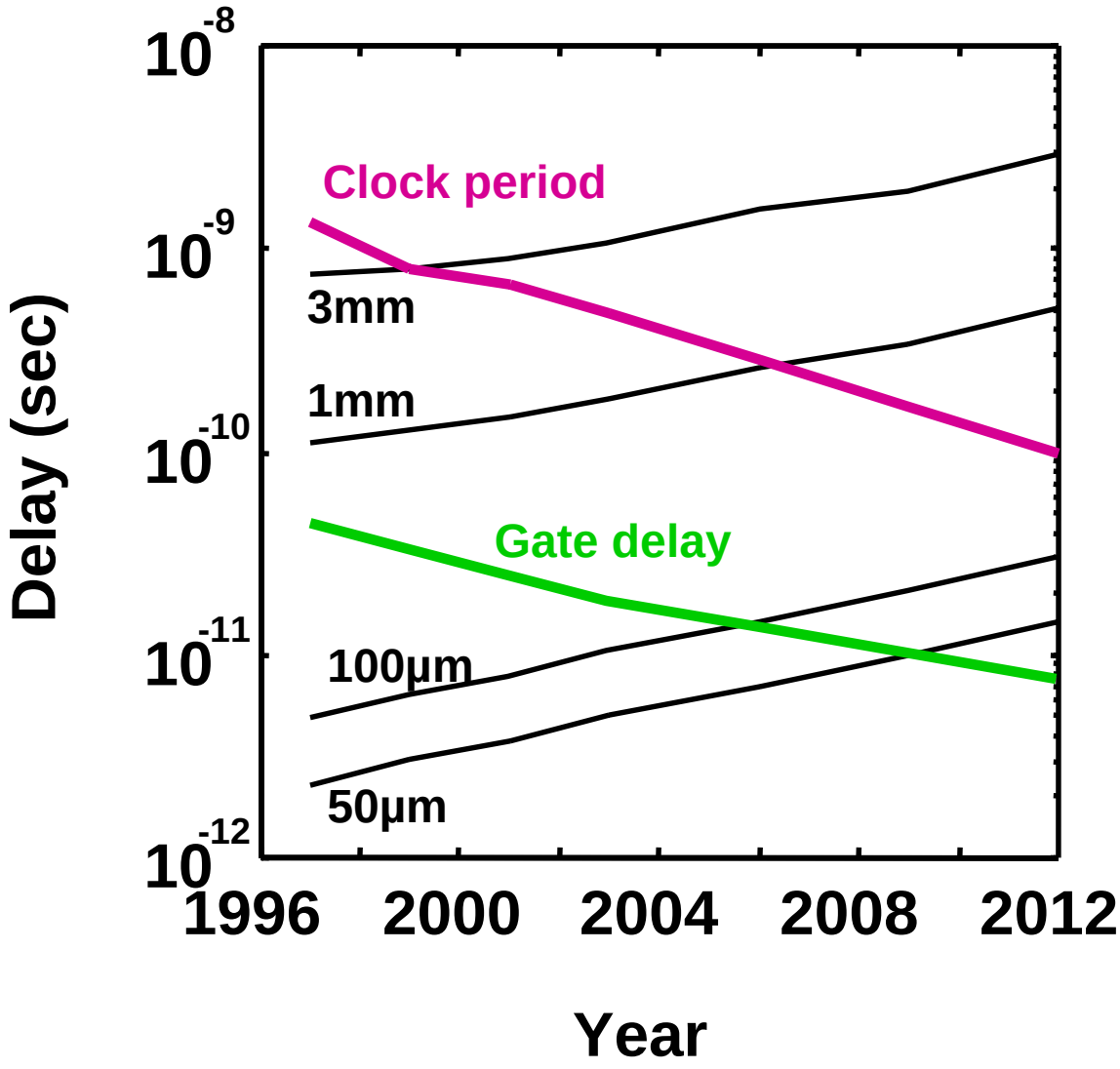
Interconnect parameters trend



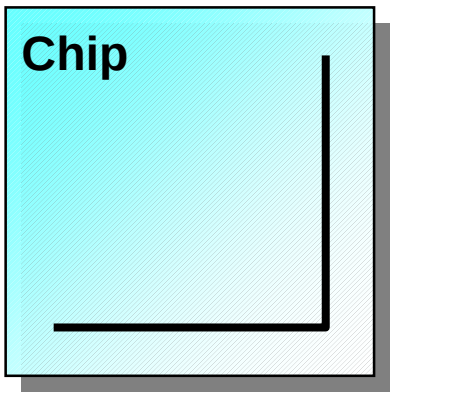
Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

T.Sakurai

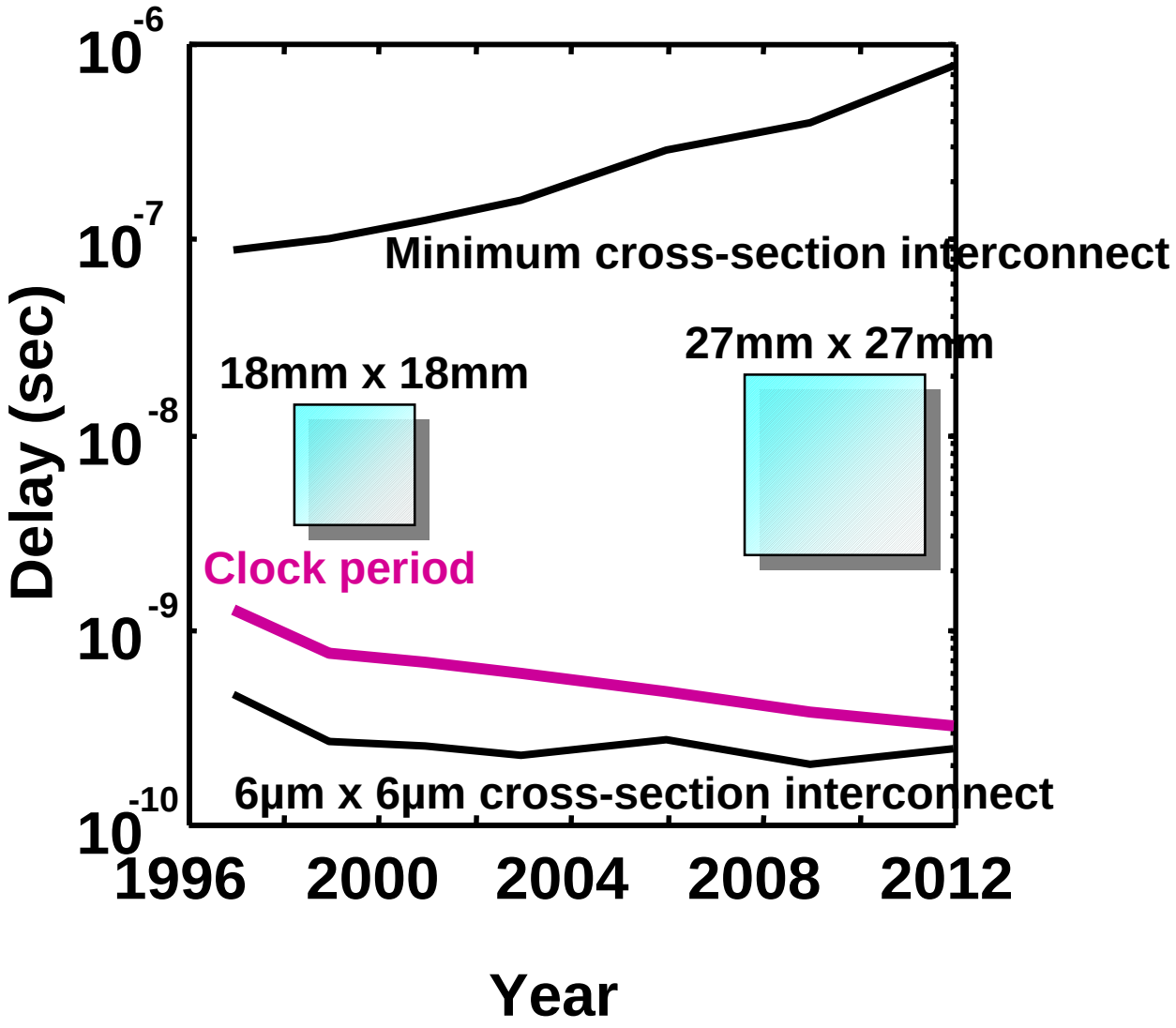
RC delay and gate delay



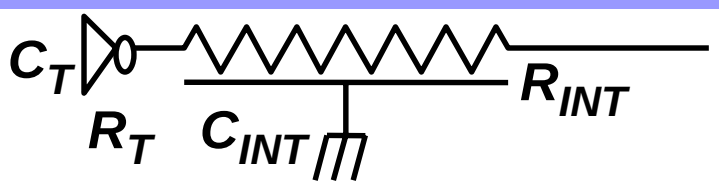
RC delay of global interconnections



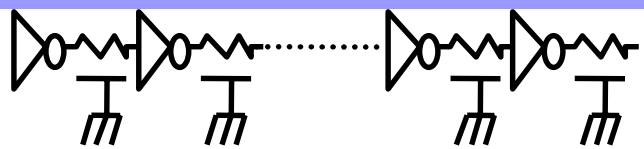
Global interconnect



Repeaters



a) Without repeaters



b) With repeaters

$$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693(R_T C_T + R_T C_{INT} + R_{INT} C_T)$$

C_0 : Gate capacitance of minimum MOSFET

R_0 : Gate effective resistance of minimum MOSFET

$$Delay \approx k\left[p_1 \frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h} h C_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k} h C_0 \right)\right]$$: Buffered

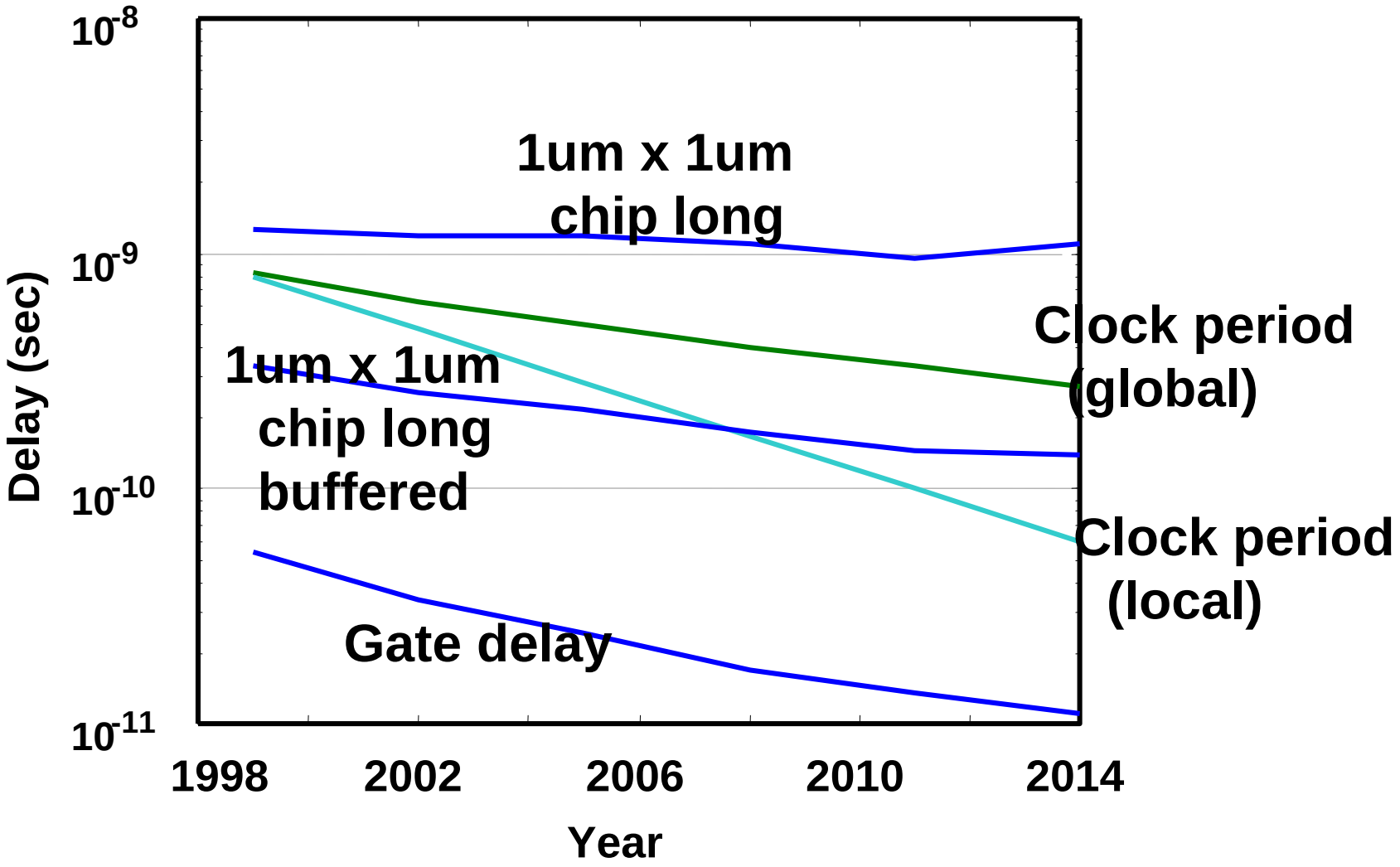
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT} R_0}{R_{INT} C_0}}$$: Optimized size of buffer inverter

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}}\sqrt{\frac{R_{INT} C_{INT}}{R_0 C_0}}$$: Optimized number of stages

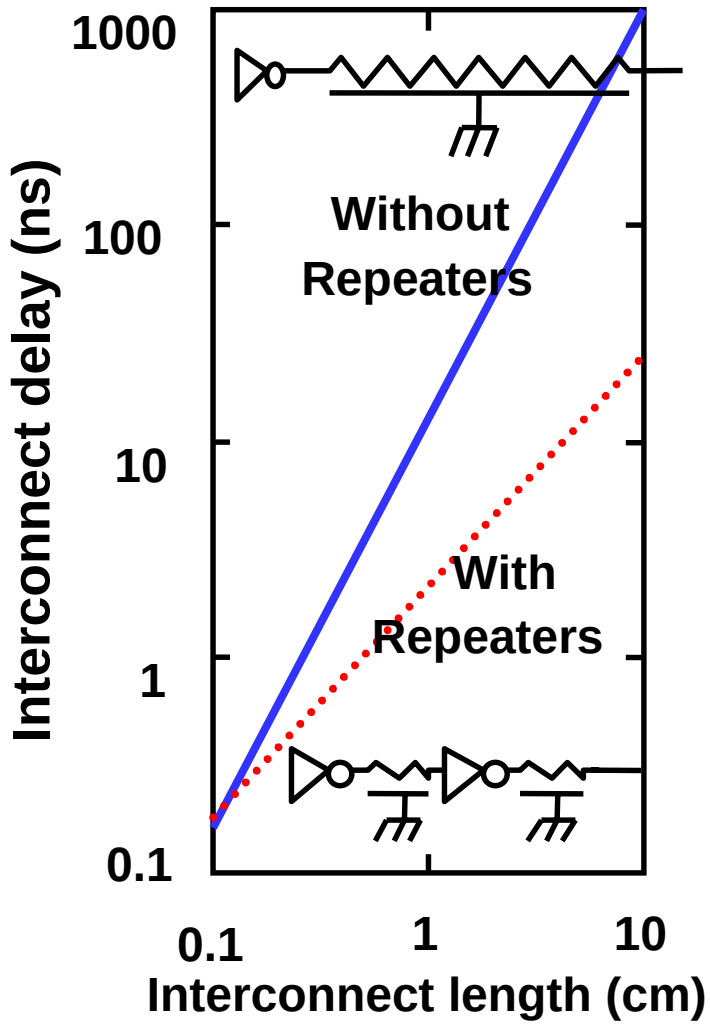
$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right)\sqrt{R_{INT} C_{INT} R_0 C_0} \approx 2.4\sqrt{\tau_{INT}\,\tau_{MOS}}$$

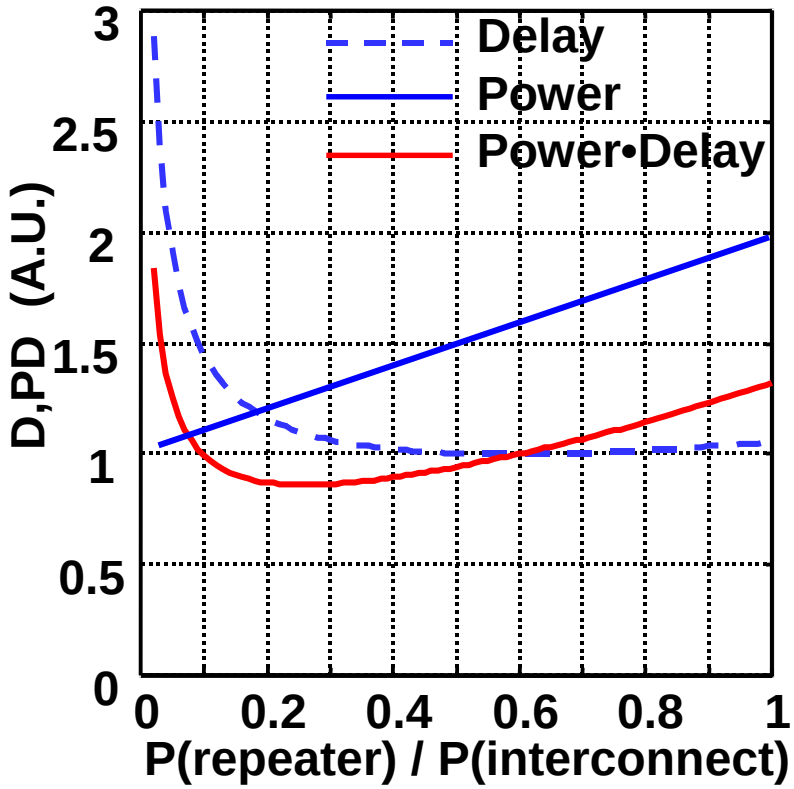
$$Cap.\ of\ gates = k_{OPT} h_{OPT} C_0 = \sqrt{p_1 / p_2}\, C_{INT} = 0.73 C_{INT}$$

Buffered interconnect delay



Delay and Power Optimization for Repeaters





Delay optimized

→P: P(repeater)=0.60 P(interconnect)

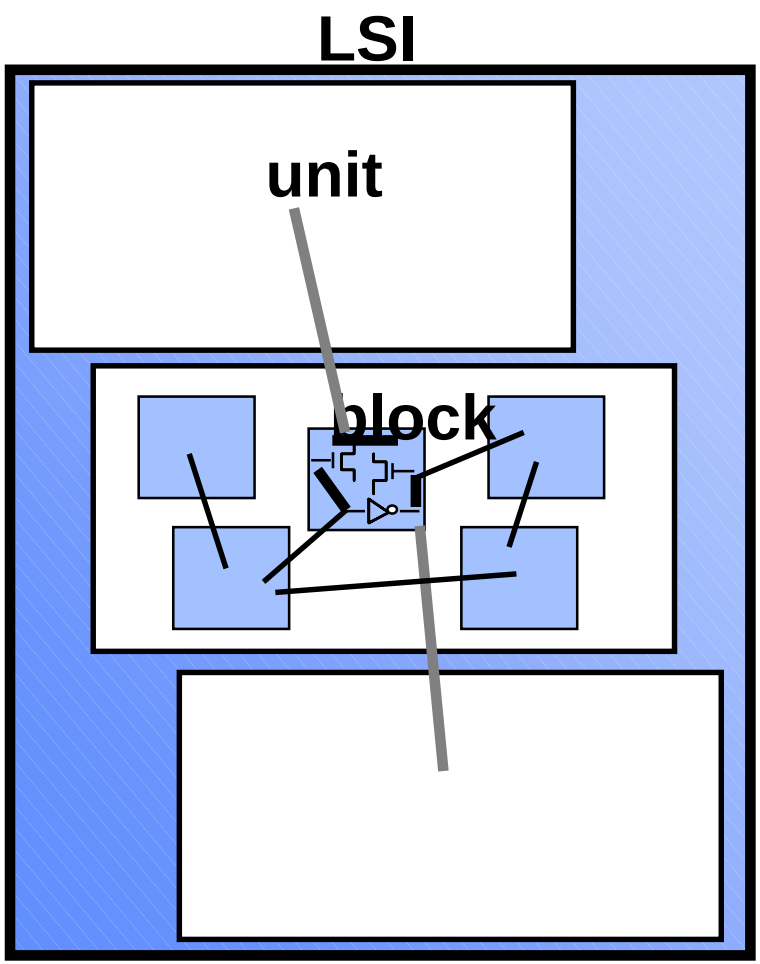
Power•Delay optimized

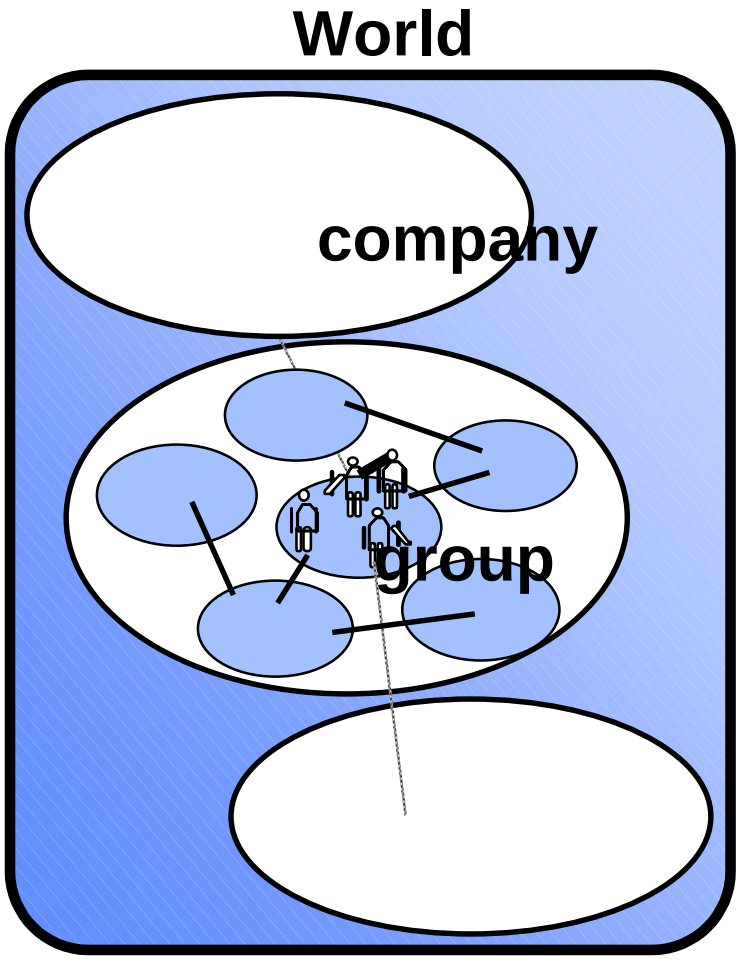
→D: 1.09 Dopt

→P: P(repeater)=0.26 P(interconnect)

→PD: 0.86 of Dopt case

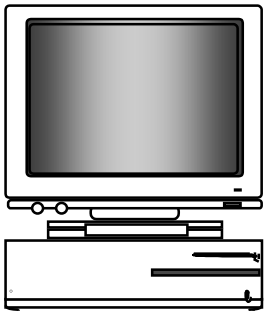
The further, the less





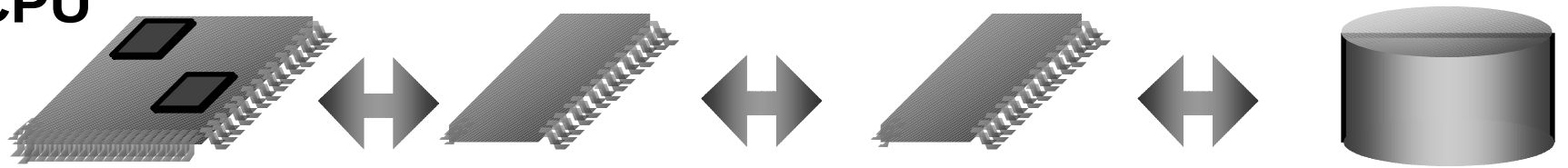
- Local memories
- Hierarchy

Locality in space & time



Use of local memories

CPU



1st cache 2nd cache Main mem. Ext. mem.

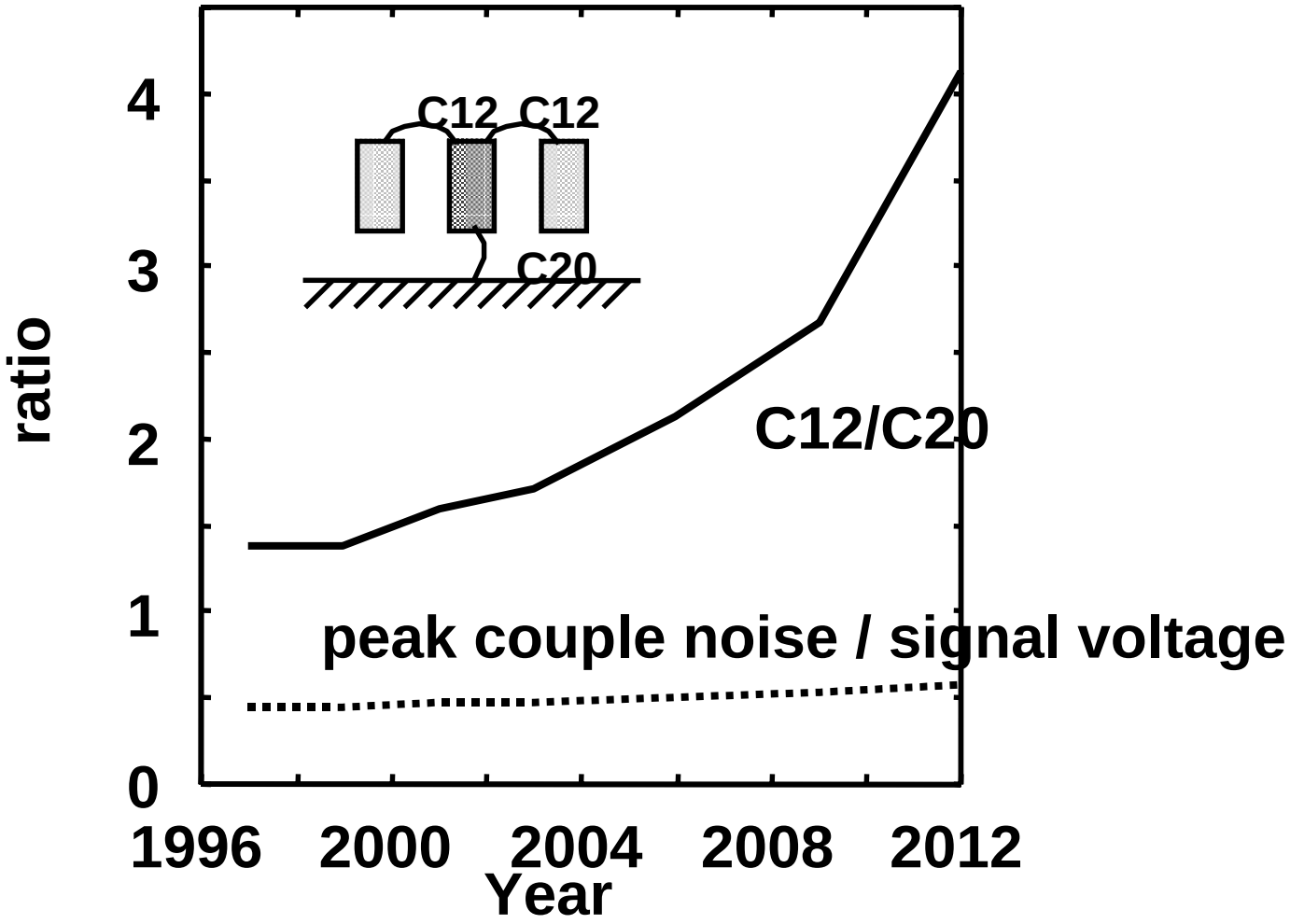
Latency

3ns 20ns 100ns 10ms

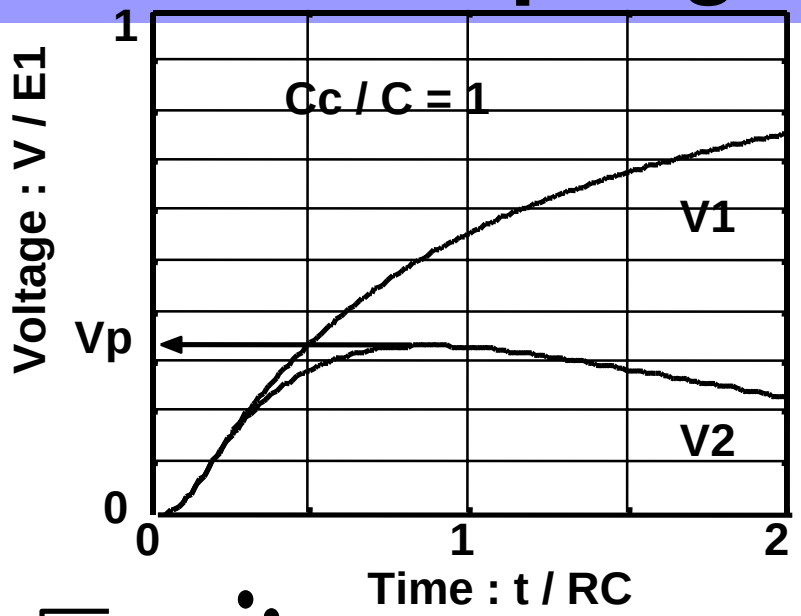
Throughput

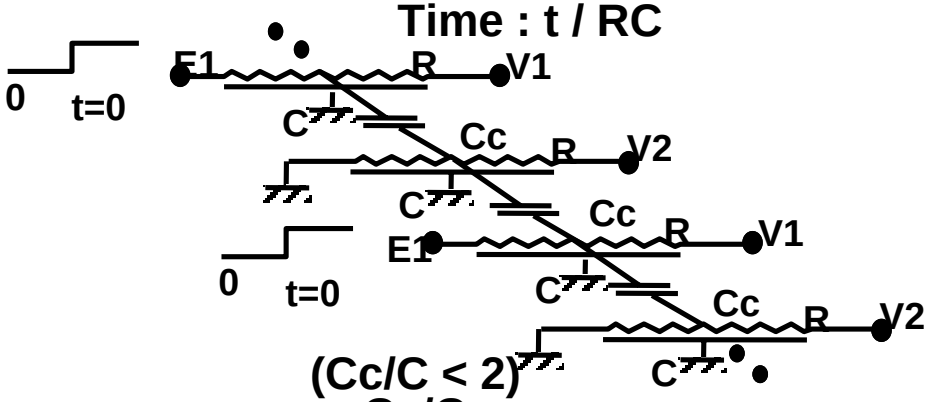
3ns 10ns 30ns 100ns

Capacitive Coupling Noise



Coupling noise in RC bus

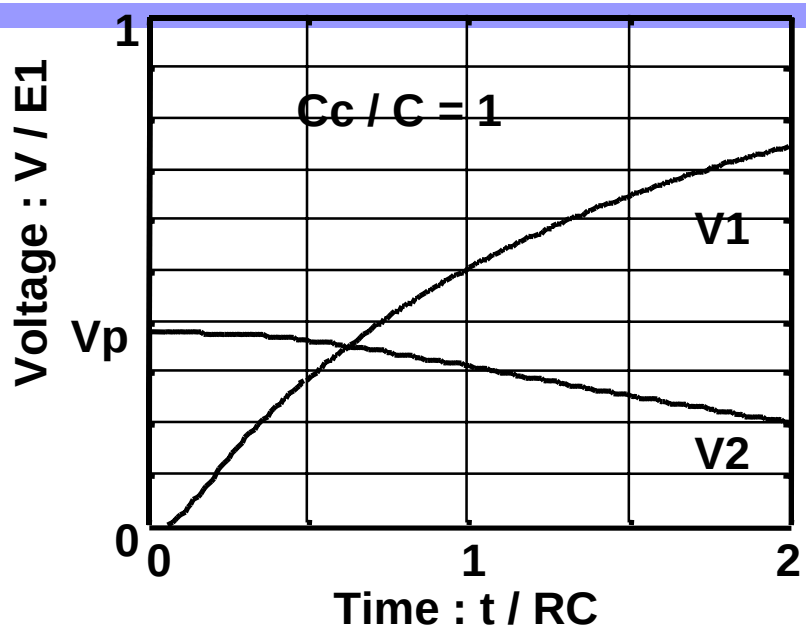


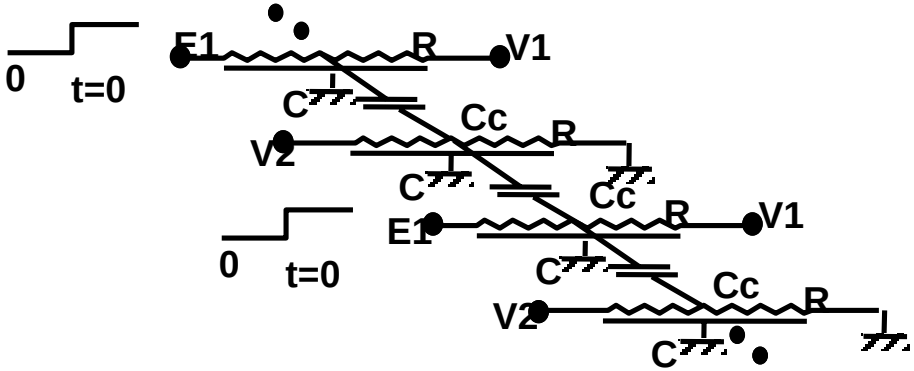


(Cc/C < 2)

$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$

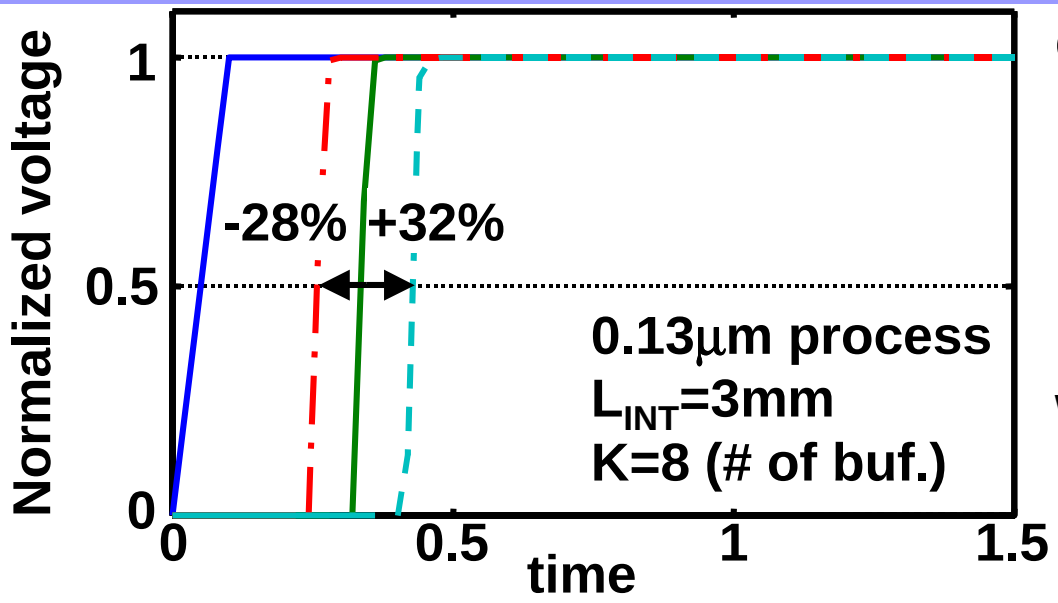


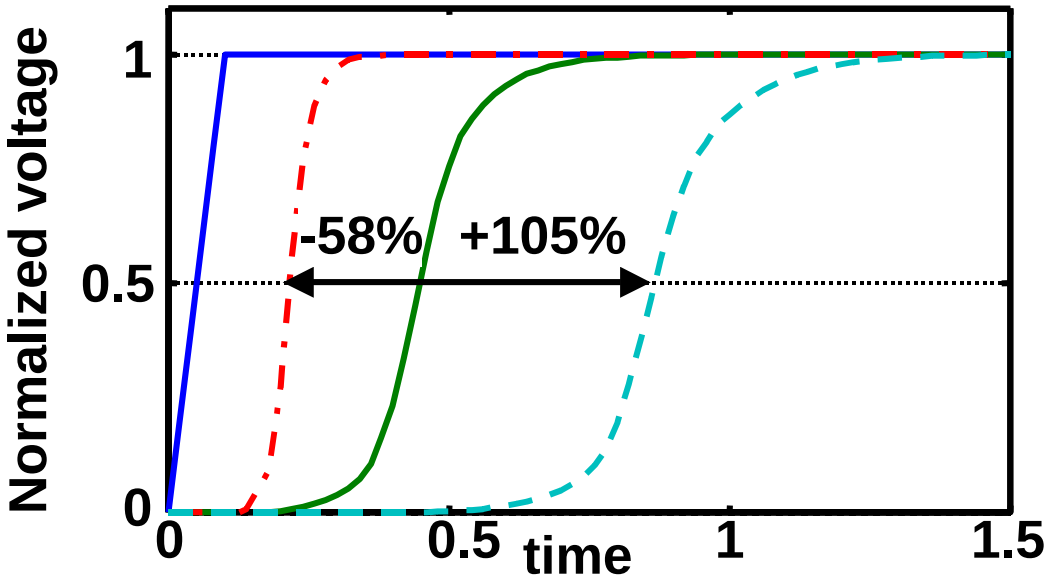


$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

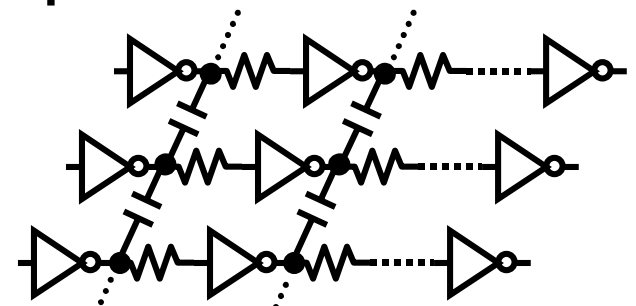
H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnections

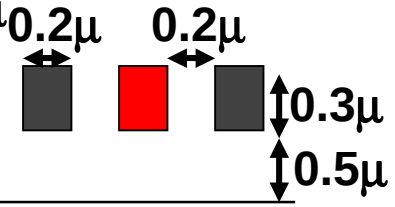


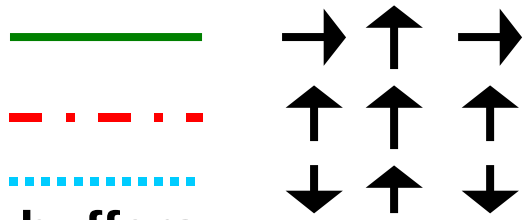


Optimized buffer insertion

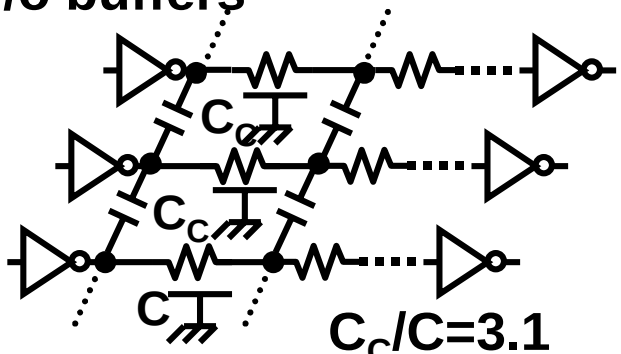


W_N/W_P=25μ/38μ



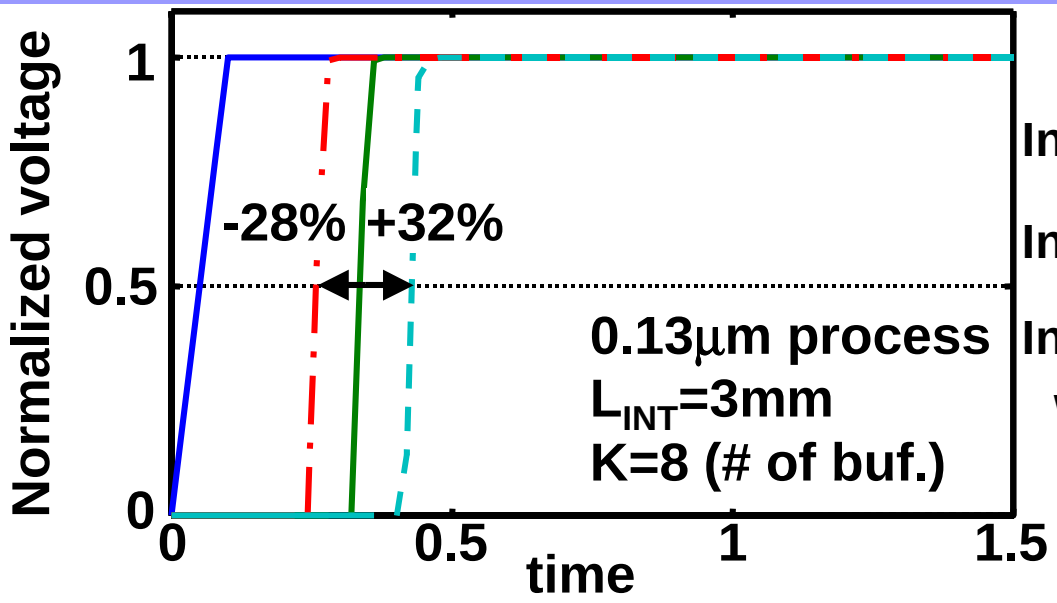


w/o buffers

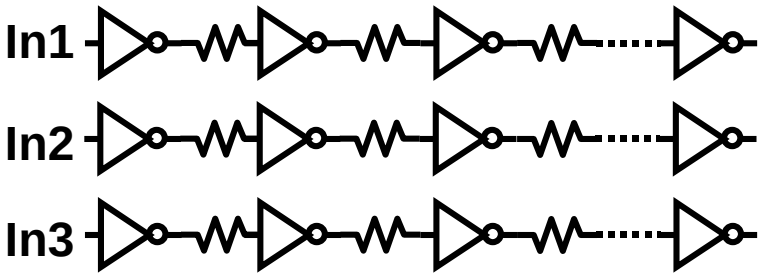


C_C/C=3.1

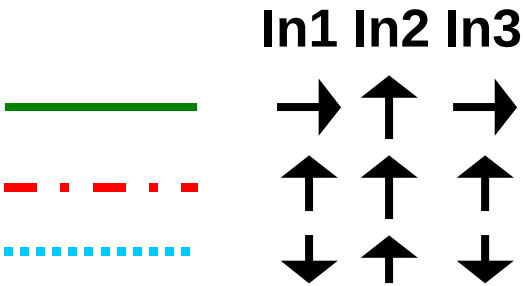
Coupling among Interconnections

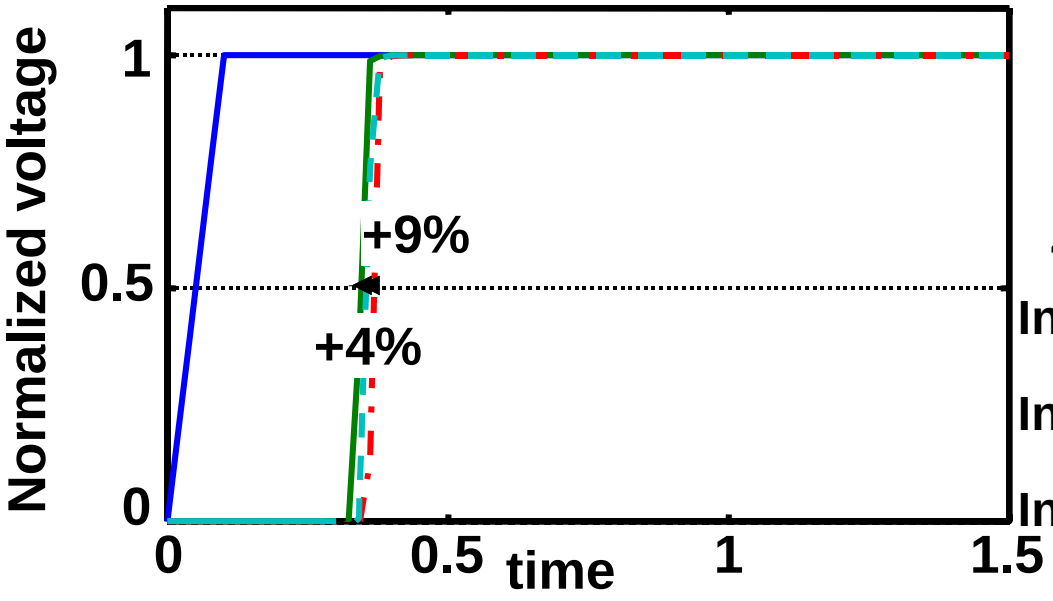


Normal buffer insertion

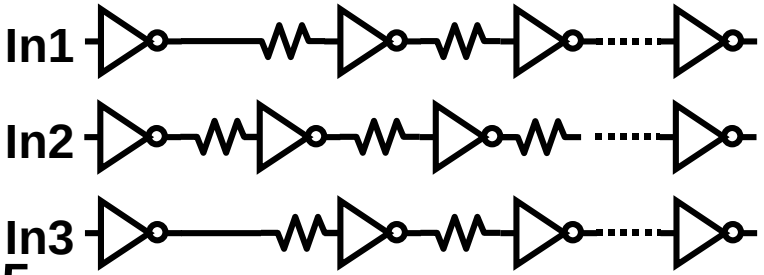


W_N/W_P=25μ/38μ

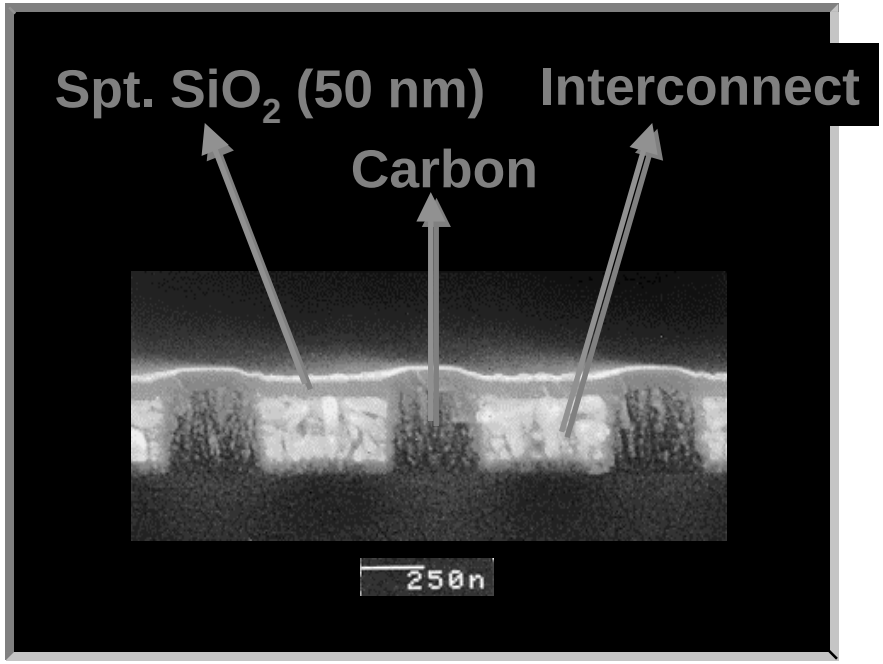




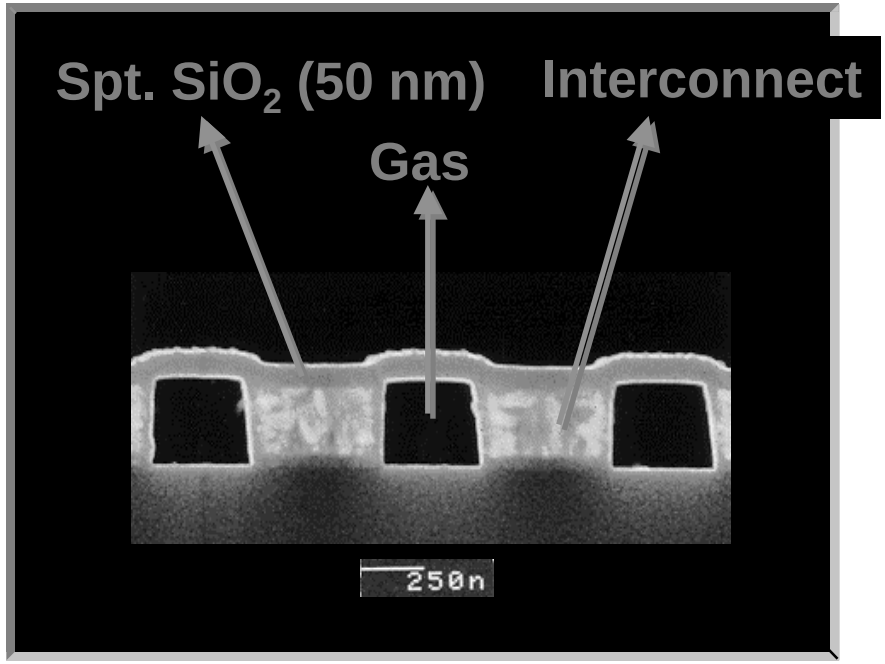
Zigzag buffer insertion



Air Isolation

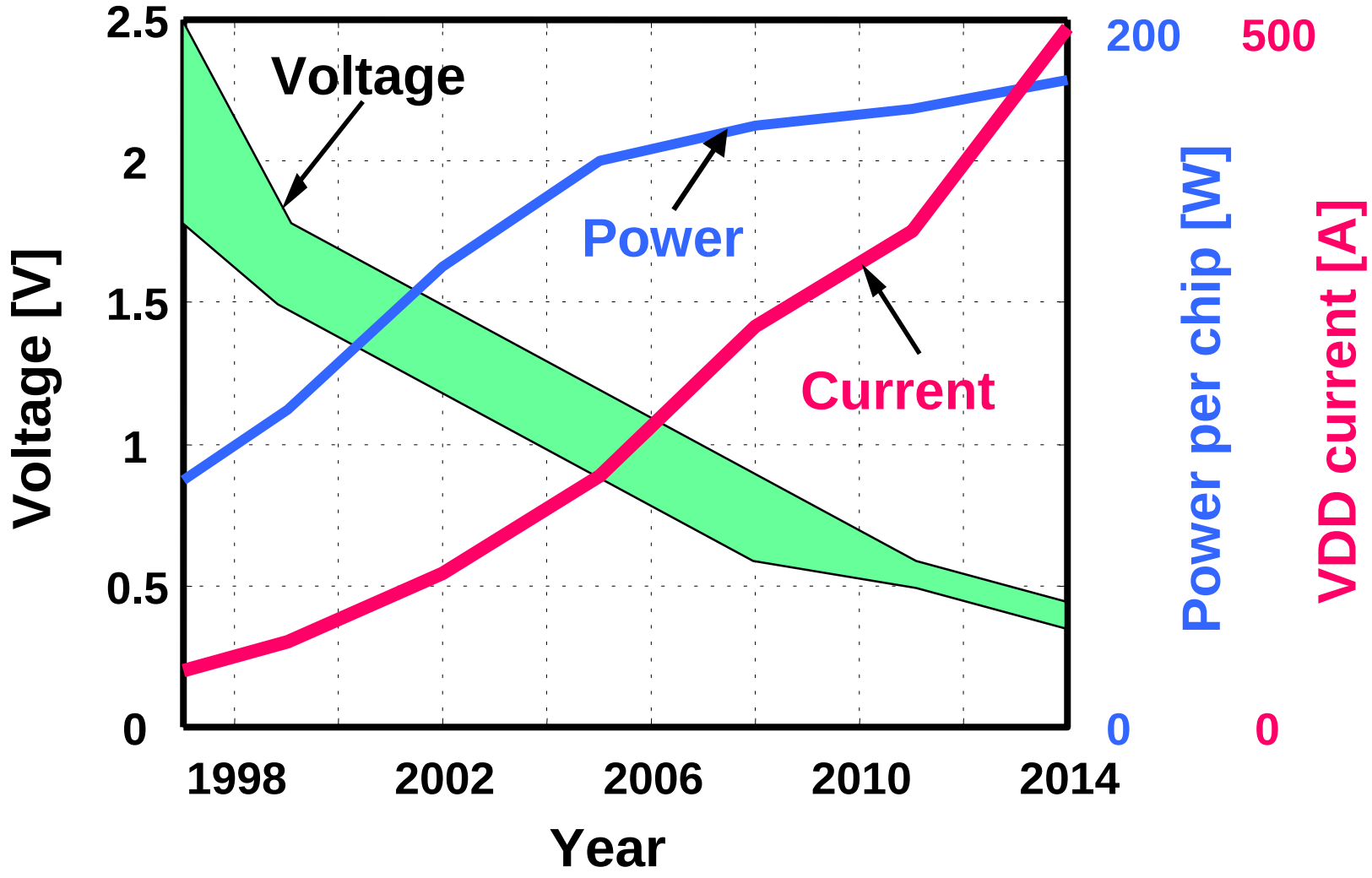


Before ashing



After 450C, 2H furnace ashing

VDD, Power and Current Trend



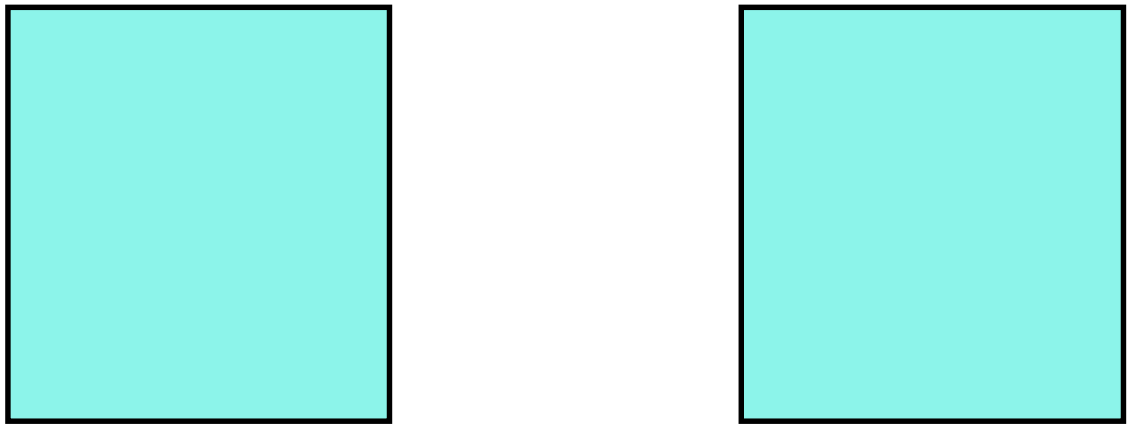
International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

T.Sakurai

Interconnect Cross-Section and Noise

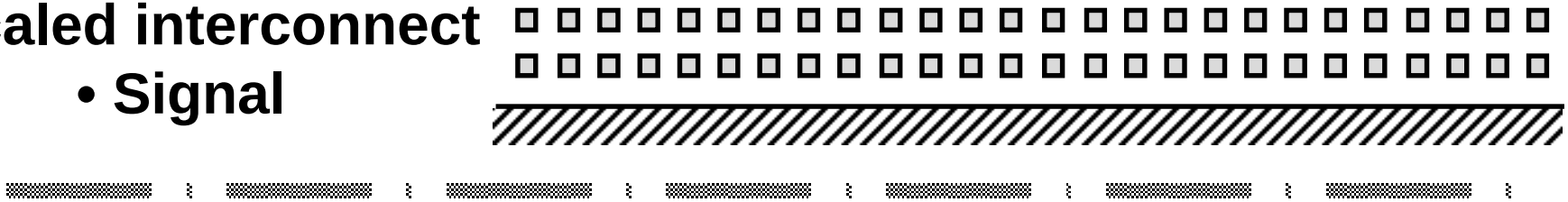
Unscaled / anti-scaled

- **Clock**
- **Long bus**
- **Power supply**



Scaled interconnect

- **Signal**

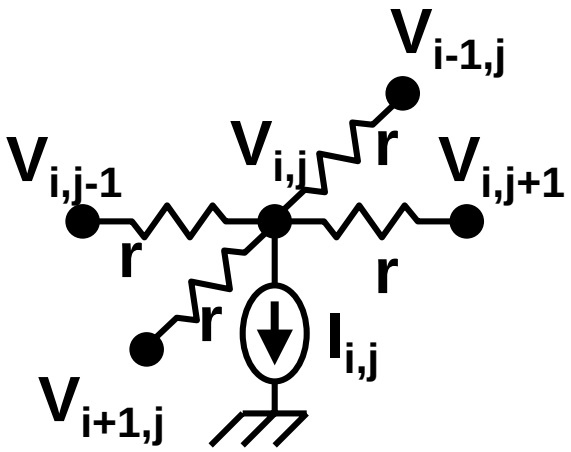


1V 50W -> 50A current

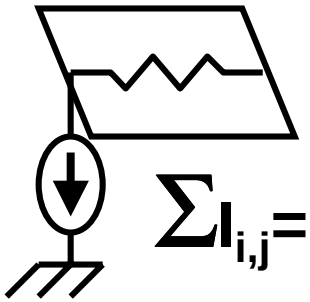
5% noise -> 0.05V noise -> 1mΩ sheet R -> 15μm thick Cu

Area pad + package, or thick layer on board is needed.

IR Drop

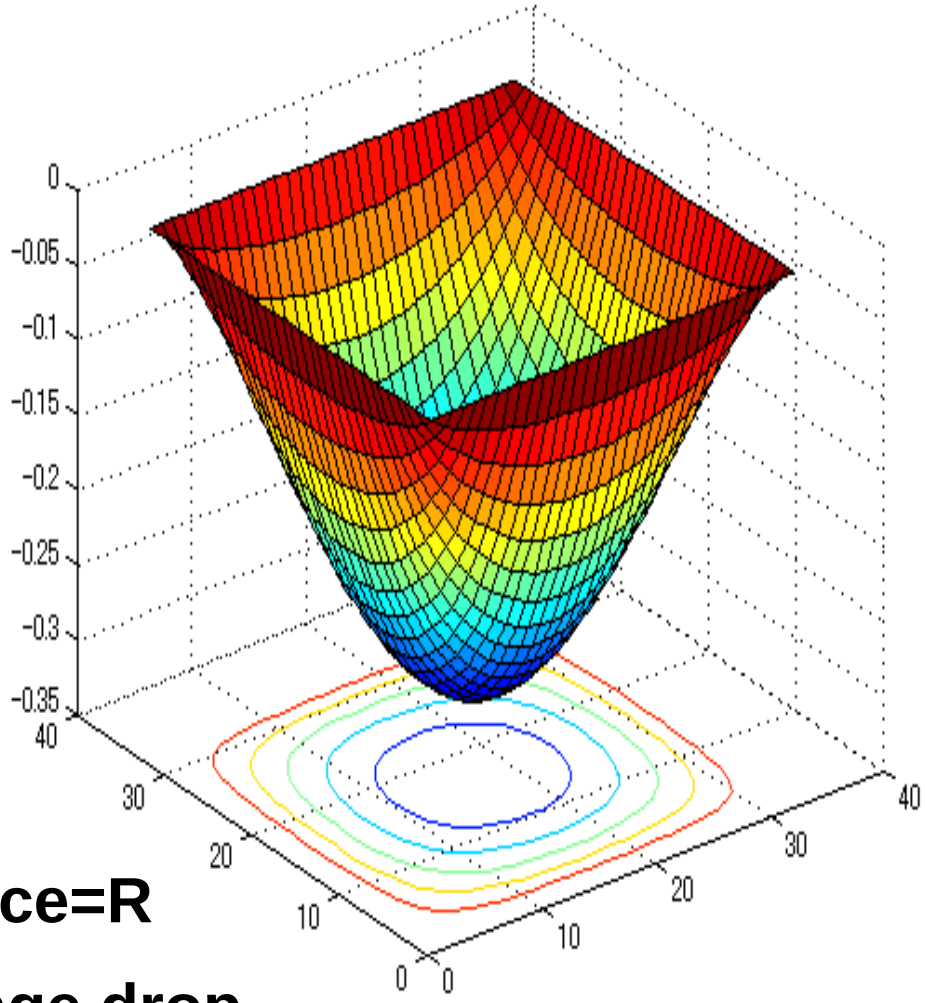


$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\,I_{i,j}$$

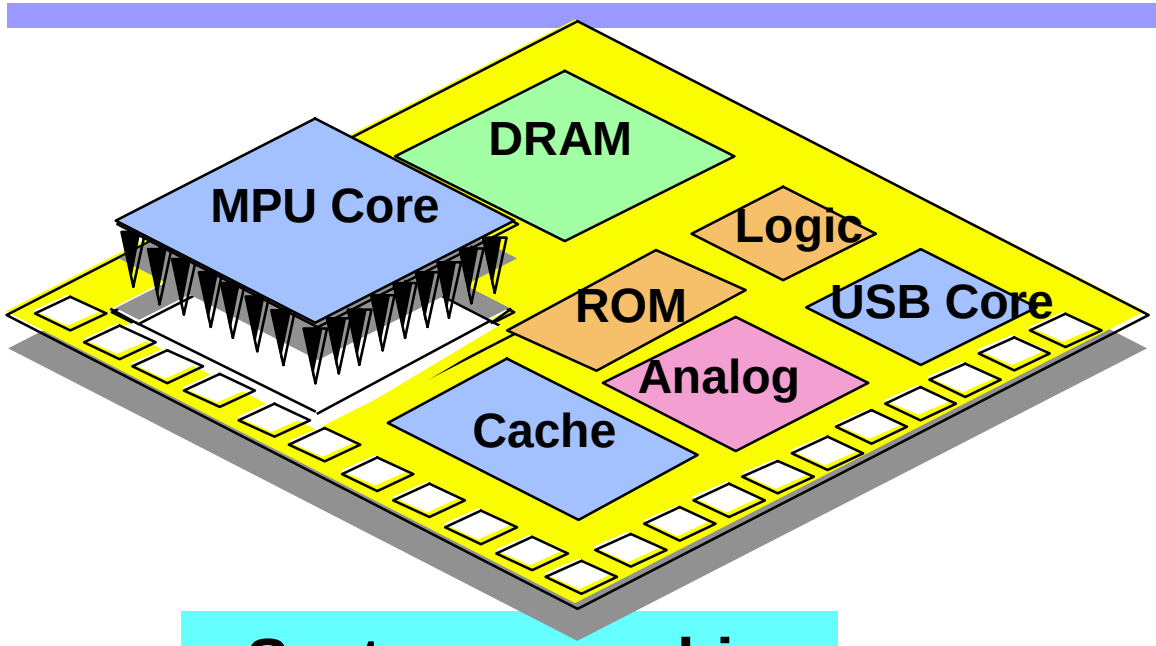


$\sum I_{i,j}=I$, Sheet resistance=R

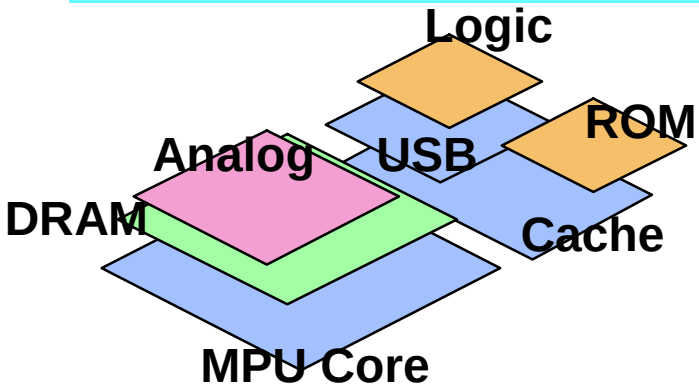
Take IR as unity voltage drop



3-Dimensional assembly



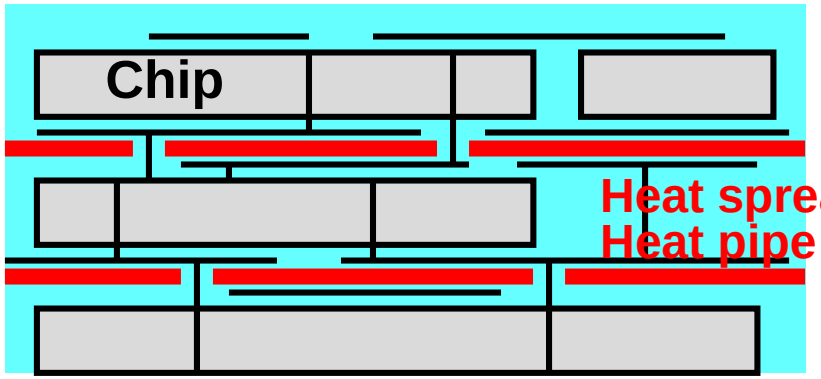
System on a chip



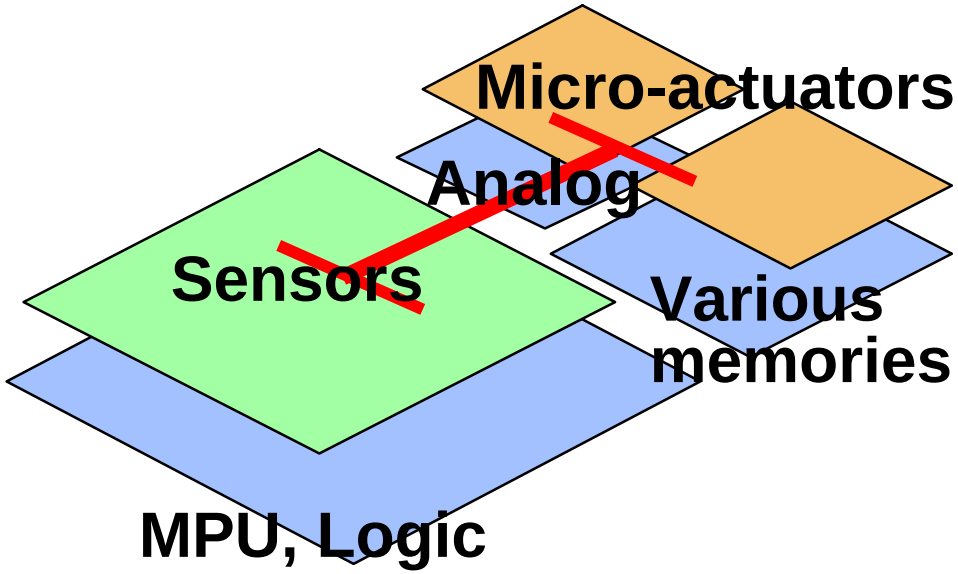
3-D assembly

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

- Heat dissipation is an issue



Possible electronic system in 2014

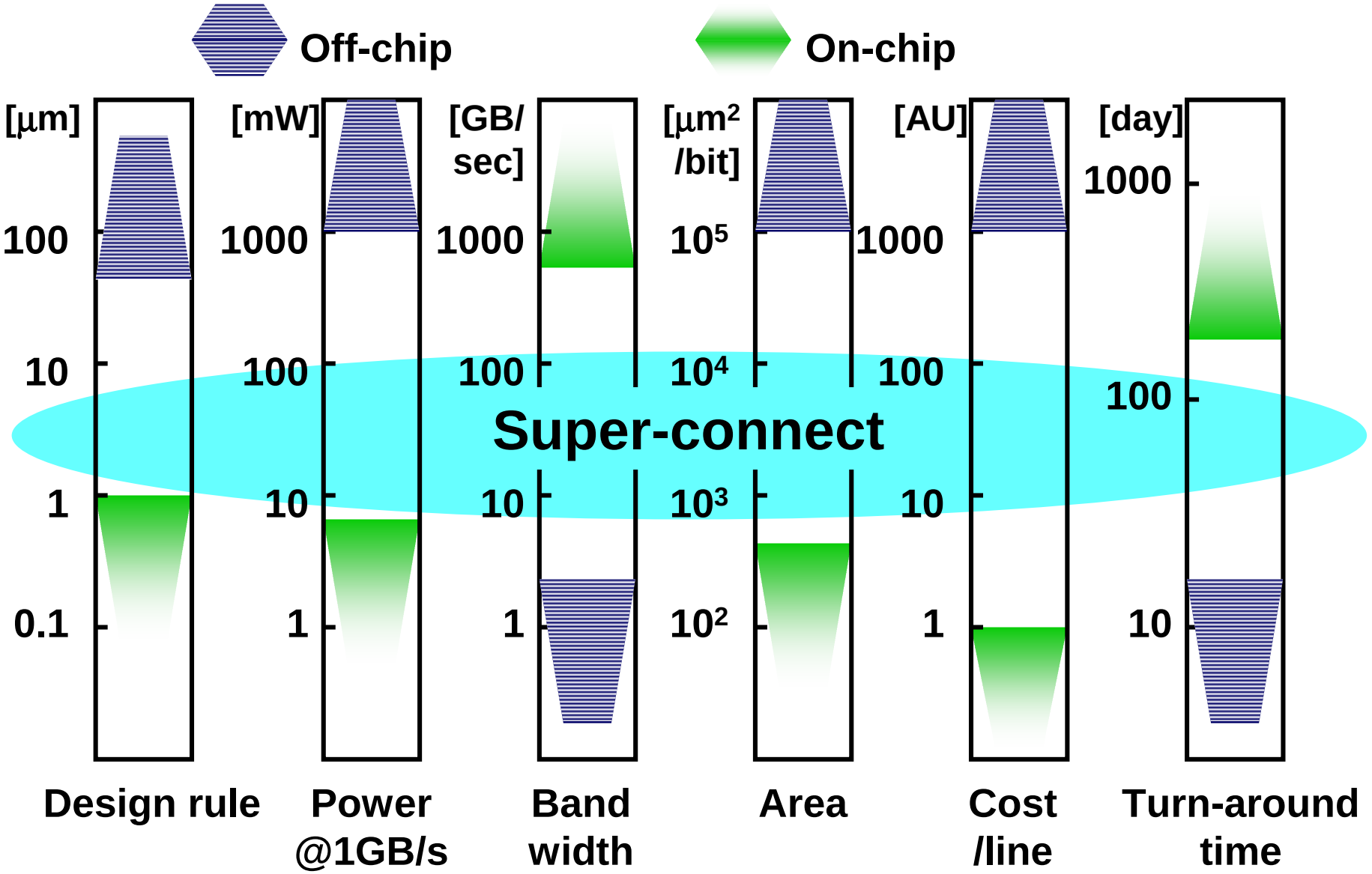


- Sensors/actutors
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)

Issues in System-on-Chip

- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

Super-connect

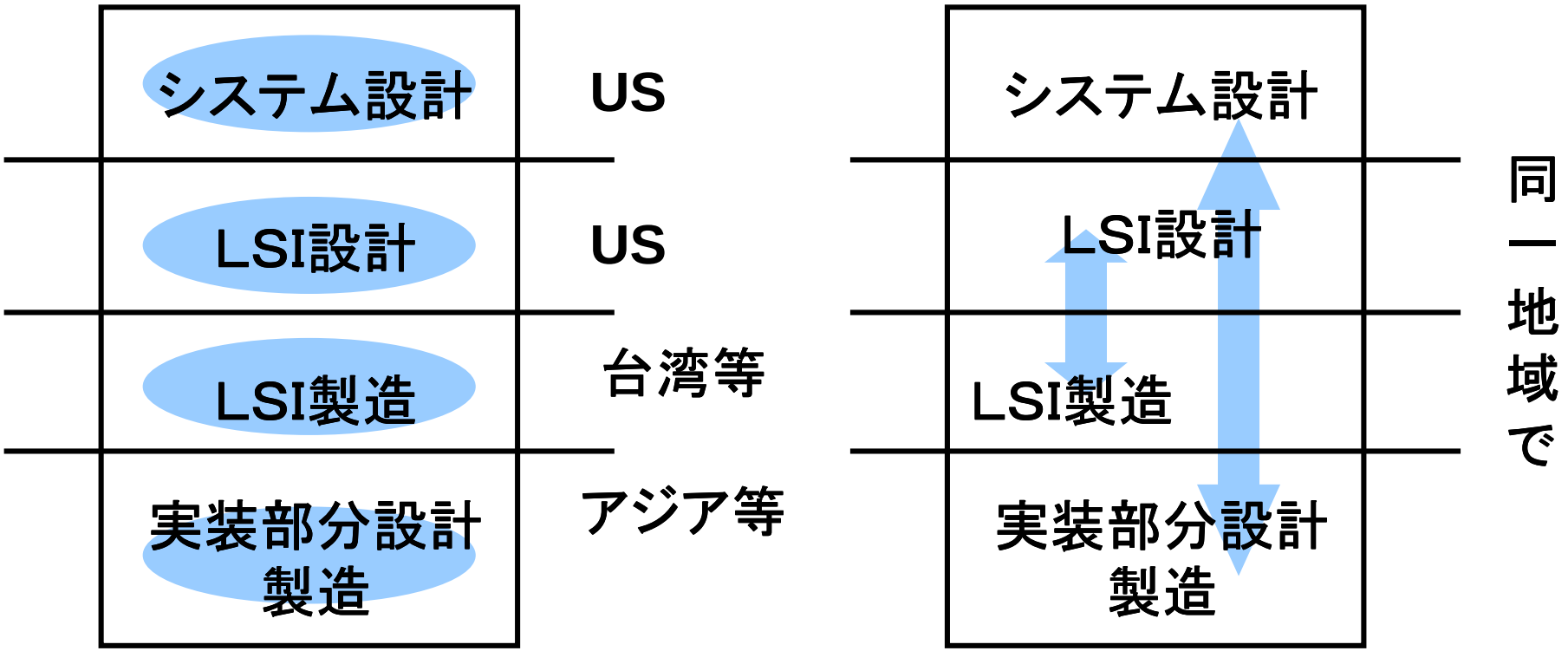


T.Sakurai

System-in-Packageの課題

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

水平分業と垂直統合



ASIC、デジタル、SoC

メモリ
アナログ
CPU

SoC

SiP

LSI配線とシグナルインテグリティ

1. 最も深刻な課題は何か？LSIプロセス/実装か、CADツール、設計手法か、設計者の意識の問題か？

2. 有効な手段はあるか？LSIプロセス/実装方法か、ロバストで手戻りの少ない設計手法はあるか？

- 近未来はカップリングや配線遅延　　設計手法、CAD
  Buffer挿入が有効

- 将来は電流問題（IRドロップや信頼性）　　プロセス/実装
  スーパーコネクト、SiP co-designなどが有効

LSI配線とシグナルインテグリティ

3．日本の産業界は正しく進んでいるか？新規問題の予防策として必要なCADツールを米国ベンダーに頼っている構図

- 同じツールを使っていてもCADベンダーとの密着度の違いが大きい（1Hr vs 3Mo）。日本語での電話一本でのサポート。
- 各設計チームは独特な問題（新規問題）と取り組んでいる。

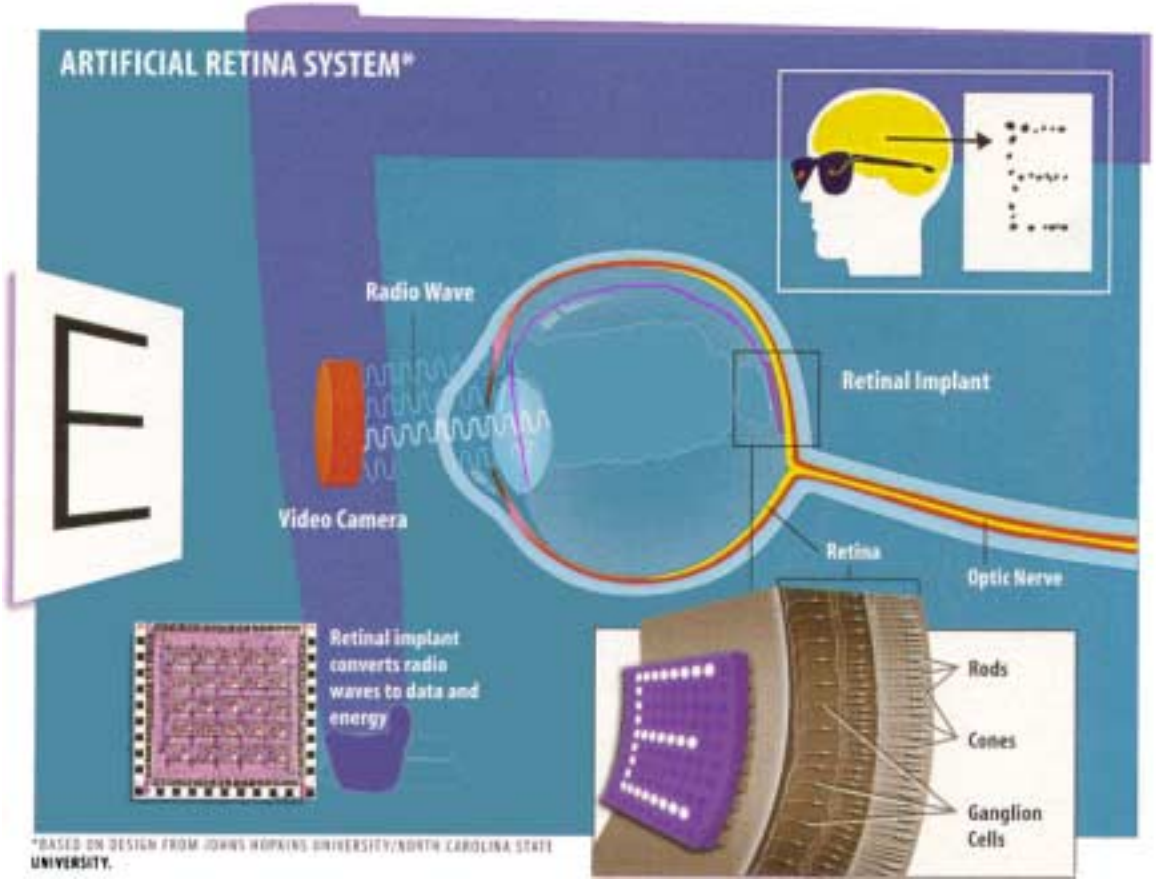
  Distributed CAD engineers

  設計者がscriptingによって対応できるように。

Prosthesis - Dual Intraocular Units

NC STATE UNIVERSITY

Retinal Prosthesis



Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html