第３１回　日経マイクロデバイス･セミナー　’00/4

LSIの新境地を切り開く「スーパーコネクト」技術

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LSIの新境地を切り開く「スーパーコネクト」技術

これから１０年のLSIの技術的課題を展望すると、配線系に多くの問題が集中していることに気付く。LSIの良し悪しを決める指標にはスピード、面積、消費電力、信頼性、ターンアラウンドタイムなどがある。従来はトランジスタがこれらの指標を決めてきた。しかし、ここにきて配線がこれらの指標を決めるというパラダイムシフトが起こっている。配線RC遅延の増大はLSIのスピードを律則し始めた。電源線の電流密度の増大は、信頼性の低下やIRドロップの増大といった問題を引き起こしている。配線の多層化によって製造期間は配線部で決まってくるようになった。

さて、このような問題を解決する上で従来のLSI上の配線だけでは限界が見えている。例えば電源線を考えてみよう。チップの消費電力は増大しており、電源電圧は低下している。International Technology Roadmap for Semiconductors によれば、2006年には160W、0.8Vといった電力と電源電圧値が出ている。すると、電源系は200Aの電流を運ぶ必要がある。チップの周辺にべったり電源パッドを配し、べた膜で配線できたとしても、中心部で5%の電圧降下しか許さないとすると0.5mΩ以下のシート抵抗が必要となる。これには銅配線を仮定しても、数十μｍ以上の膜厚が必要になってくる。このような厚膜配線は従来のLSI技術ではむずかしい。この例は極端だとしても、1μm～20μm程度の膜厚配線層が必要になるのは数年以内に起こると考えられる。

現在のところLSI上では１μｍ程度の配線膜厚が限度、一方プリント基板やパッケージなど実装側では数十μｍ以上というように、この中間部分の膜厚とデザインルールが欠落している。この辺の配線技術、すなわちスーパーコネクト技術が必要になってくる所以である。スーパーコネクトはLSI側と実装側双方の融合が図られる技術である。実装側もビルドアップ工法などLSIに近い製造法なども出てきて、LSIと実装との融合も取れやすい環境が整ってきている。マイクロパッドといった15μｍ角程度のパッド技術も実用化されている。

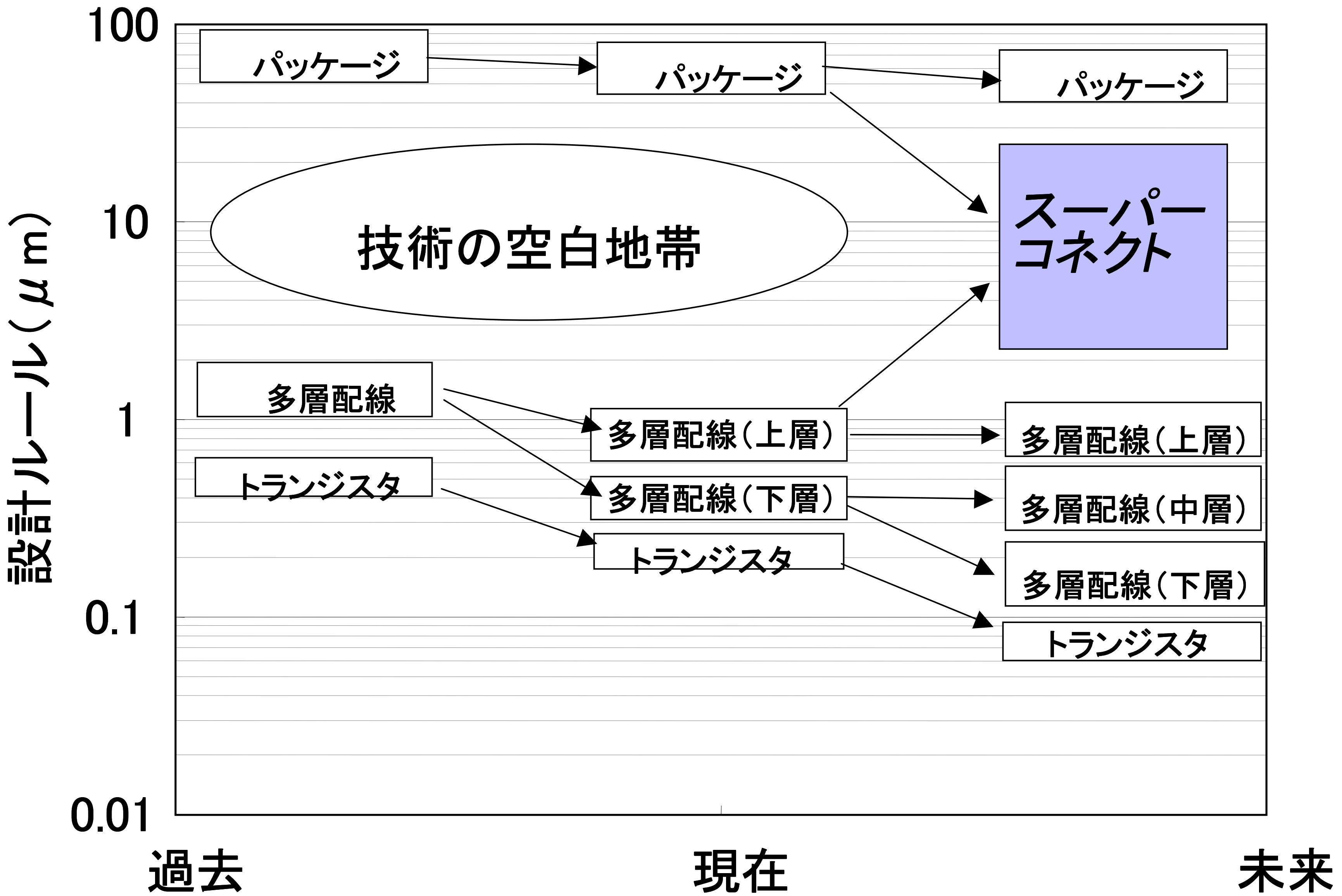
LSIの新境地を切り開く「スーパーコネクト」技術（続）

さて、このようなスーパーコネクトは配線遅延を軽減するにも役立つ。クロック系のスキューの低減は頭のいたい課題だが、低抵抗な配線層があればスキューを小さくできる。従って、クロックの基幹系をスーパーコネクトで行いたい。それにはLSI上の配線とスーパーコネクトを同時にシームレスに設計するコデザインが必要になってくる。

スーパーコネクトには、従来の配線問題の解決のみならず、新しい付加価値の創造という側面もある。プロセスの異なるチップを高いバンド幅で繋ぐ技術は、システムをワンチップで構成するよりバランスのとれたソリューションを提供する。チップを積層するスーパーコネクトでは、チップを平面に並べるマルチ・チップ・モジュールより全体の配線距離を小さくできるので、システムがより小型、高性能になる。熱の放散やインダクタンスの制御、特性インピーダンスの調整などにも利用できる可能性がある。LSI上の配線とスーパーコネクトを並列して製造できればターンアラウンドタイムの減少にも寄与する。

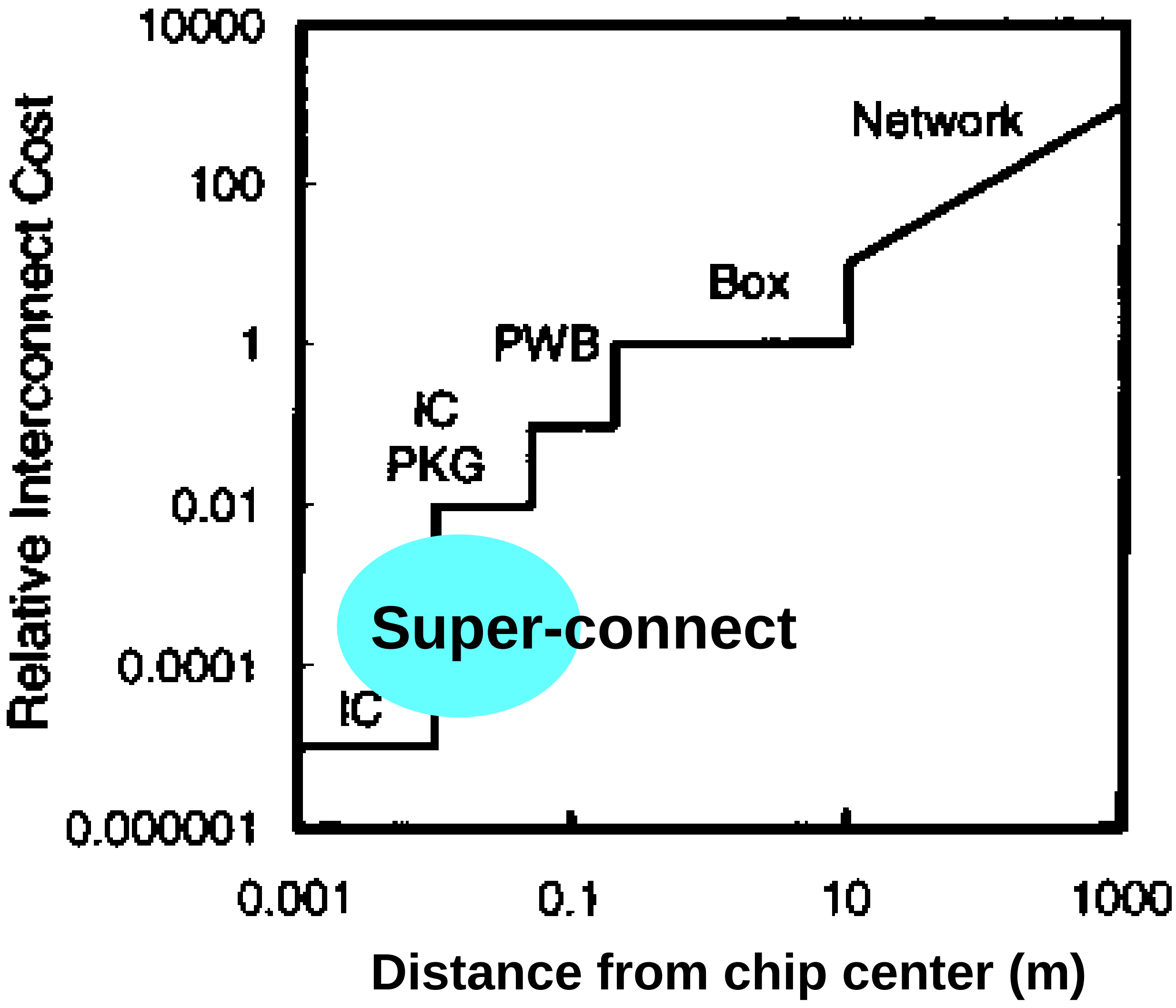
少し振りかえってみると、配線技術がLSIのビジネスモデルを変えた例に気づく。配線の多層化によって、LSIの製造ターンアラウンドタイムが配線系によって決まるようになってきた。こうなると、ゲートアレイがセルベースのASICに対して持っている製造時間の優位性が保てなくなった。これを反映して、面積や性能的に有利なセルベースビジネスに主流が移行してきた。このように配線技術はビジネスモデルにも影響を与える。スーパーコネクトによってこれからのビジネスモデルが変わる可能性も十分にある。

スーパーコネクト



出典：日経マイクロデバイス

Cost of interconnect



M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

スーパーコネクト

目的	手段	具体策（LSI側）	具体策（実装側）
高速化	配線長の短縮	多層化→逆スケーリング	3次元積層
	RC遅延の削減	Cu＋low-k	low-k
	L遅延の考慮	今後インダクタンス考慮	既にインダクタンス考慮
	リピータ	リピータ内蔵配線	3次元積層
	IRドロップ	厚膜配線、幅広配線	厚膜配線、幅広配線
	ゲート遅延の削減	トランジスタの微細化	ーーーーーー
低消費電力化	配線部の電力削減	Cu＋low-k	ーーーーーー
	配線長の短縮	多層化	3次元積層
	トランジスタの低電力化	微細化，SOI，・・・	ーーーーーー

スーパーコネクト
LSI側と実装側が共通の技術へ
従来の枠組みが変わる

出典：日経マイクロデバイス

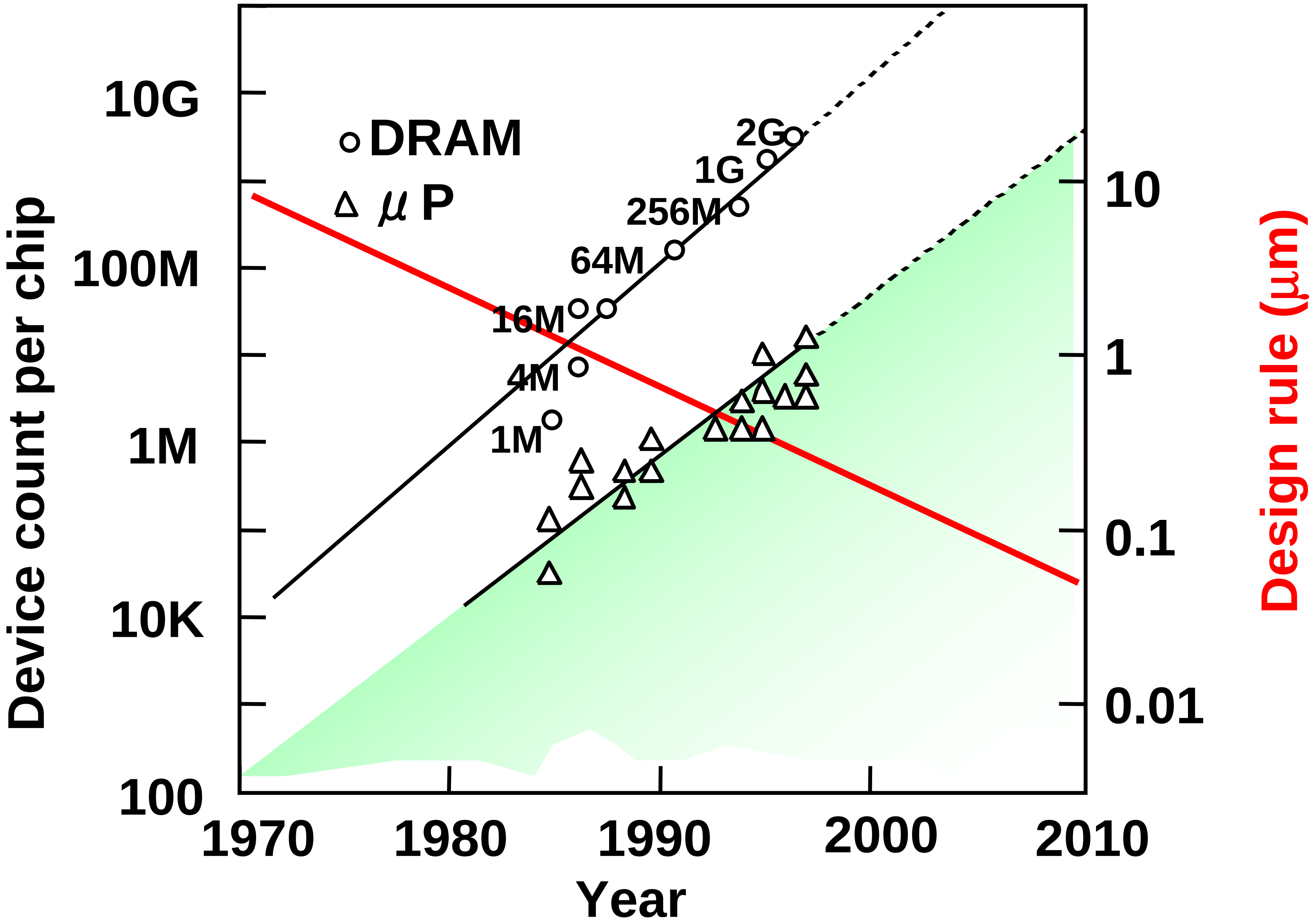
スーパーコネクト

目的	手段	具体策（LSI側）	具体策（実装側）
高信頼性化	マイグレーション対策	Cu，Cu＋Mg	――――――
	放熱対策	サーマル・ビア	サーマル・ビア
	接続信頼性の向上	――――――	各種バンプ/バンプレス接合
小型化	チップの小型化	微細化	――――――
	パッケージの小型化	――――――	チップ・サイズ実装
		――――――	3次元積層
		――――――	マイクロパッド
多機能化	複数機能の混載	高集積化，システムLSI	微小MCM
		3次元LSI	3次元積層
	受動素子の混載	オン・チップ・インダクタ	RLC内蔵プリント基板
		オン・チップ・アンテナ	超小型アンテナ

スーパーコネクト
LSI側と実装側が共通の技術へ
従来の枠組みが変わる

出典：日経マイクロデバイス

Moore's Law

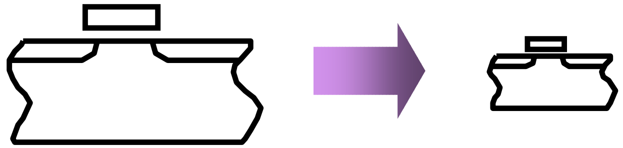


T.Sakurai

Scaling Law

Transistor		Numbers are exponent to k (k^n)
Voltage	[V]	-1
Tr. size	[x]	-1
Oxide thickness	[t]	-1
Current	[$I \sim V^{1.3}/t$]	- 0.3
Tr. capacitance	[$C_g \sim x^2/t$]	-1
Tr. delay	[$T_g \sim C_g V/I$]	-1.7
Tr. power	**[$P_g \sim C_g V^2/T_g$]**	-1.3
Tr. power density	**[$p \sim P_g/x^2$]**	0.7
Tr. desity	**[$n \sim 1/x^2$]**	2

Interconnection		Local	Middle	Global	VDD/VSS
Length	[L]	-1	- 0.5	0	0
Width	[W]	-1	- 0.5	0	1
Thickness	[T]	-1	- 0.5	0	1
Height	[H]	-1	- 0.5	0	0
Resistance	[$R_m \sim L/W/T$]	1	0.5	0	-1
Capacitance	[$C_m \sim LW/H$]	-1	- 0.5	0	1
RC Delay/Tr. delay	**[$T_m \sim R_m C_m/T_g$]**	1.7	1.7	1.7	–
Current density	**[$J \sim pLW/V/W/T$]**	–	–	–	0.7
Dc Noise	**[$SN_{dc} \sim JWLR_m/V$]**	–	–	–	1.7

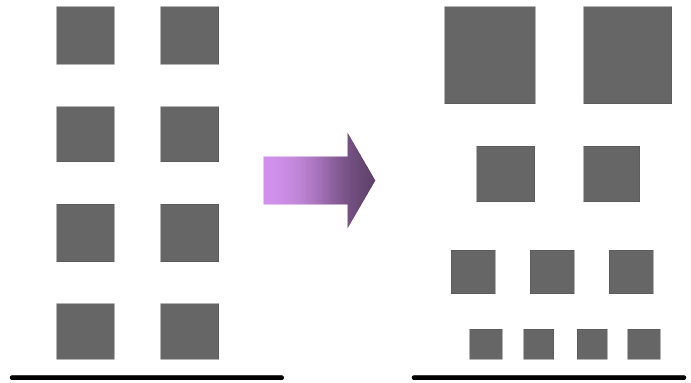


K=2

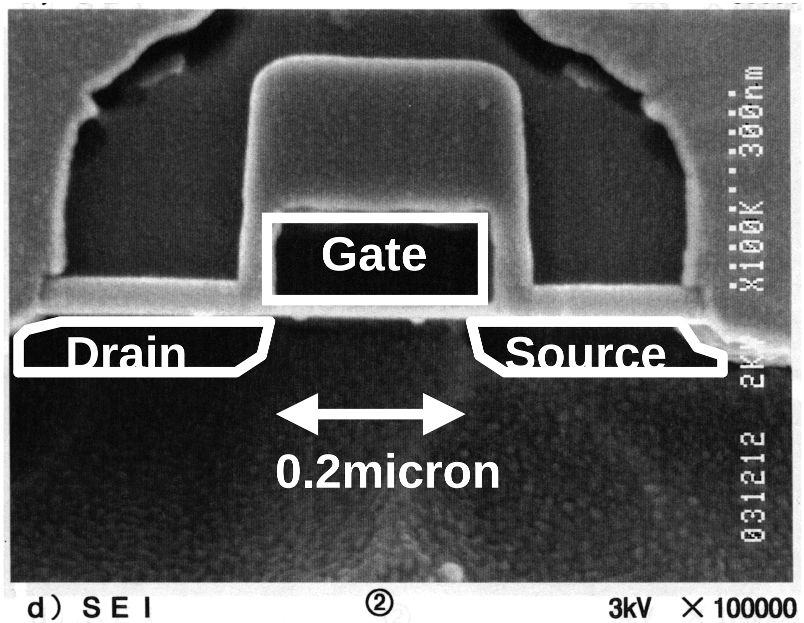
$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)\left(\frac{V_{gs}-V_t}{2}\right)^{\alpha} \sim [V^{\alpha}/t]$$

$\alpha = 1.3$

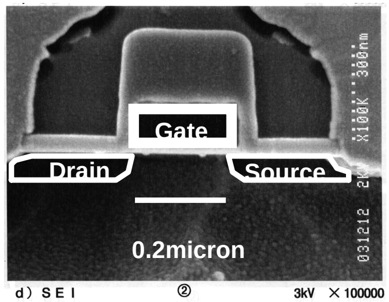
T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no,2, pp.584-594, Apr. 1990.



Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

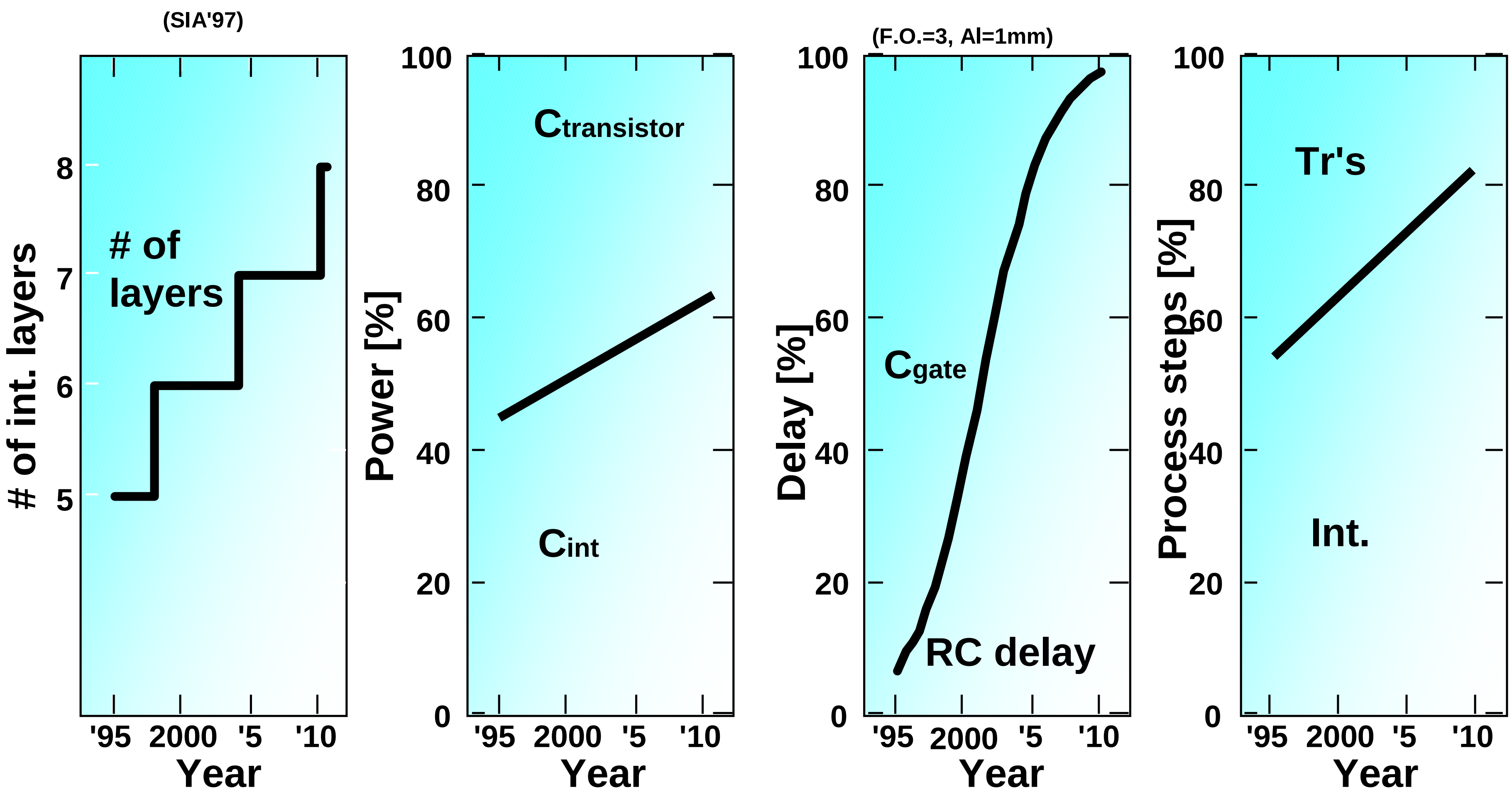
T.Sakurai

Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



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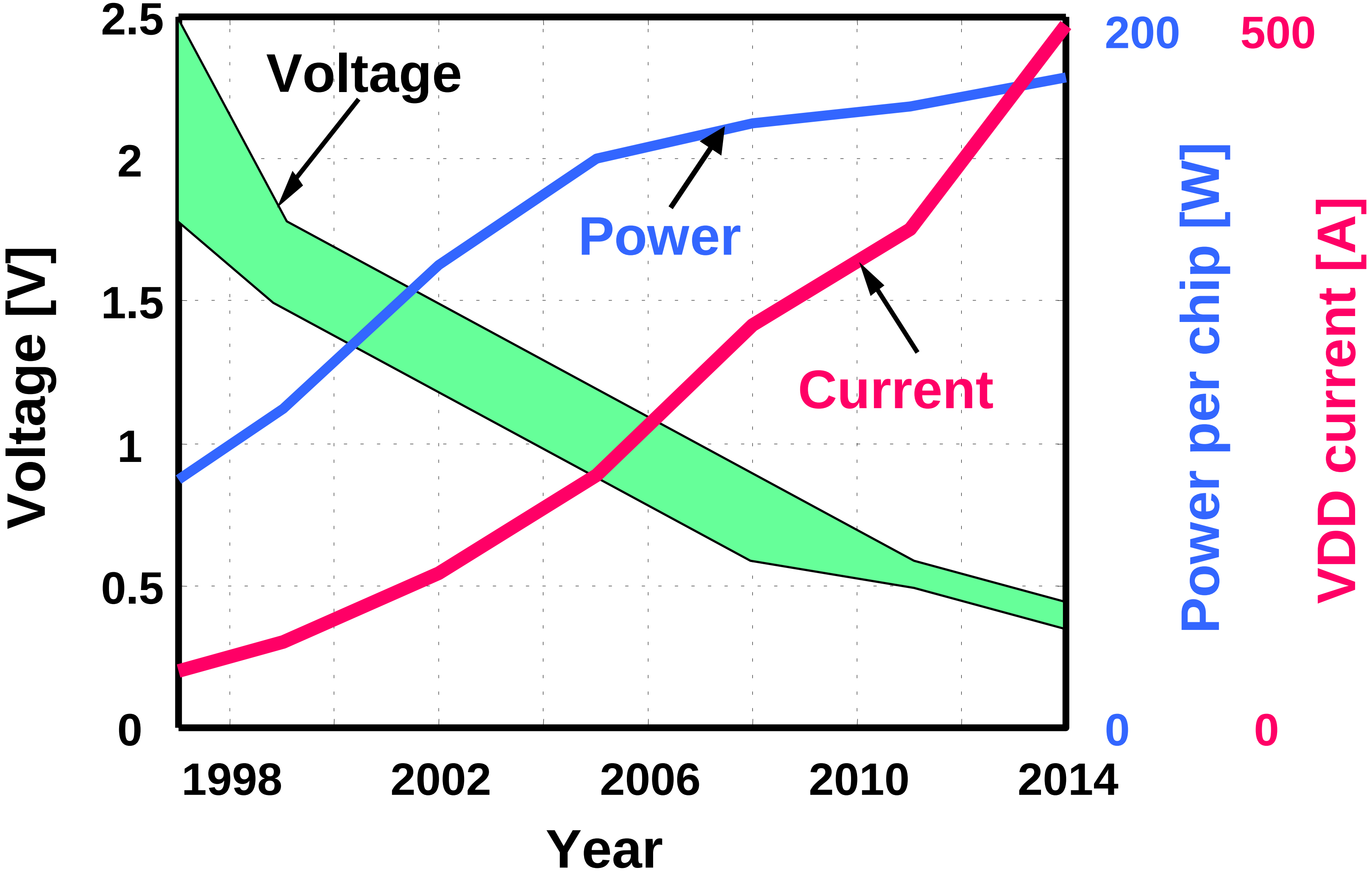
VDD, Power and Current Trend



International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA), Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

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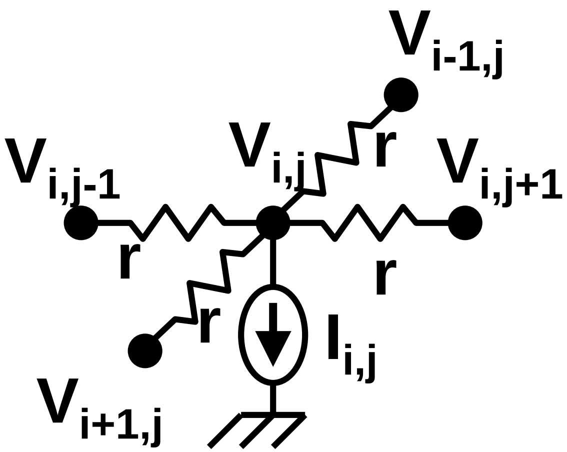
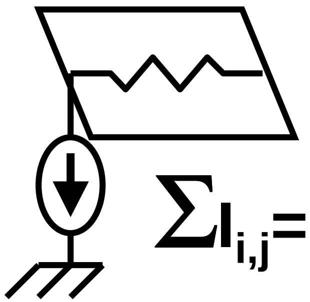
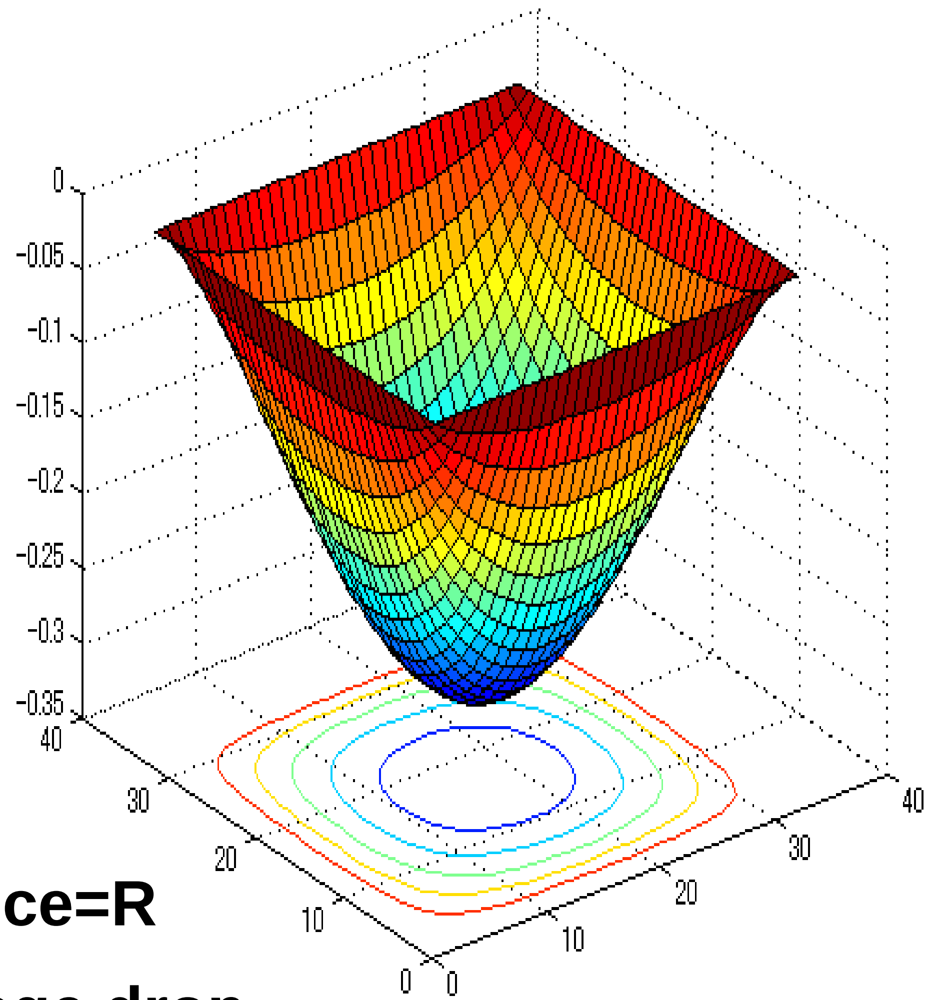
IR Drop



$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\ I_{i,j}$$

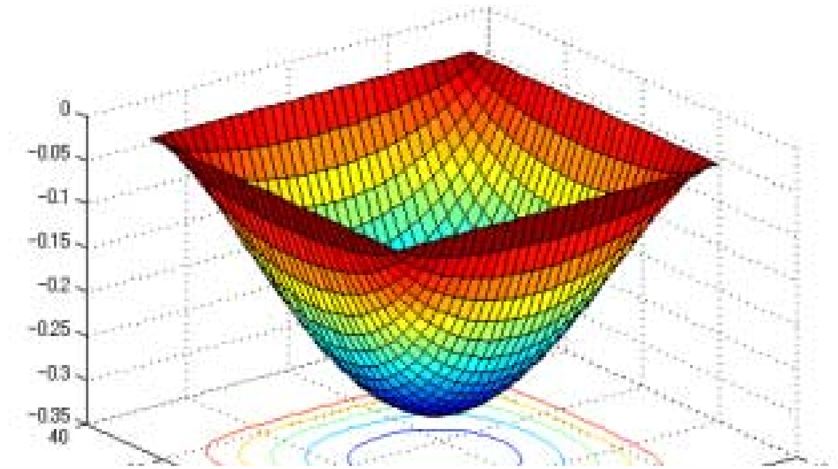


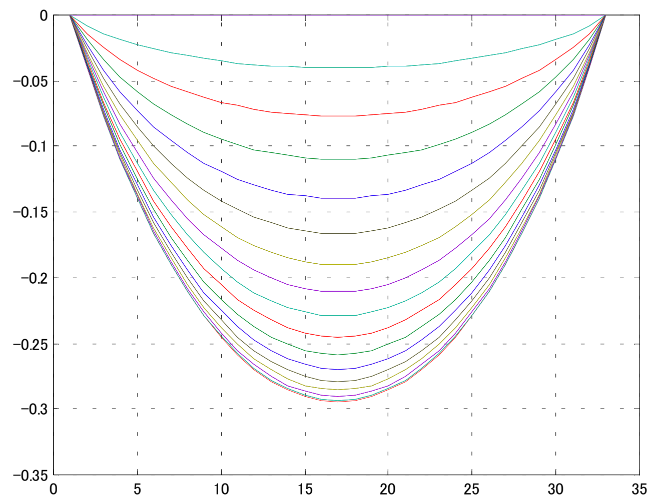


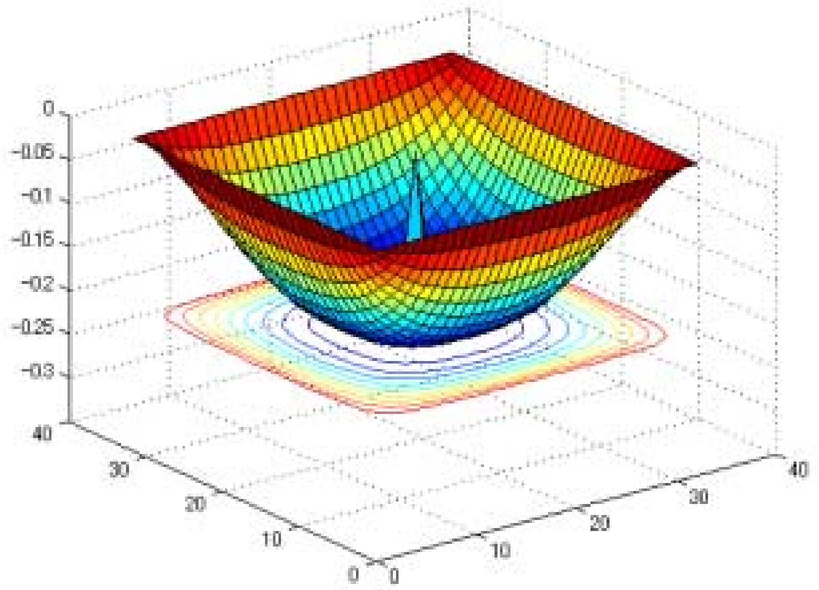
$\Sigma I_{i,j}=I$, Sheet resistance=R

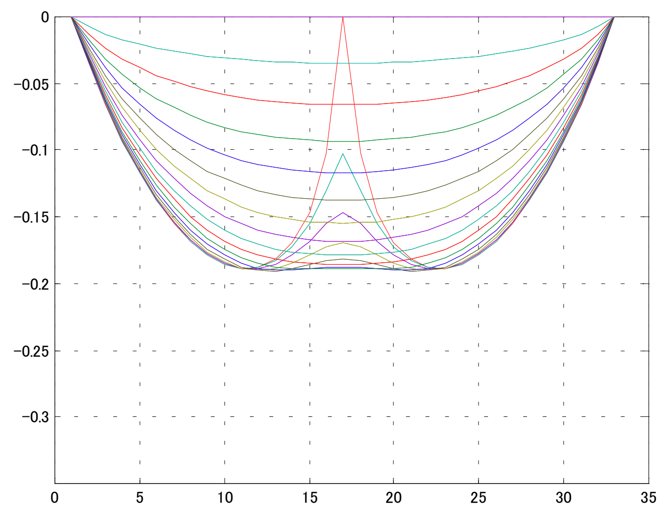
Take IR as unity voltage drop

IR Drop


0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
-0.35
40


0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
-0.35
0
5
10
15
20
25
30
35

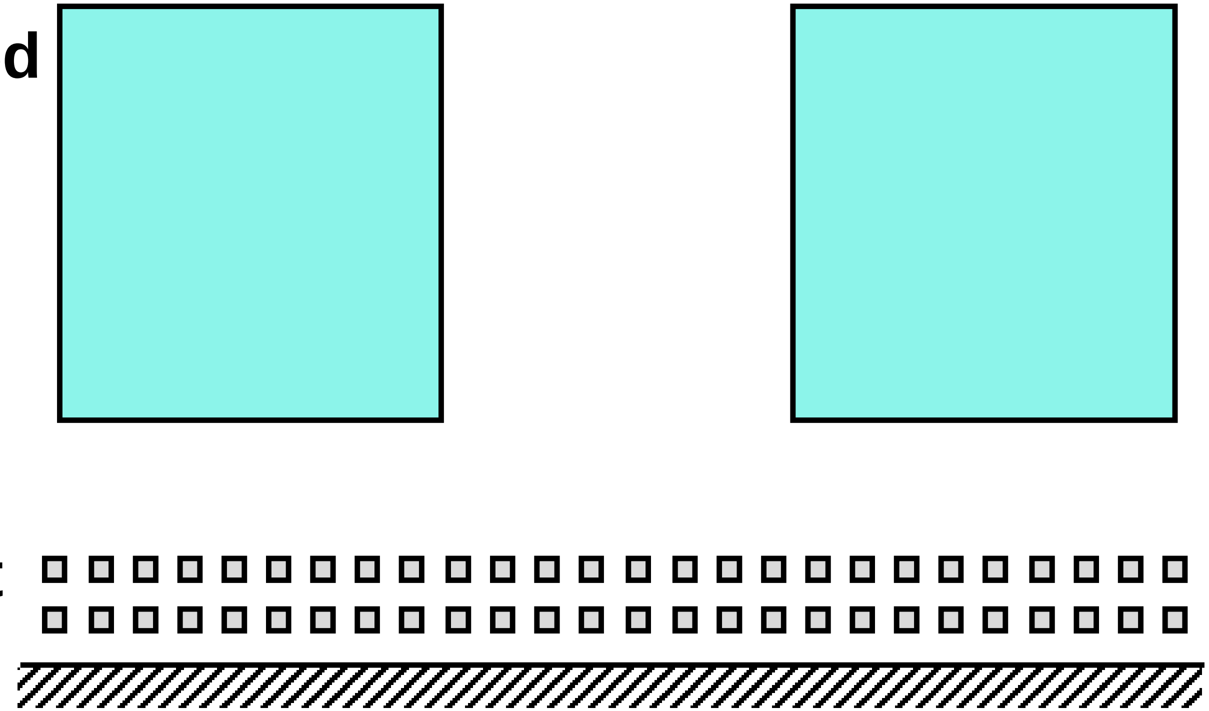

0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
40
30
20
10
0
0
10
20
30
40


0
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
0
5
10
15
20
25
30
35

Interconnect Cross-Section and Noise

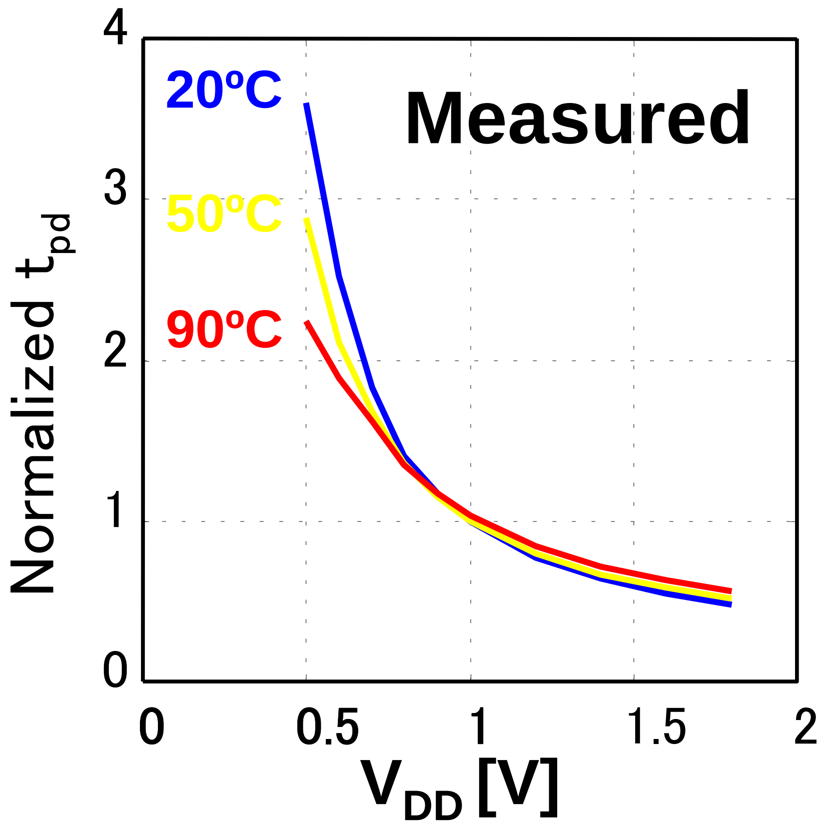
Unscaled / anti-scaled
- **Clock**
- **Long bus**
- **Power supply**

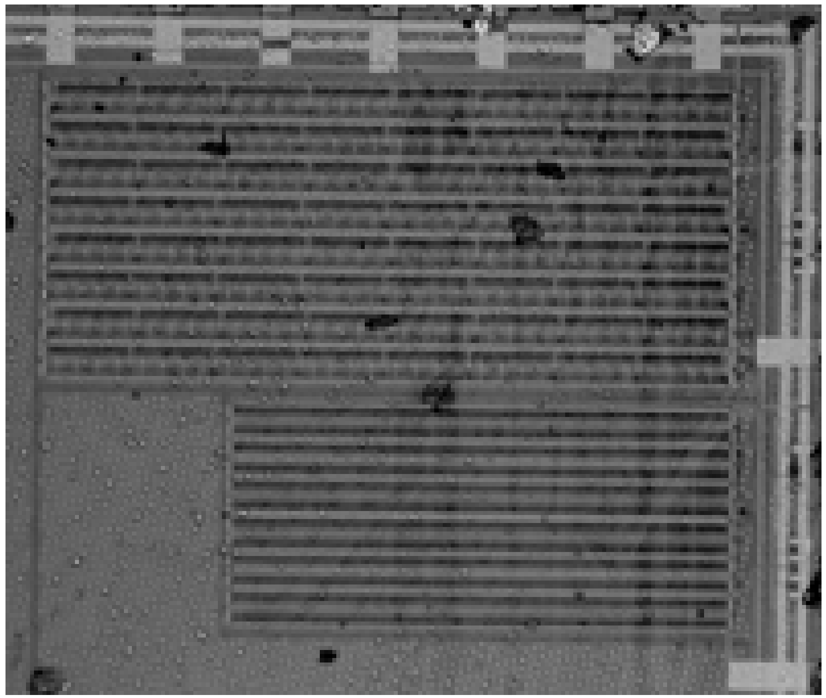
Scaled interconnect
- **Signal**



1V 20W -> 20A current
2% noise on VDD & VSS -> ~0.02V / 20A -> ~10µm thick Cu
Thick layer on LSI, area pad, package are co-designed.

Measurement of 32bit full adder

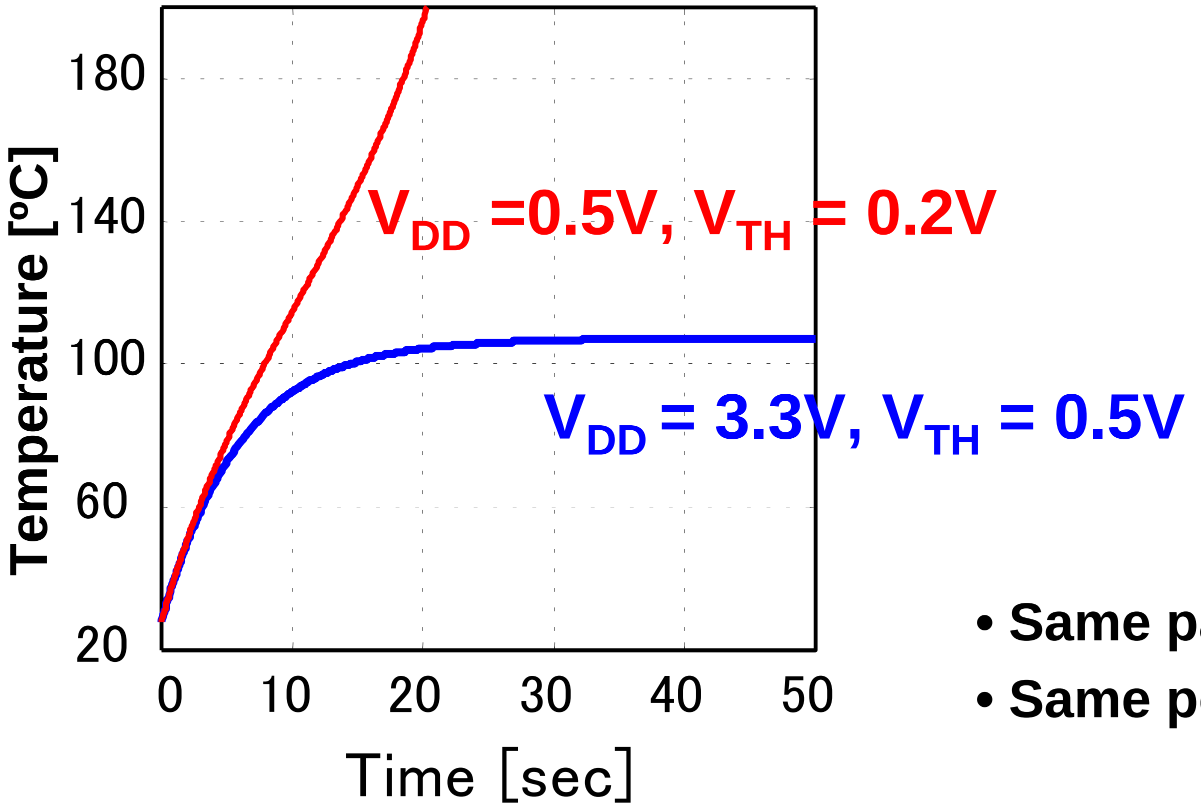




Photograph of 32bit FA

0.3μm CMOS

Transient response of chip temperature

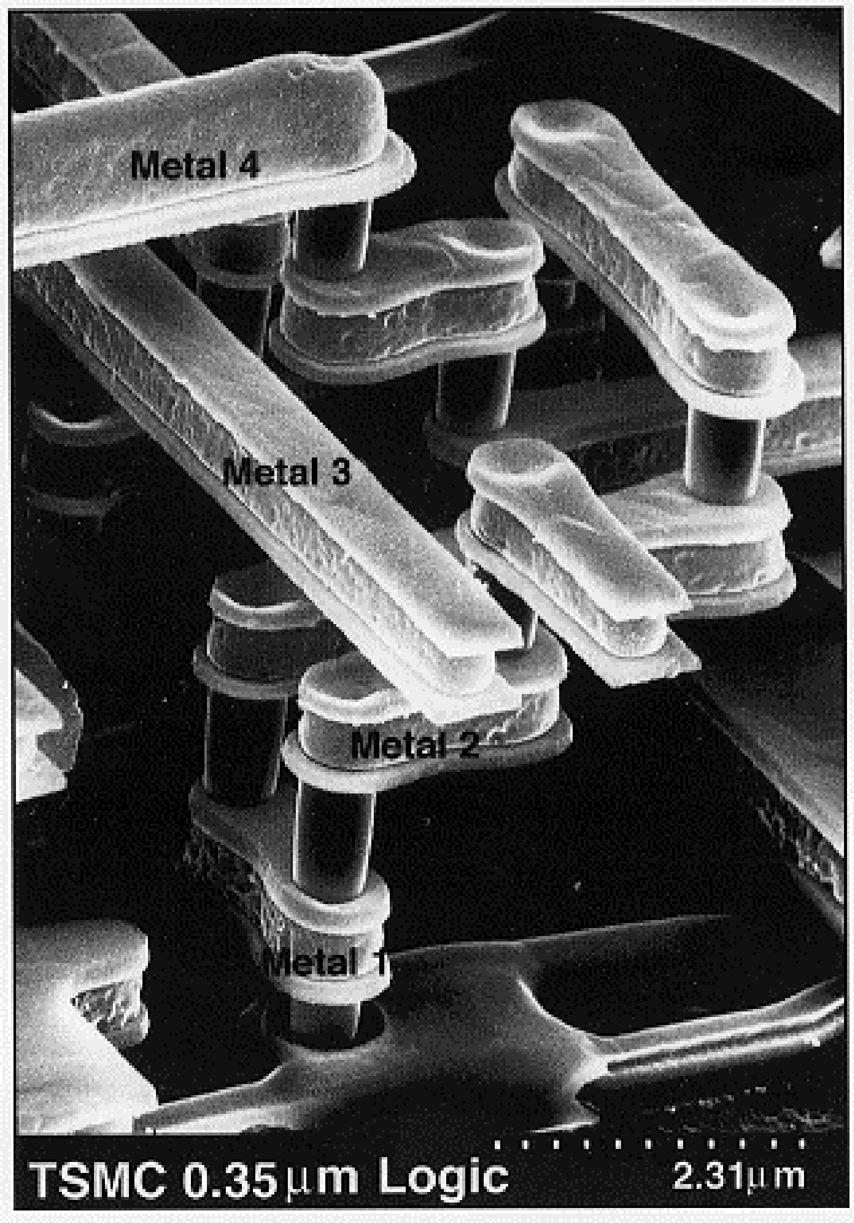


- Same package
- Same power at room temp.

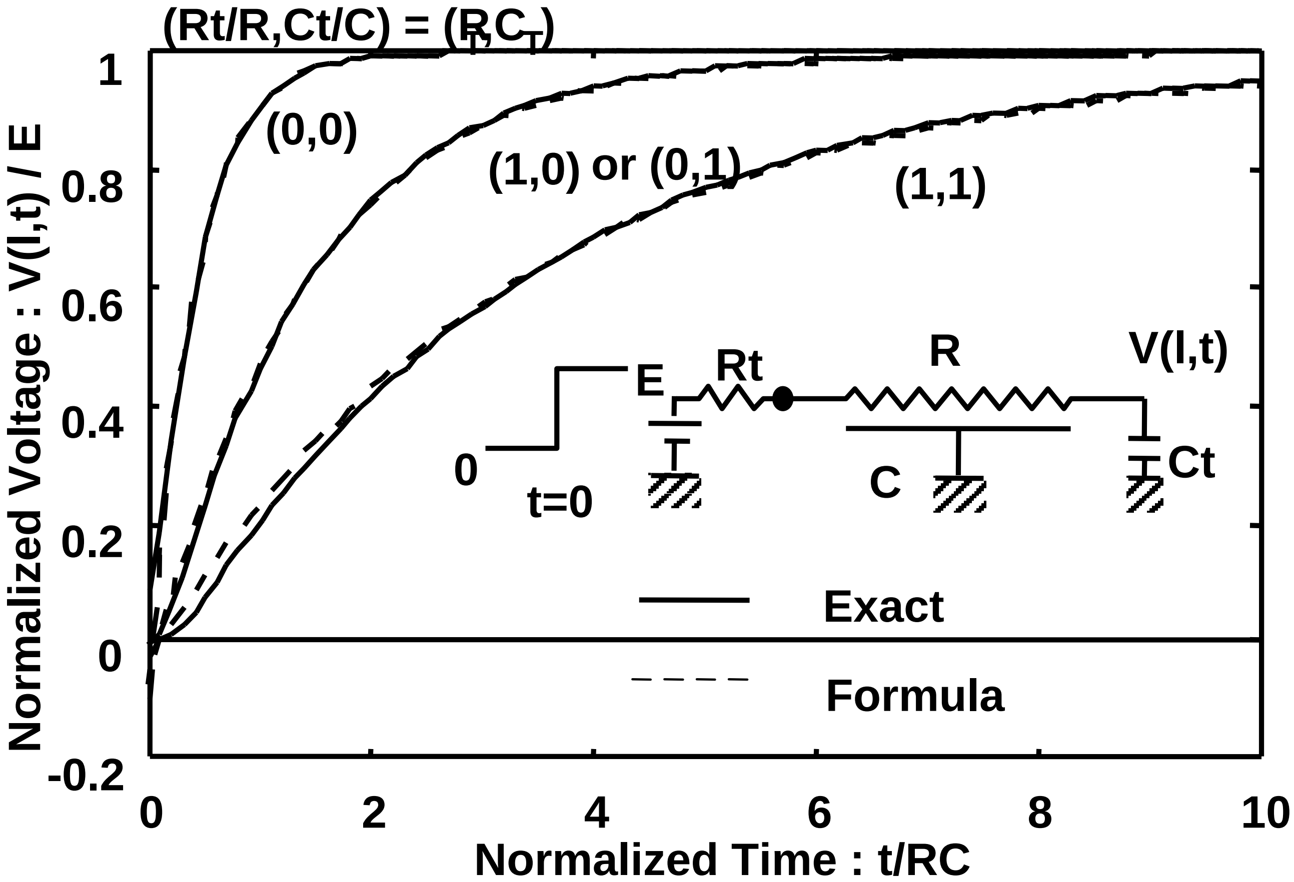
Better package is needed to avoid thermal runaway in low voltage.

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

Complex interconnect



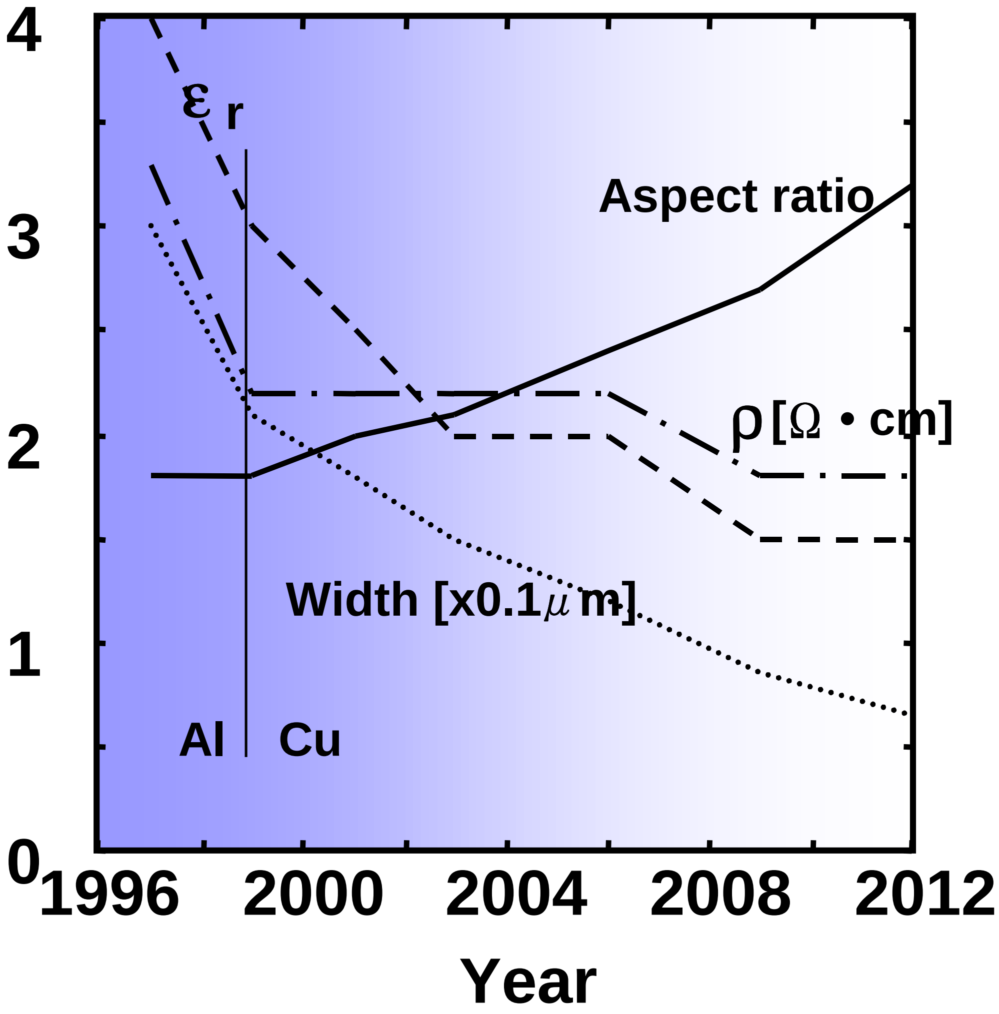
Voltage waveforms of a distributed RC line



$$\frac{V(l,t)}{E} \approx 1 - \exp\left(- \frac{t/RC - 0.1}{R_T C_T + R_T + C_T + 0.4} \right)$$

T.Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling and Crosstalk in VLSI's," IEEE Trans. on ED, Vol.40, No.1, pp.118-124, Jan.1993.

Interconnect parameters trend



Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

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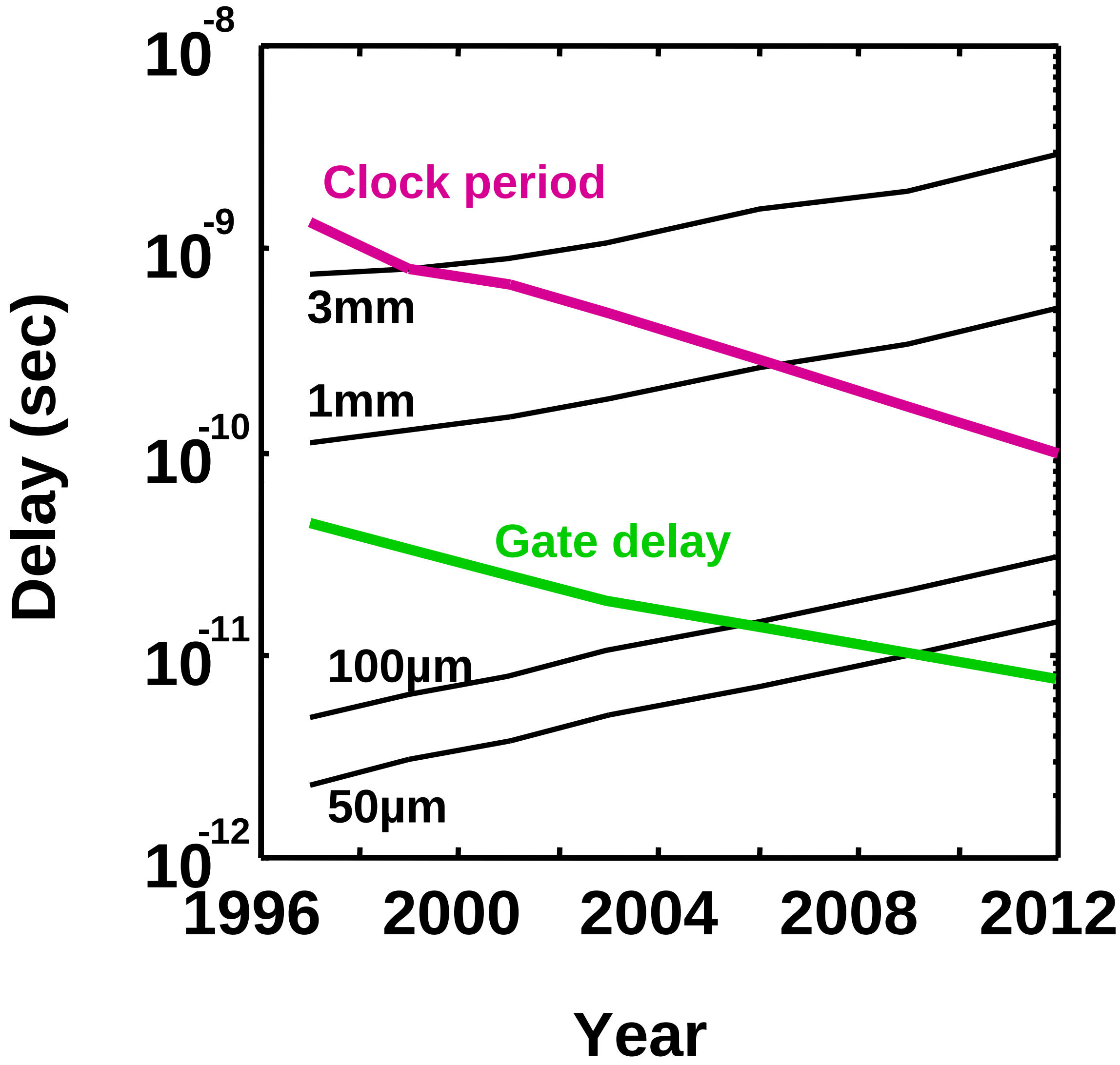
RC delay and gate delay



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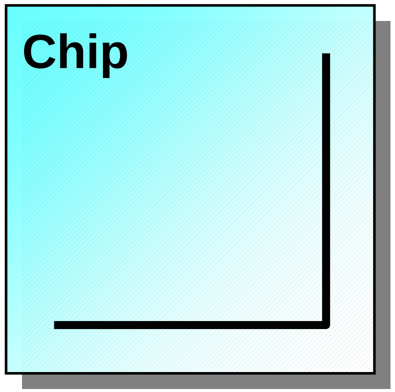
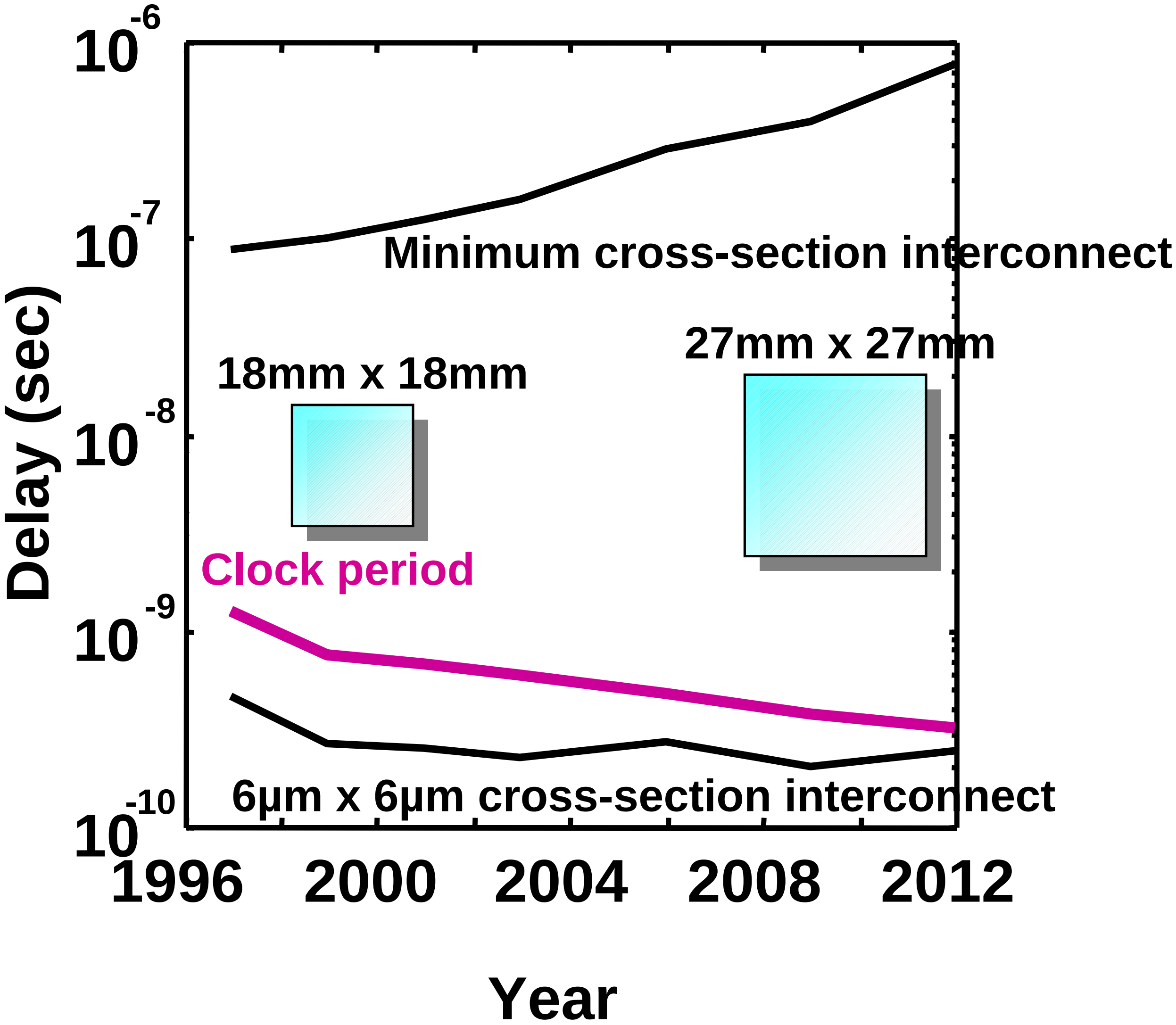
RC delay of global interconnections



Global interconnect



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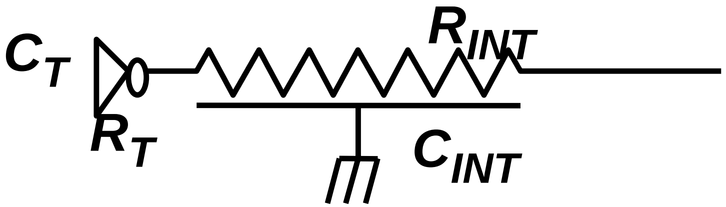
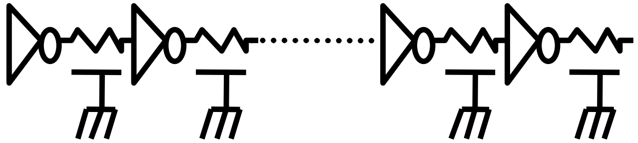
Repeaters



a) Without repeaters



b) With repeaters

$$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693 (R_T C_T + R_T C_{INT} + R_{INT} C_T)$$

C_0 : *Gate capacitance of minimum MOSFET*

R_0 : *Gate effective resistance of minimum MOSFET*

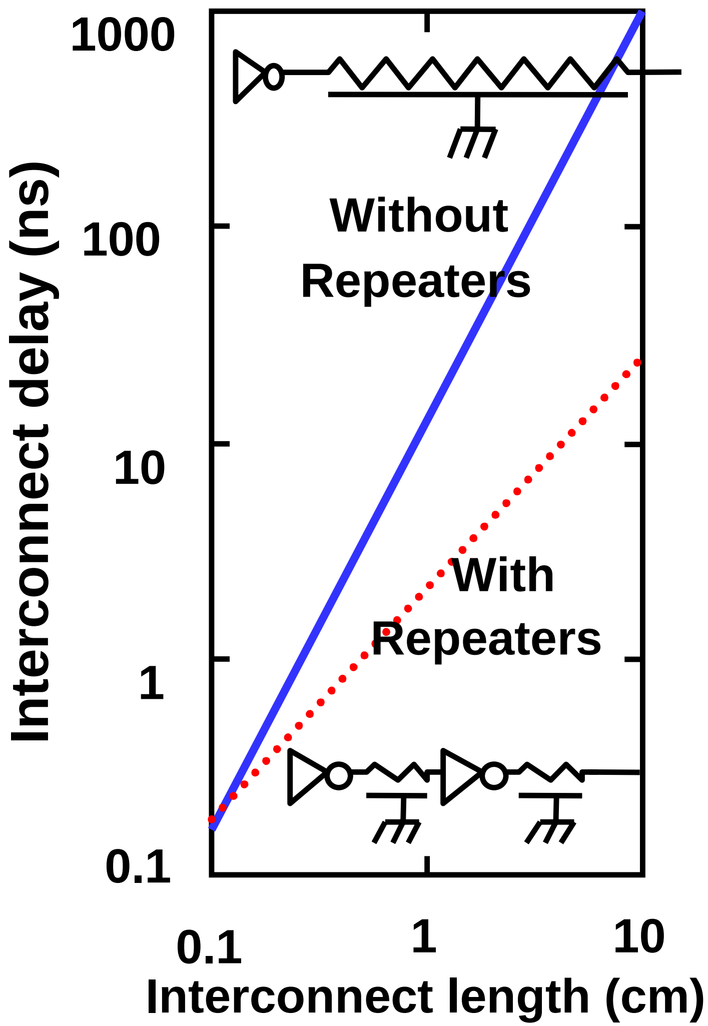
$$Delay \approx k\left[p_1 \frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h} hC_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k} hC_0\right)\right] : Buffered$$

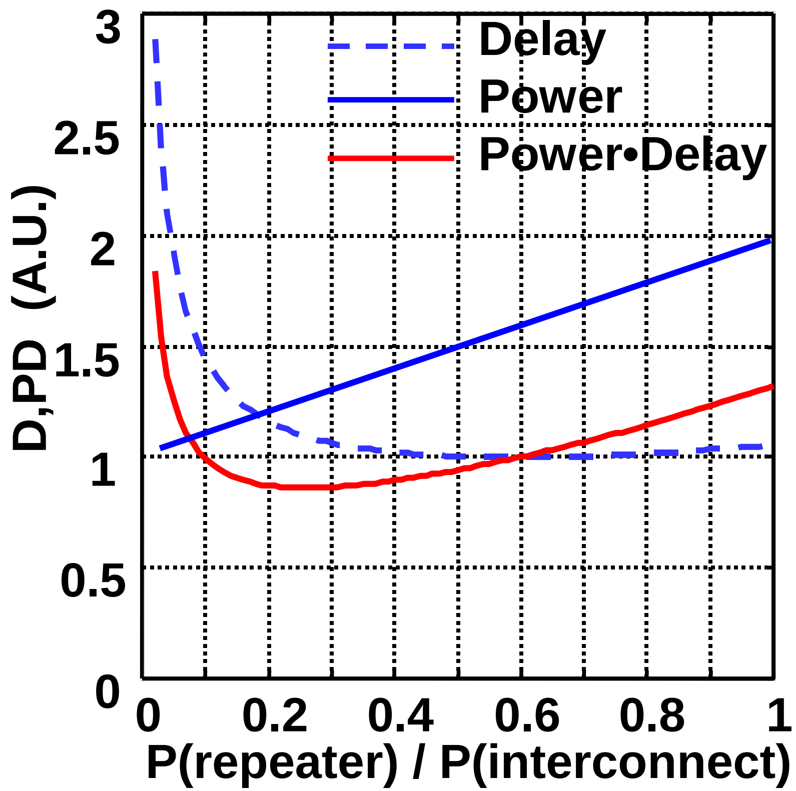
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT} R_0}{R_{INT} C_0}} : Optimized\ size\ of\ buffer\ inverter$$

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}}\sqrt{\frac{R_{INT} C_{INT}}{R_0 C_0}} : Optimized\ number\ of\ stages$$

$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right)\sqrt{R_{INT} C_{INT} R_0 C_0} \approx 2.4\sqrt{\tau_{INT}\tau_{MOS}}$$

Delay and Power Optimization for Repeaters





Delay optimized

→P: P(repeater)=0.60 P(interconnect)

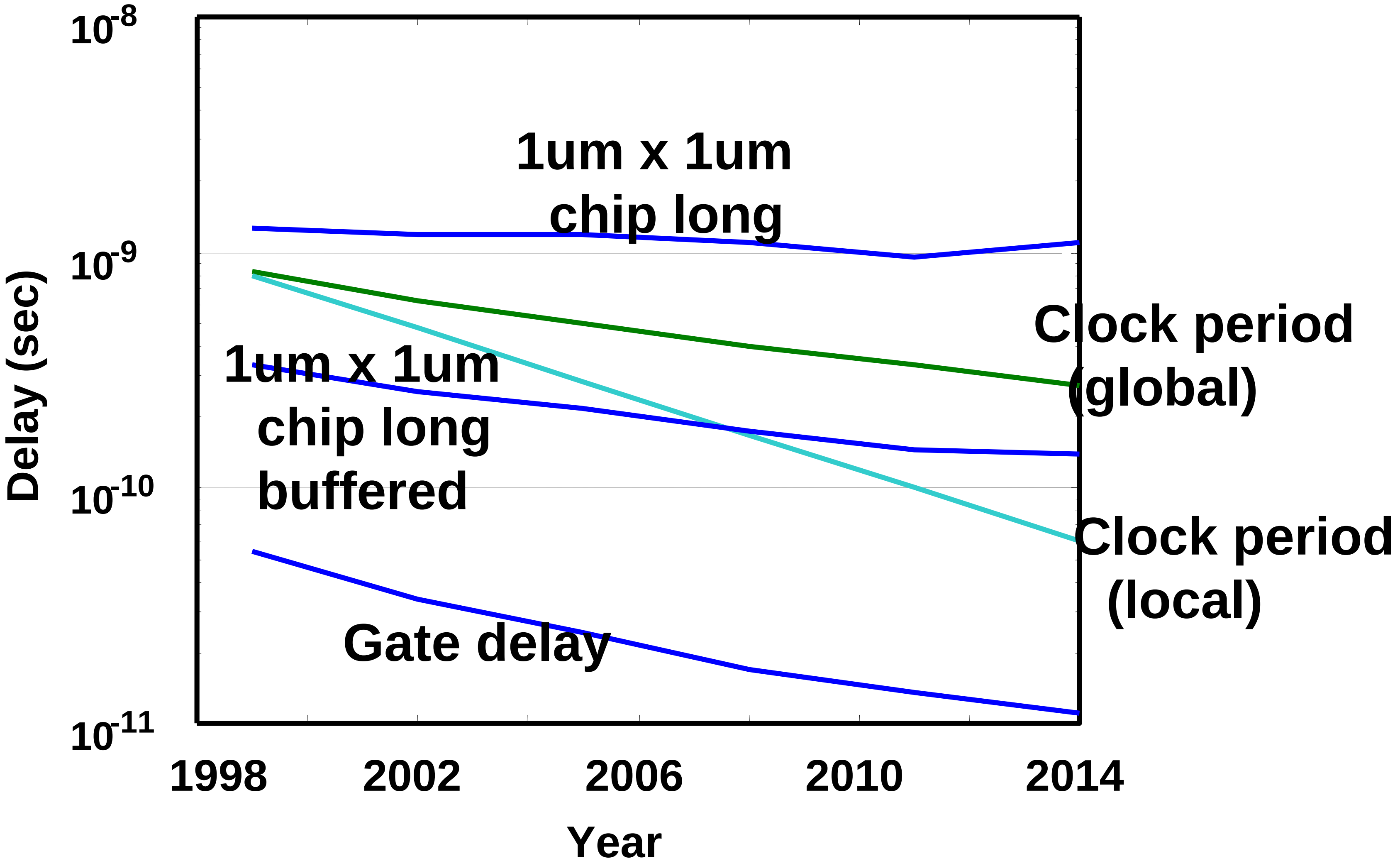
Power•Delay optimized

→D: 1.09 Dopt

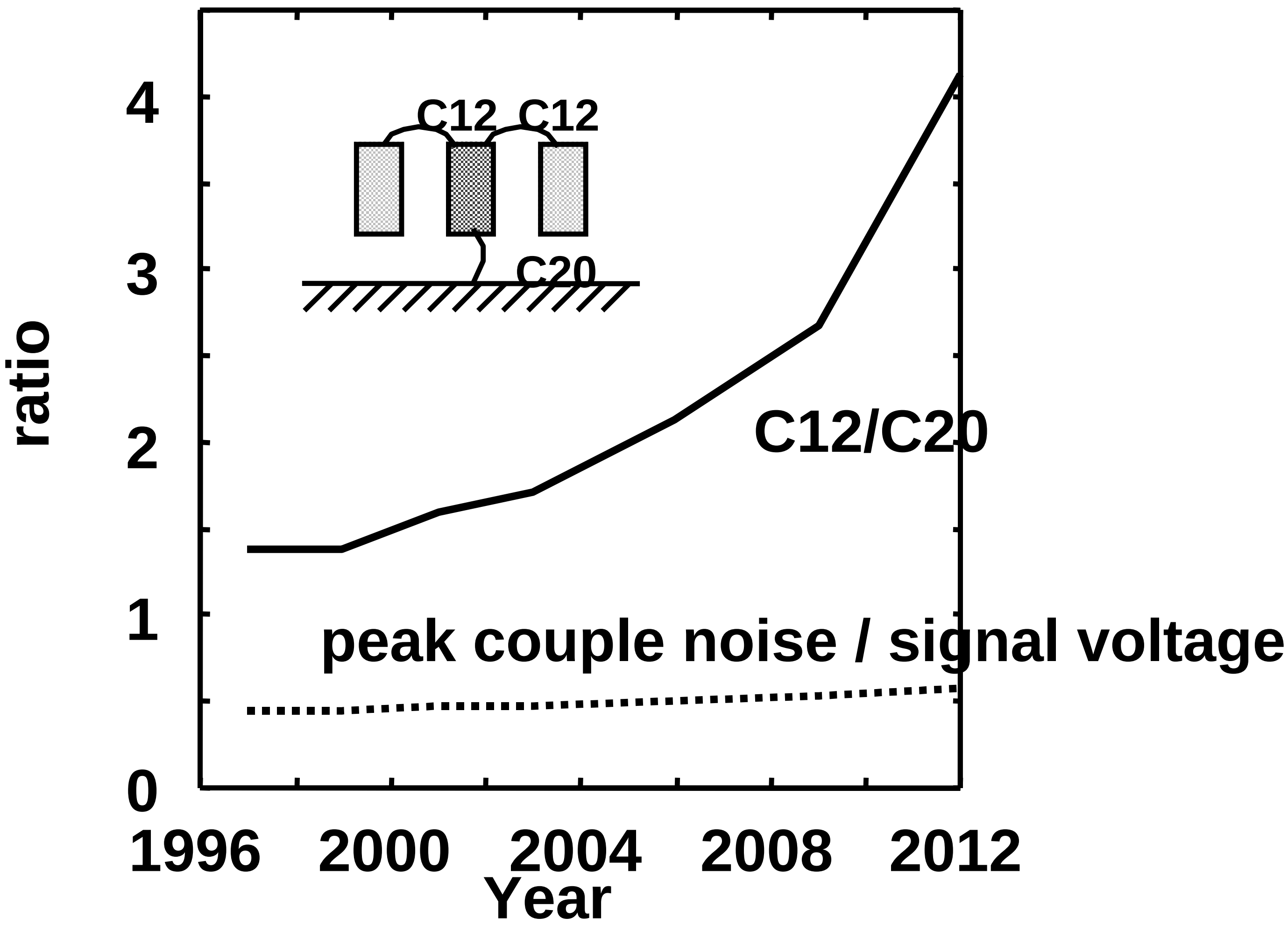
→P: P(repeater)=0.26 P(interconnect)

→PD: 0.86 of Dopt case

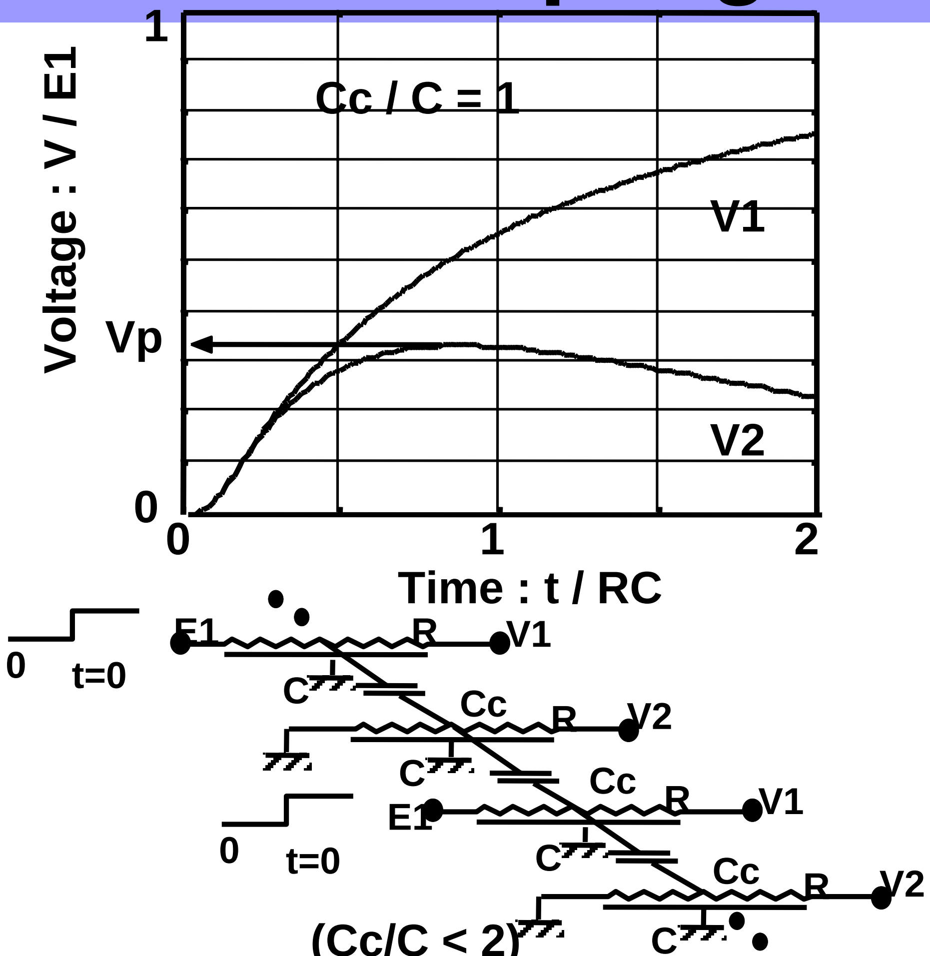
Buffered interconnect delay



Capacitive Coupling Noise



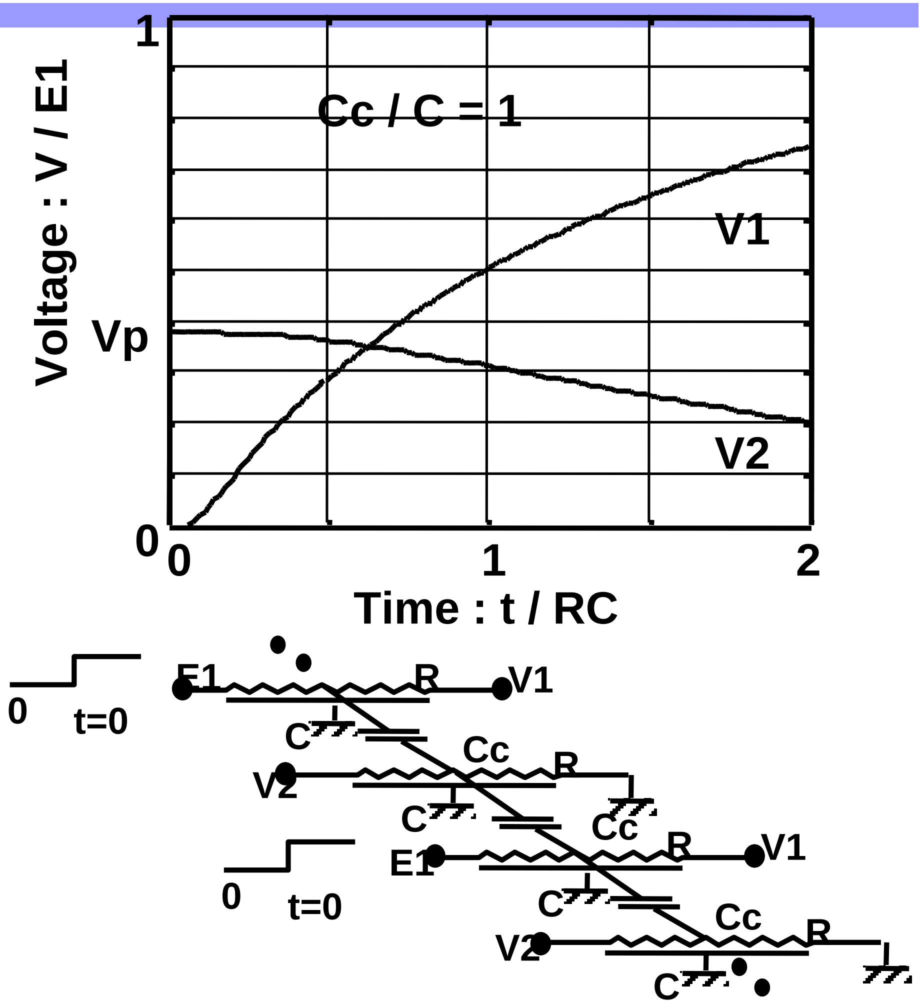
Coupling noise in RC bus



(Cc/C < 2)

$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

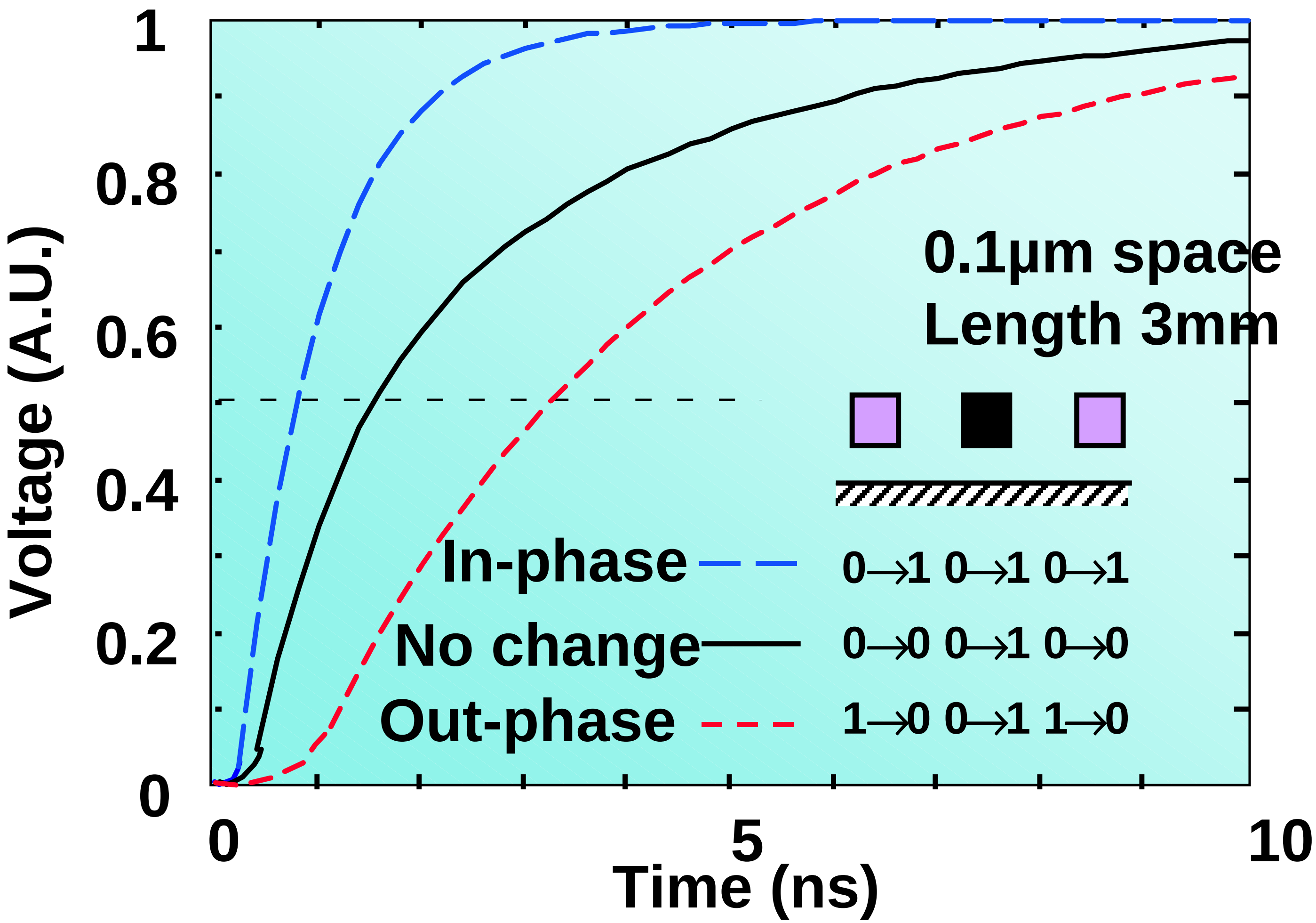
$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$



$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

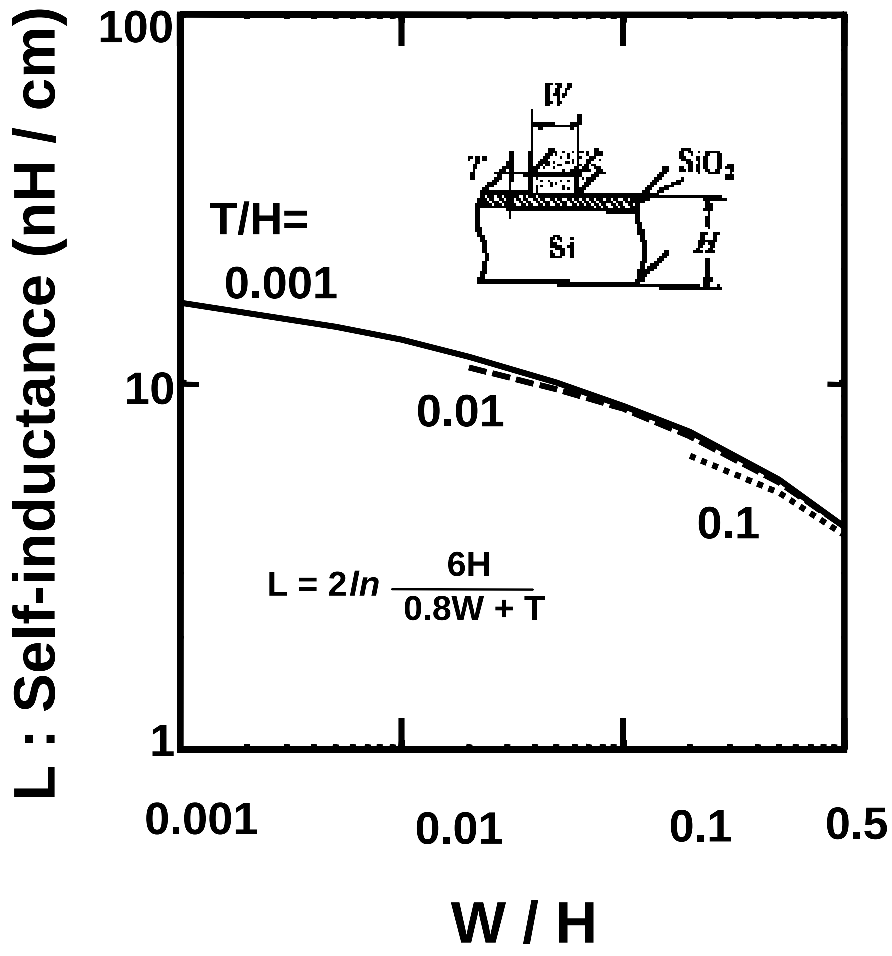
H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnection



<u>Difficulty in checking setup and hold time.</u>

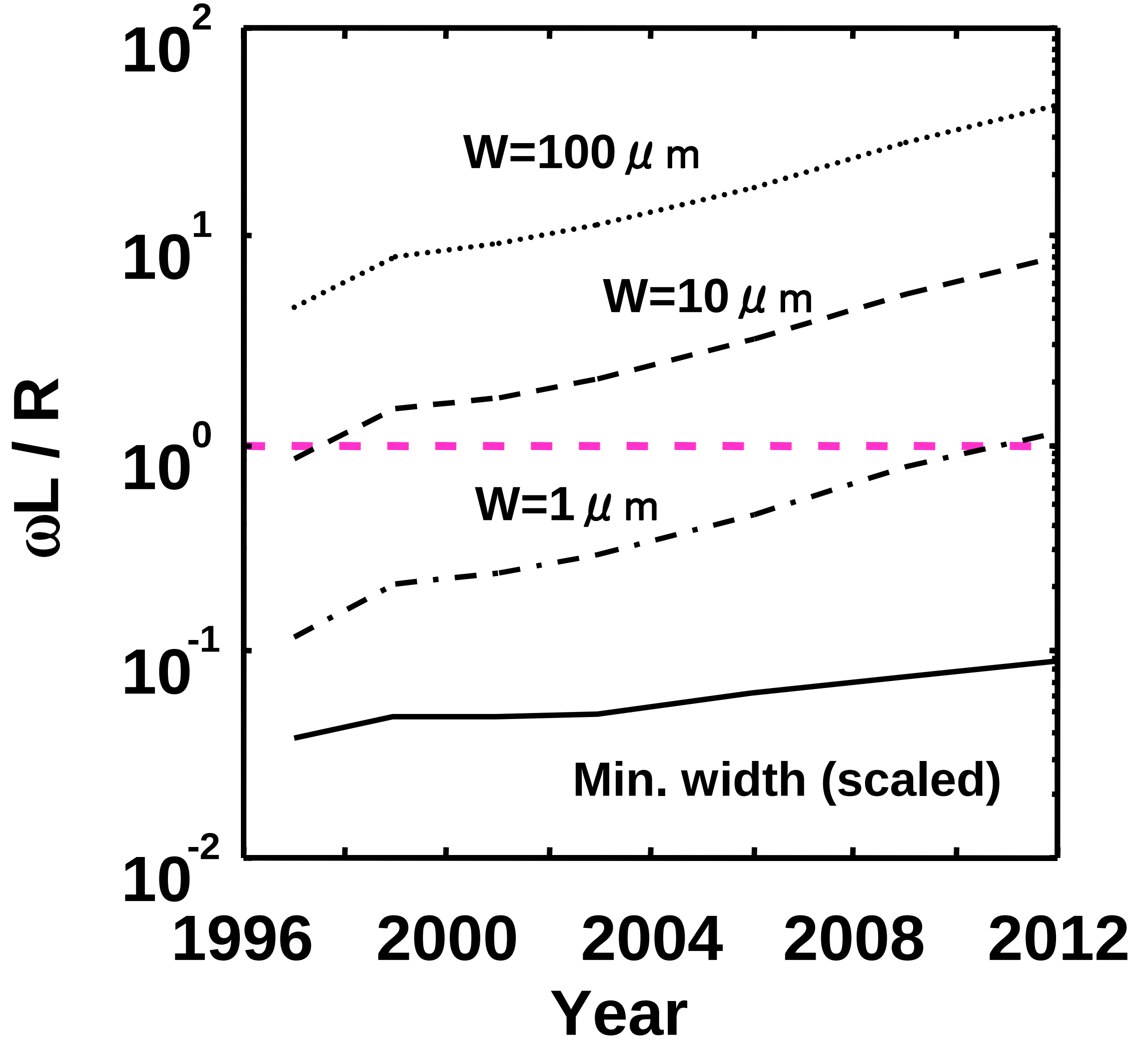
Inductance?



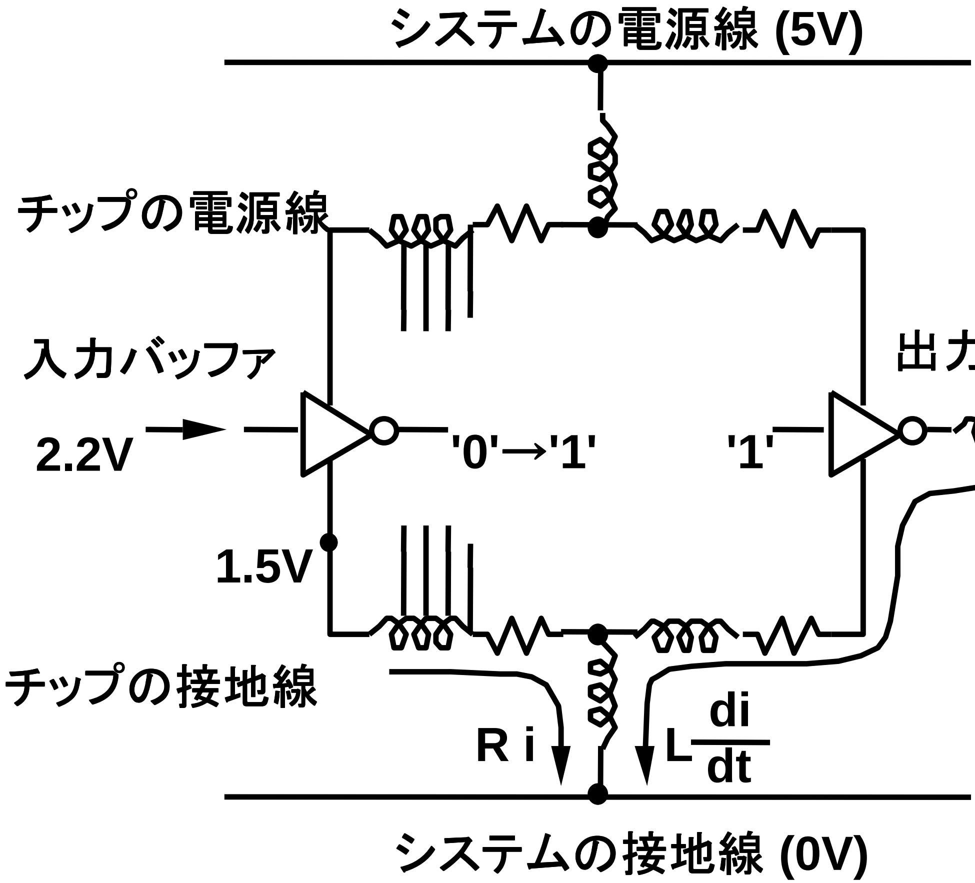
- Now RC effects surmounts LC effects because R > |jωL|.
- In the future, both of R and ωL increase (R increases more rapid?).
- Exception in low-R lines
- Inductive effects in wide clock lines in a fast processor are claimed to be observed in simulation.
- Clock lines are placed on power plane to reduce inductive effects.

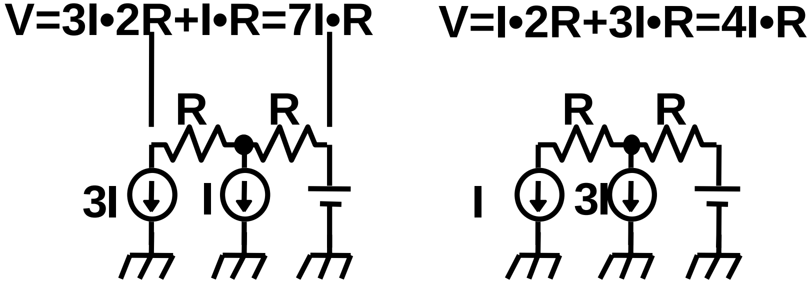
[1] D.A.Priore, "Inductance on Silicon for Sub-micron CMOS VLSI," Symp. on VLSI Circuits, 1993.

Inductive Effects

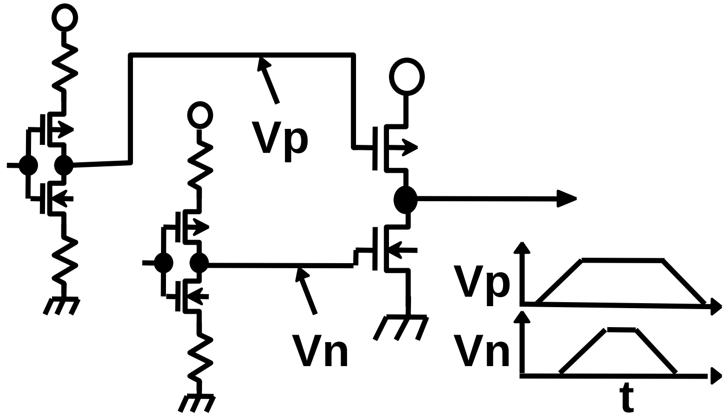


電源ノイズ

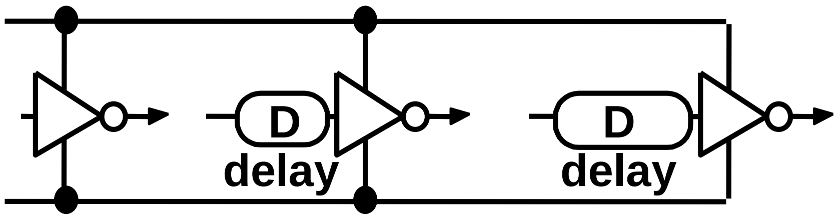




電流を多く食うブロックは電源線の根元に

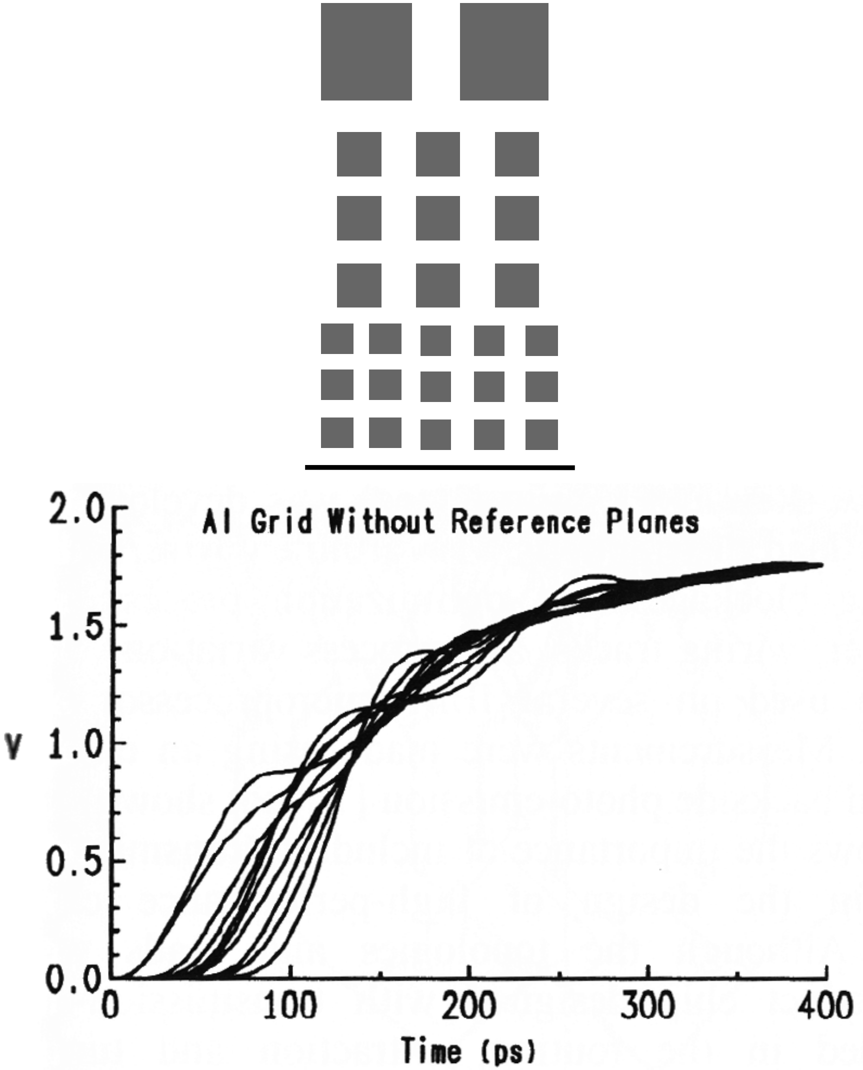


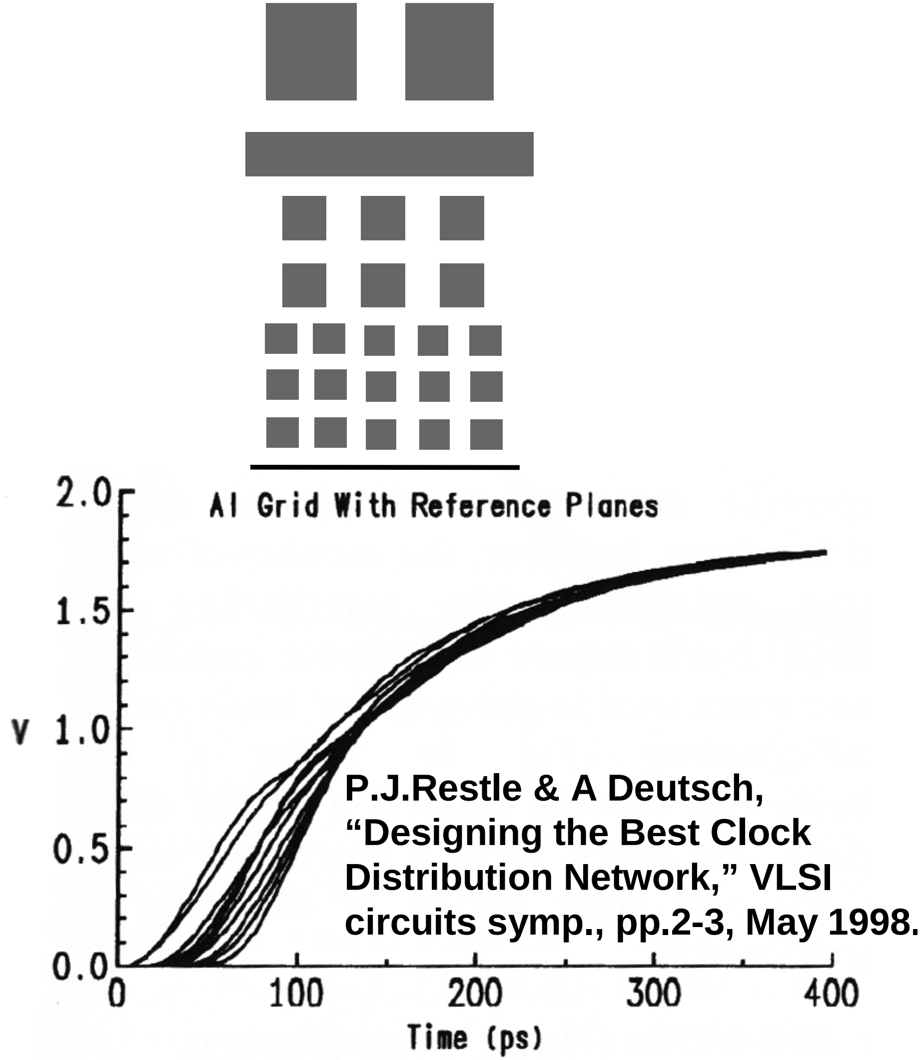
Slew-rate controlled buffer（di/dtを小さくする）



Staggered firing (電流のピーク時刻をずらす)

Inductive Effects in Clock Lines



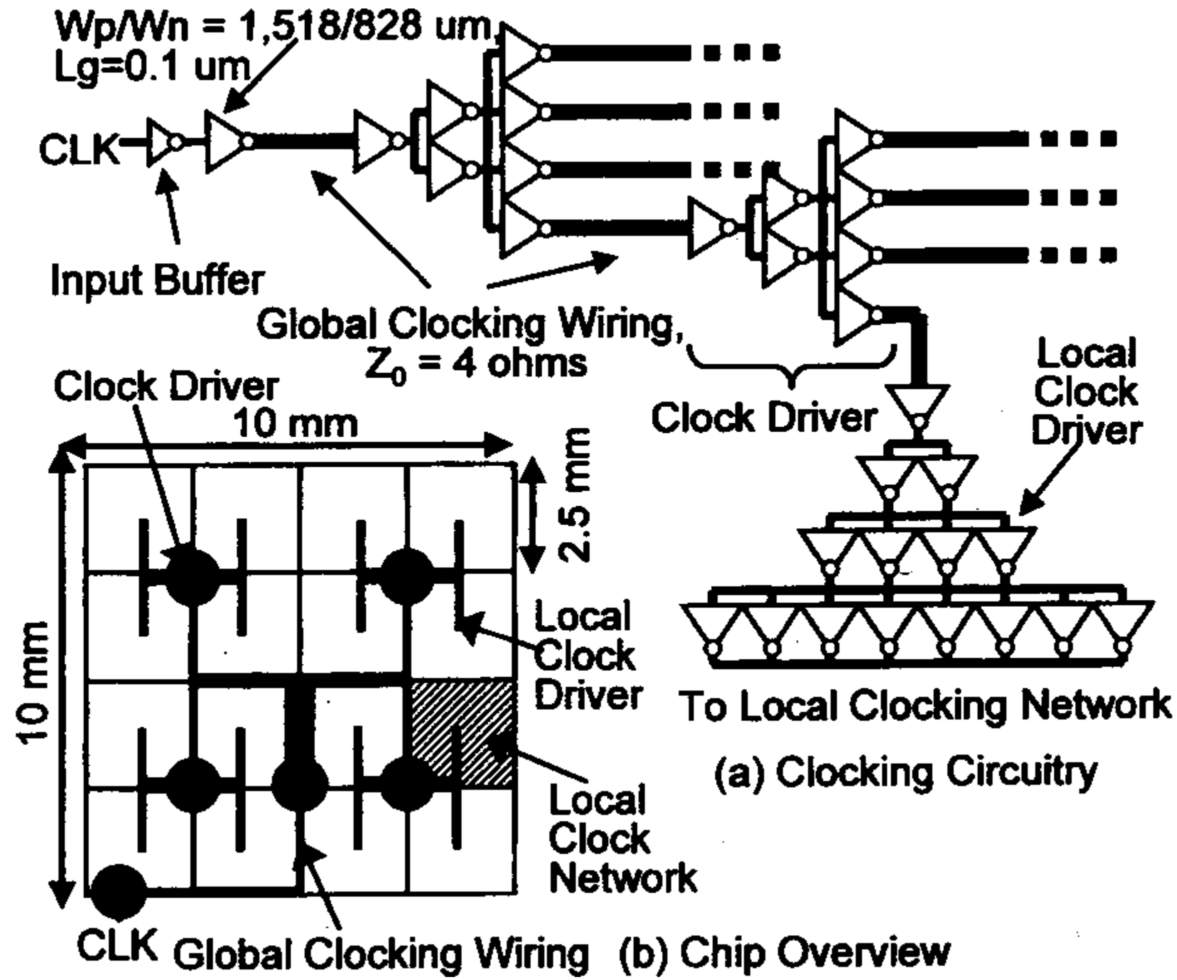


P.J.Restle & A Deutsch, “Designing the Best Clock Distribution Network,” VLSI circuits symp., pp.2-3, May 1998.

Board design practice is imported in LSI.

T.Sakurai

H-tree clock distribution

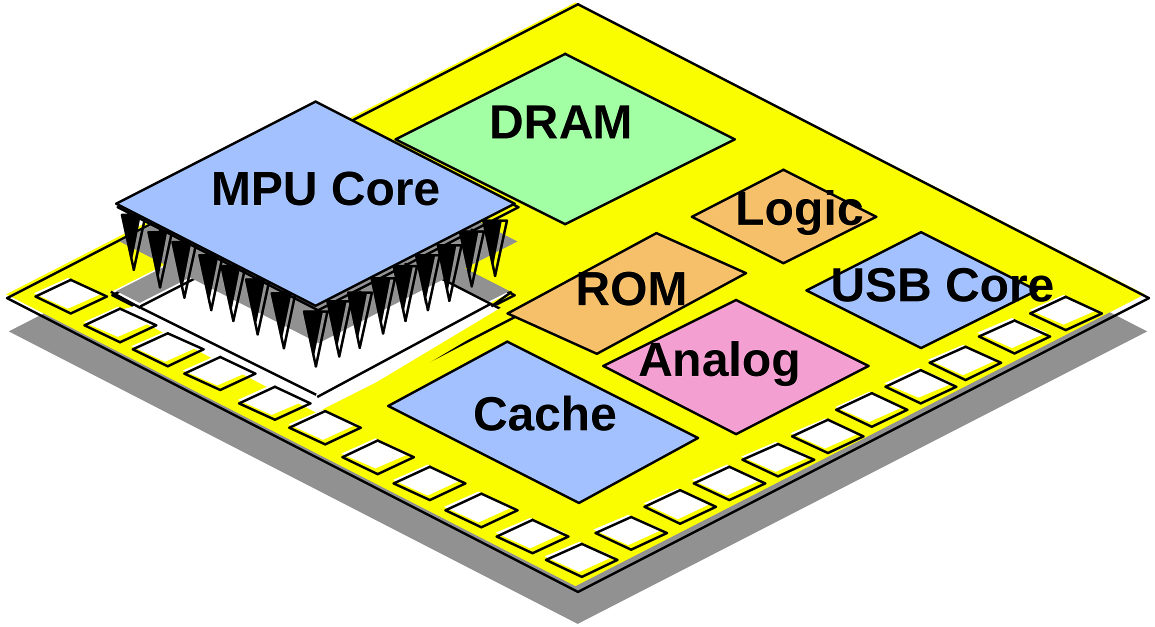


M.Mizuno, K.Anjo, Y.Sumi, H.Wakabayashi, T.Mogami, T.Horiuchi, M.Yamashina, “On-Chip Multi-GHz Clocking with Transmission Lines,” ISSCC, pp.366-367, Feb. 2000

System on a Chip (SoC)

- Re-use and sharing of design
- Design in higher abstraction

IP (A inc.)
IP (B univ.)
IP (C inst.)
IP (D semi.)

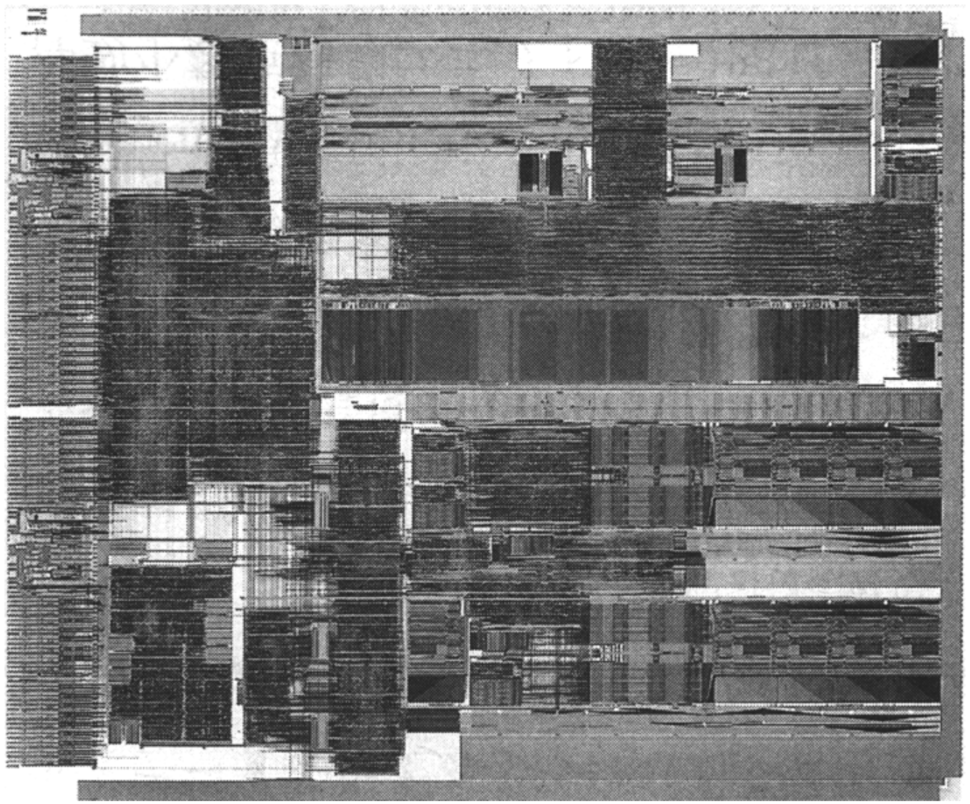


IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

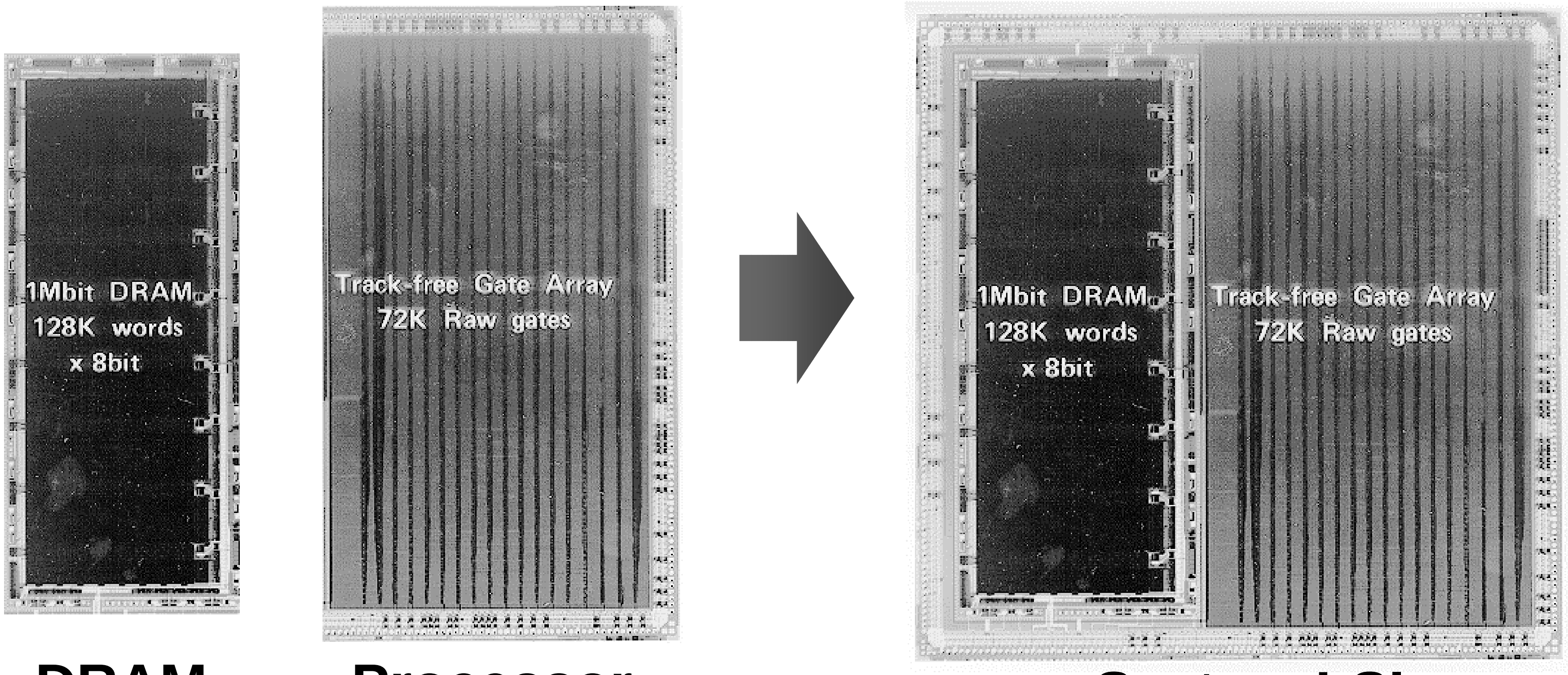
System LSI for Games

- Clock freq. 300MHz
- 10M transistors
- Graphics synthesizer integrate

  40M tr. With embedded DRAM
- Memory bandwidth 3.2GB/s
- Floating operation 6.2GFLOPS/sec
- 3D CG 6.6M polygon/sec
- MPEG2 decode



DRAM embedding

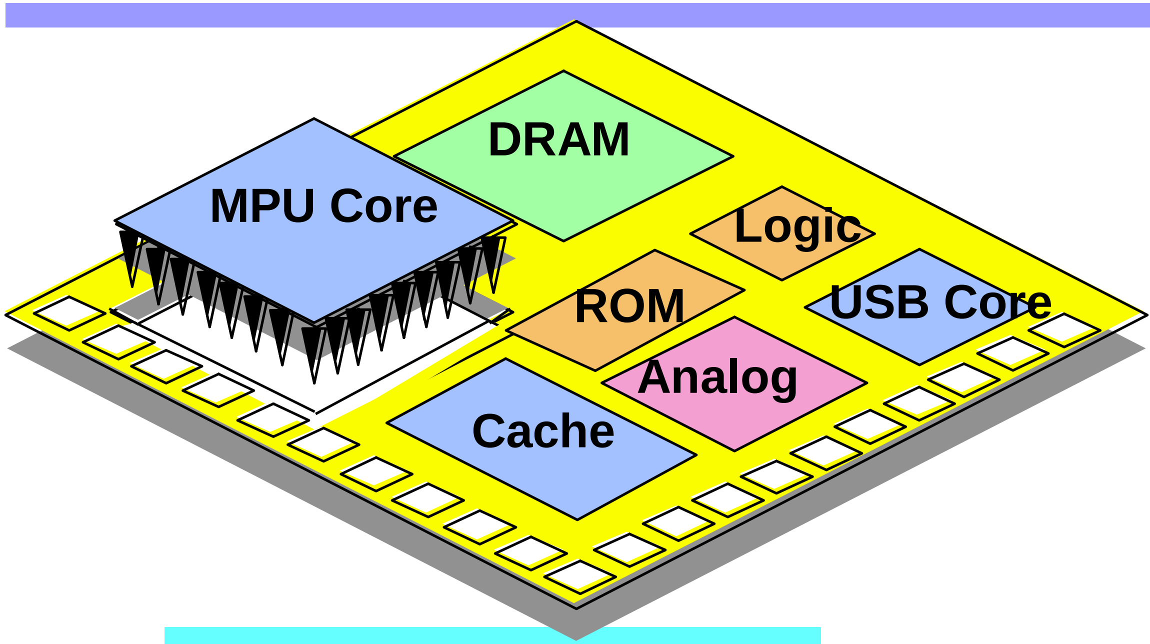


DRAM **Processor** **System LSI**

K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

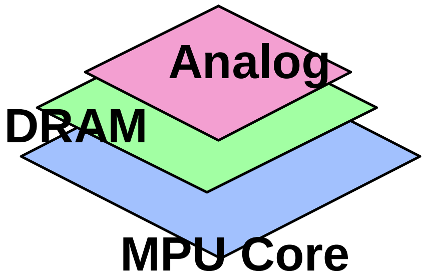
- **Two orders of magnitude improvement in bandwidth and power**

Stacked chips

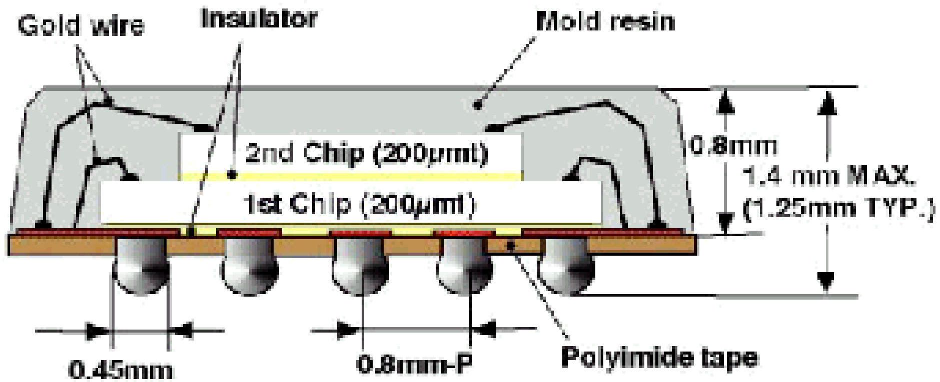


System on a chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Heat dissipation is an issue

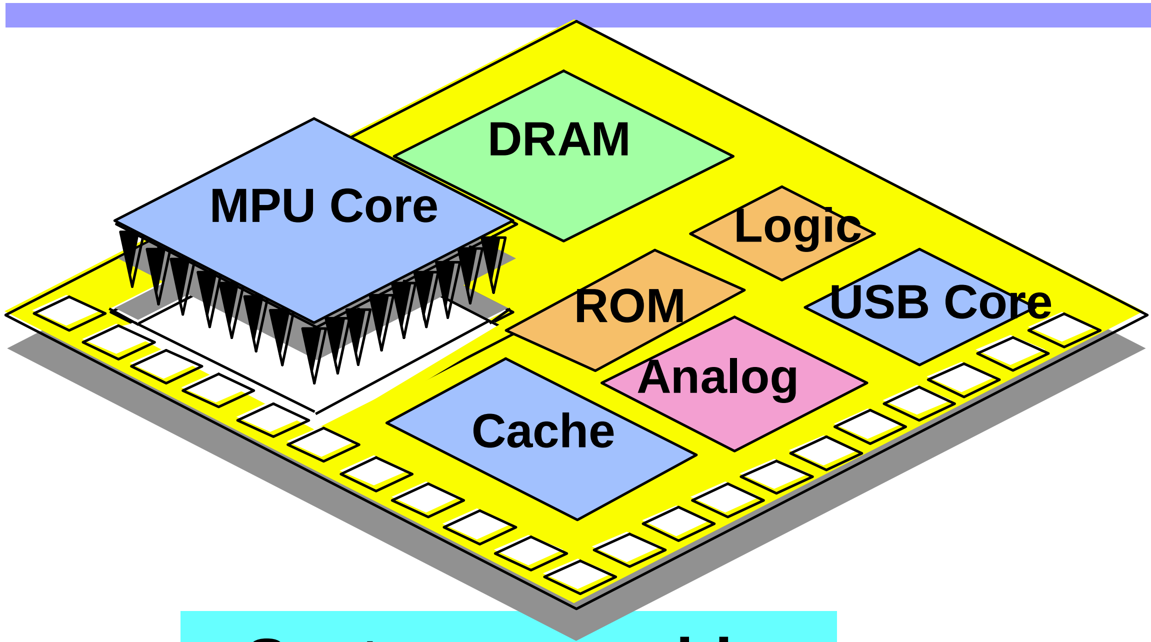


Stacked chips

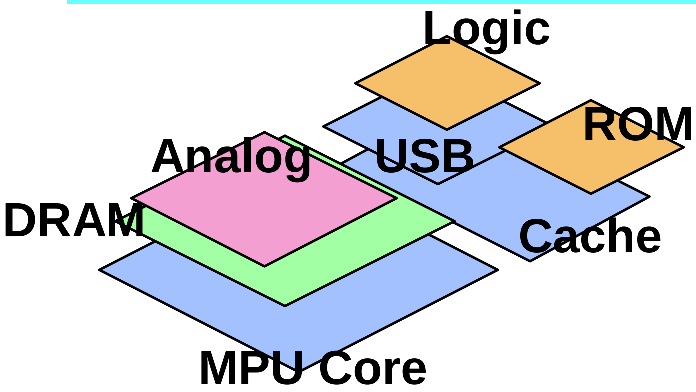


藤田他、「スタックドCSP技術」、シャープ技法、1998.8

3-Dimensional assembly



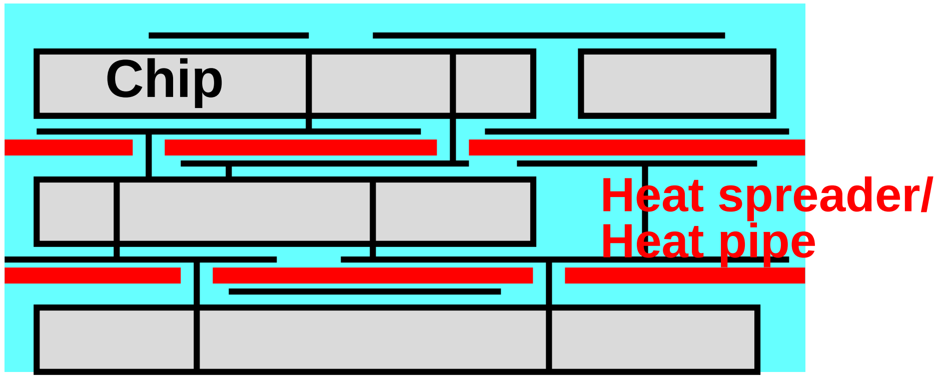
System on a chip



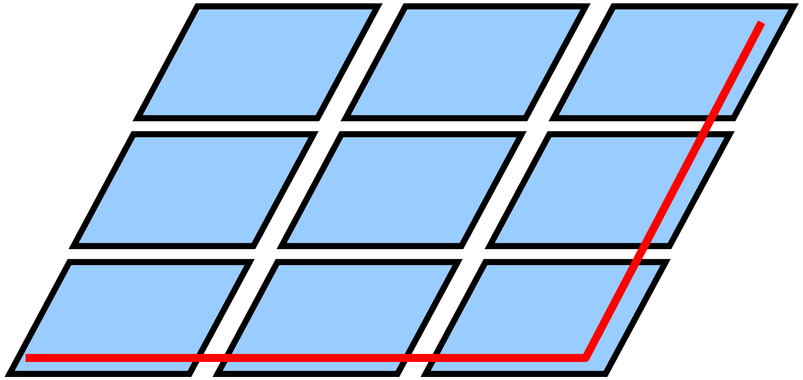
3-D assembly

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

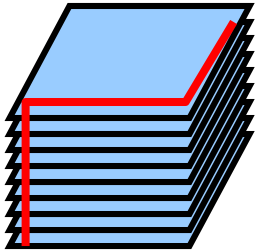
- Heat dissipation is an issue



Shorter interconnect in 3-D assembly



System on a chip



3-D assembly

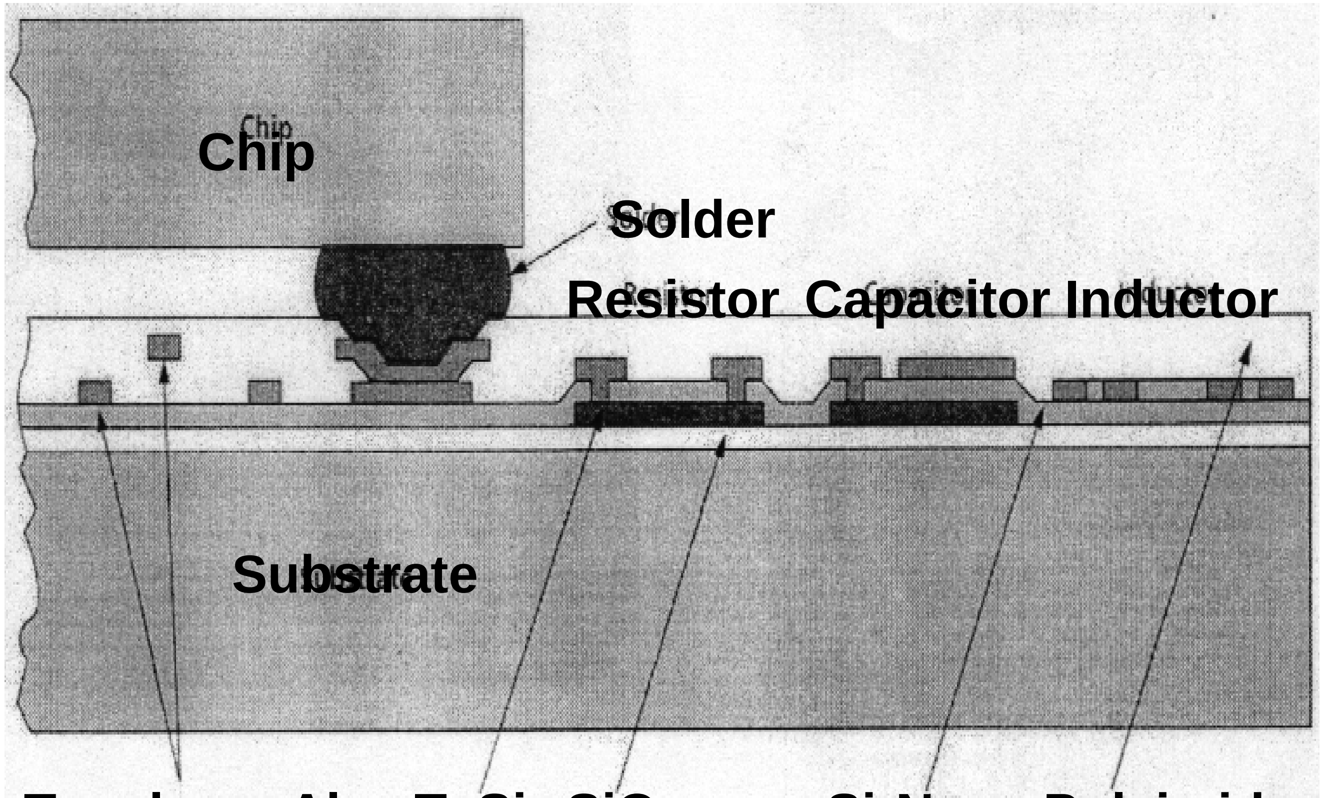
$$\frac{\#\textit{of devices in d}\,(3D)}{\#\textit{of devices in d}\,(2D)} = \frac{1}{3}\left(2\frac{d}{h} + \frac{h}{d}\right)$$

$$\approx \frac{2}{3}\left(\#\textit{of stacked chips in d}\right)$$

d: Manhattan distance

h: Height between chips

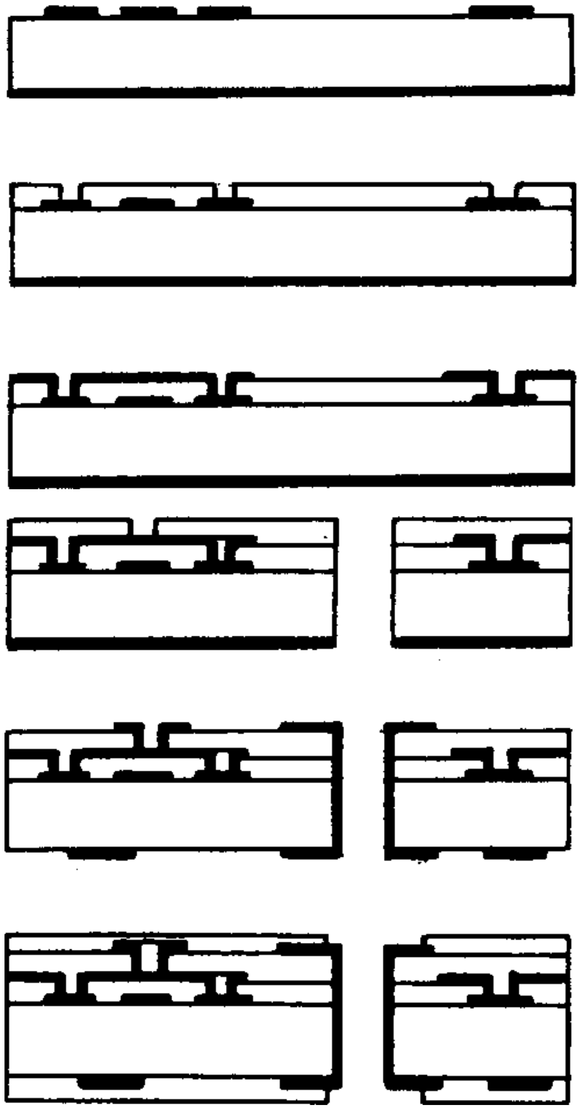
System-in-Package (SIP)



Two-layer Al TaSi SiO_2 Si_3N_4 Polyimide

K.L.Tai, “System-In-Package (SIP): Challenges and Opportunities,” ASPDAC, pp.191-196, Jan. 2000

ビルドアップ基板



両面銅張積層板→第１信号回路形成

第１絶縁層塗布→ファトバイアホール形成

銅めっき→第２信号回路形成

第２絶縁層塗布、バイアホール形成

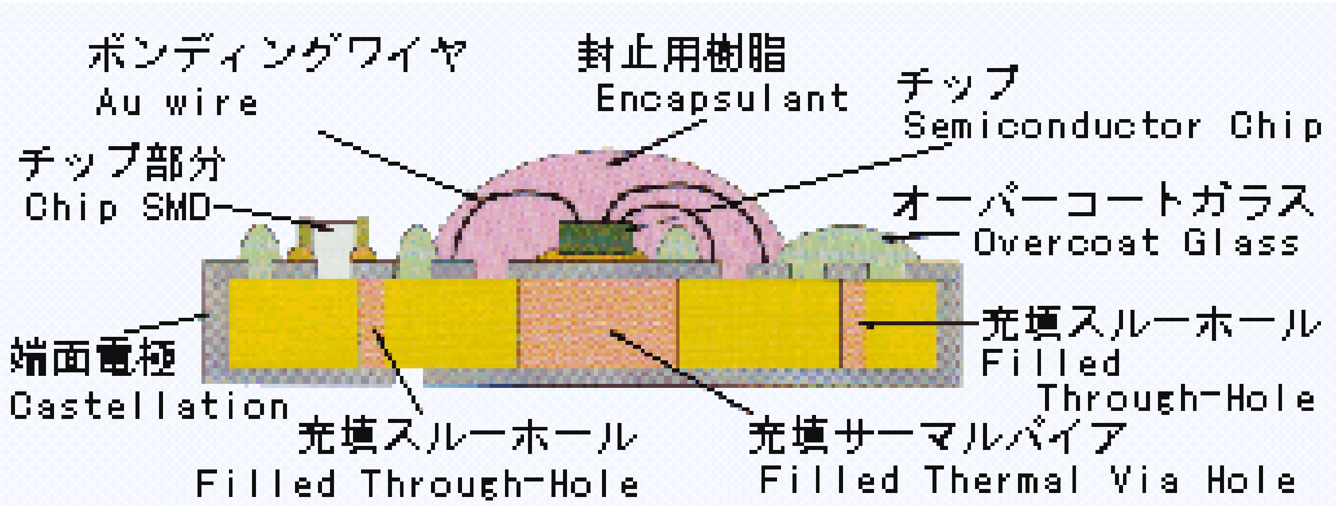
銅めっき→電源層形成

はんだ保護膜塗布

日本ビクター，10層のビルドアップMCM基板を展示，ライン／スペースは30μm／30μm
http://ne.nikkeibp.co.jp/NE/1998/eleshow98/42556.htm

出典：プリント回路技術便覧、プリント回路学会編、日刊工業新聞社

Thermal via



ミヨシ電子工業:http://www.elec.co.jp/1_kaisya/Page1410.html

System-in-Package

ELECTRONIC ENGINEERING
EE TIMES
eet.com The industry newspaper for engineers and technical management Monday, November 8, 1999

Expanding role of packaging seen relegating SoC to niche status

System-chip may topple . . .

By Robert Ristelhueber

INDIAN WELLS, CALIF. – The wheels might be coming off the system-on-chip (SoC) bandwagon, if the chatter at last week's Dataquest Semiconductor conference is any barometer of industry sentiment. Heavyweights including IBM and Lucent Technologies indicated that costs may relegate SoC to niche status, with new packaging techniques stepping into the breach.

"A couple of years ago we really thought that the embedded DRAM model would be the panacea for many applications," said John Kelly, general manager of IBM Microelectronics. "It's not always the right thing. In many applications it still remains much cheaper to do it with multichip modules. It gives you satisfactory performance and often for lower cost."

"We have systems-on-chip now that are really 'system on chips,' " said John Dickson, president of Lucent Technologies' Microelectronics Group. "We do it that way because it's most cost-effective, and the customer will prefer it that way because it offers more flexibility."

The subject was broached at the conference here by a Dataquest analyst who claimed that SoC designs will increasingly be supplanted in coming years by multichip packaging as higher mask costs squeeze SoC profitability.

Chip designers have often been willing to add mask steps

►CONTINUED ON PAGE 6

IBM's Kelly: 'In many apps, cheape to do it with multichip modules.'

. . . as industry grapple with impact of cores mode

By Peter Clarke and Brian Fuller

EDINBURGH, SCOTLAND – Intellectual property cores were a hot topic last week, both here at the IP99 Europe conference and at Dataquest Inc.'s annual semiconductor conference in Indian Wells, Calif. But as the industry struggles with new business models, new cus tomer-supplier re lationships an fast-moving tech nology, there was scant agree ment on either side of the At lantic on how the cores marke will unfold.

On one thing there was agree ment: IP cores and design reus

In some apps, multichip modules do the job more cheaply, conference told

'System-in-package' could make SoC a niche

►CONTINUED FROM PAGE 1

and complexity to their logic devices in order to place analog and memory functions onto chips. "But when we get below 0.2 micron we get a cost shock, and the [return on investment] will be diminished or even eliminated in many cases," said Clark Fuhs, vice president and director of Dataquest's Semiconductor Manufacturing Programs.

Mask costs will dramatically rise at deep submicron because of the use of phase-shift and optical proximity correction techniques as well as more expensive, 193-nm lithography equipment, putting low-volume SoC at a cost disadvantage, Fuhs said.

Militating against SoC designs for many applications is the wide disparity in revenue per square inch among the various blocks in the chip, Fuhs said. "The DSP or microprocessor block can be getting $150 or $200 per square inch, the FPGA about $120, the analog block about $35, the memory block about $50 to $60. . . You're basically diluting your high-value logic pieces with all these other low-value pieces, yet you're adding cost because you're adding mask levels."

An alternative is to fabricate the different blocks as discrete chips, placed close together using chip-scale packaging, Fuhs said. "This enables you to build the pieces in fabs that are optimized for those pieces. You can build analog in a 0.7-micron fab, standard logic can be done in 0.35 or even 0.5 micron, and for the memory you can buy a wafer from somebody and break it up. The package is more expensive, but the overall system cost is going to be substantially less.

"The concept here is to take some level of interconnect . . . and simply move [it] from the chip into the package."

Fuhs noted that Intel's Pentium III is actually an 11-level-metal device—six levels of aluminum inside the chip and five levels of copper outside. And he showed a photograph of a Sony digital Handycam, which he said contains 20 chip-scale devices, "so this technology is here, it's real."

National's Halla touts 'integrated disintegration.'

In the not-too-distant future, he said, wafer foundries will give customers a choice of implementing a design either as a system-on-chip or as several discrete devices using chip-scale packaging.

To survive, the SoC must evolve to fit a more standard-product model that would allow it to increase volume and become more cost-efficient, Fuhs said. He predicted that within five years, multichip packaging will be growing faster than SoC designs.

That view has its detractors. "Mask sets cost in excess of a couple hundred thousand dollars, whether you do small chips or large chips," said National Semiconductor Corp. chief executive officer Brian Halla, who has championed the notion of an information appliance-on-a-chip. "I can get tremendously more performance out of the same square inches of silicon by having it all together instead of having it two inches apart on a board.

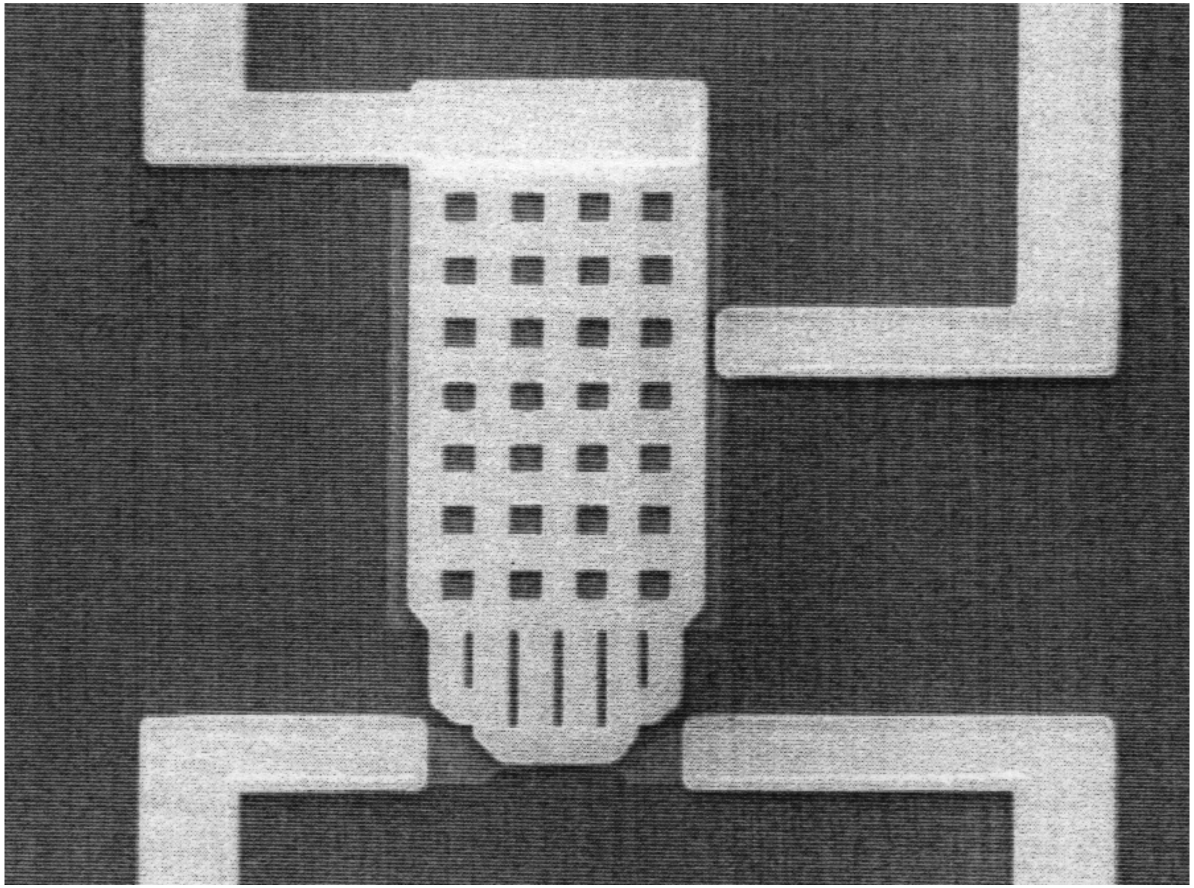
"SoC isn't a marketing crusade anymore; it's something you can do because the technology allows it," Halla added. "A very small die can contain an awful lot of functionality."

Halla noted that Intel used to say graphics shouldn't be combined with the microprocessor, because the pace of innovation differs between those parts; but Intel's upcoming Timna processor, he said, combines both functions.

"Having said all that, there are cases where we agree [about putting a system on a package]," he said. "There is a substrategy of ours called integrated disintegration, which means there are analog functions you can pull off the chip because they are such a tiny portion of the overall chip, and yet they are the most difficult thing to port to the next-generation [process] technology."

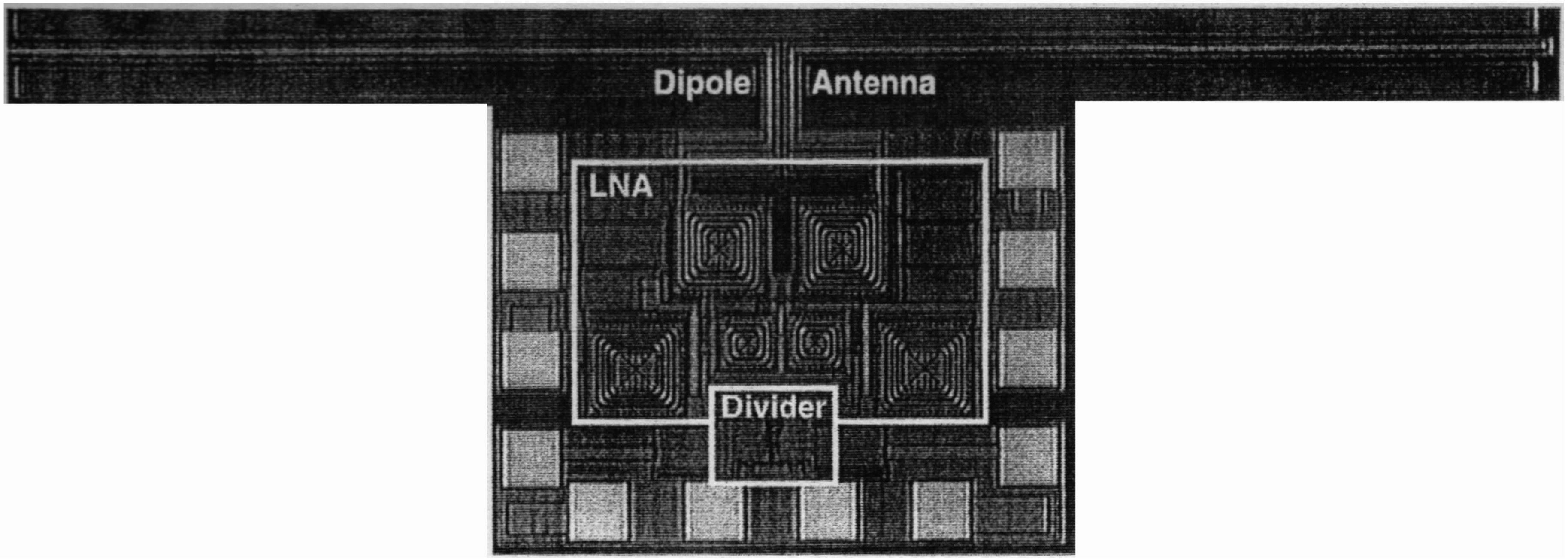
IBM's Kelly said that "SoC integration has to be done se-

Micro-machined mechanical switch



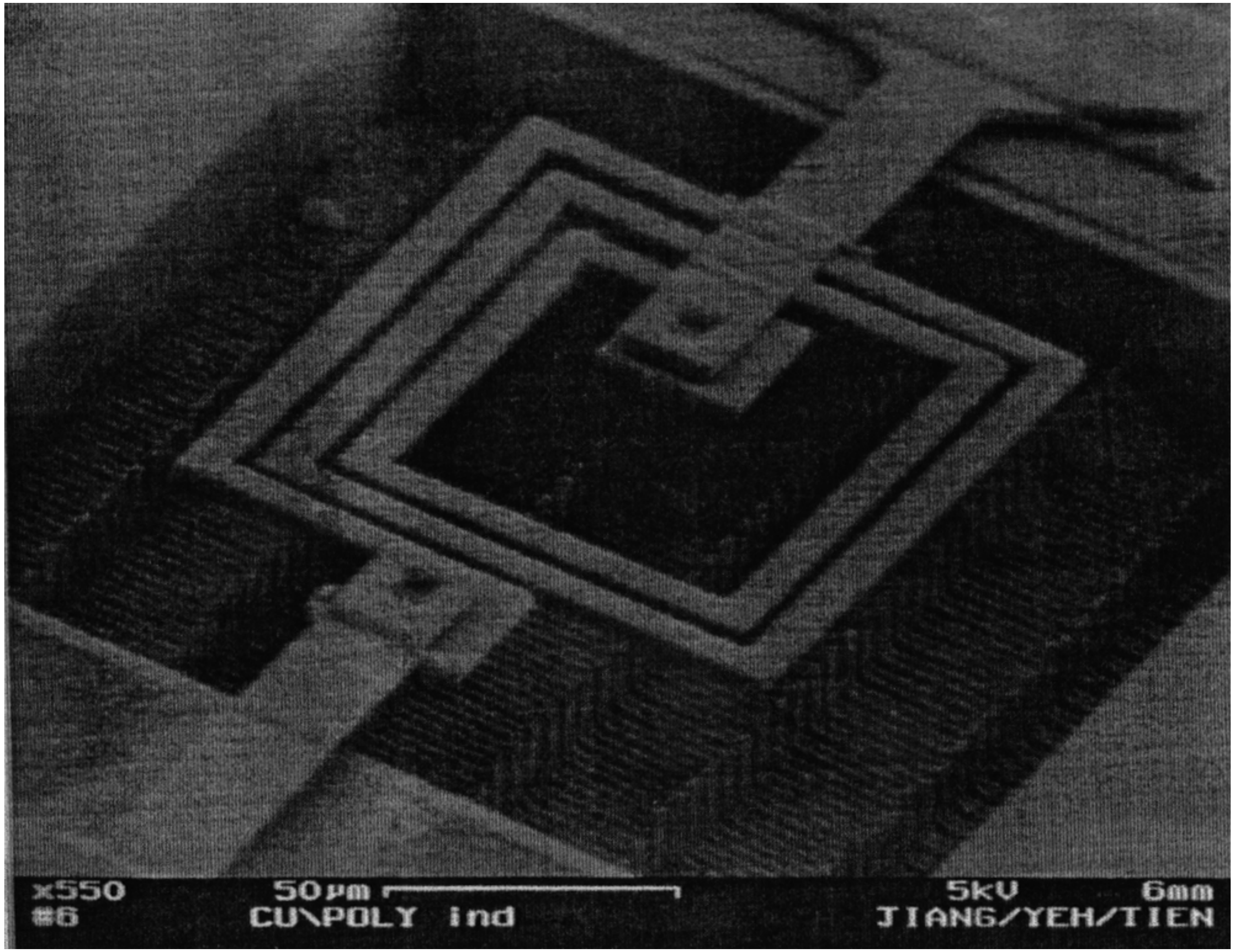
G.Weinberger, “The New Millennium: Wireless Technologies for a Truly Mobile Society,” ISSCC, pp.20-24, Feb. 2000.

Antenna on chip



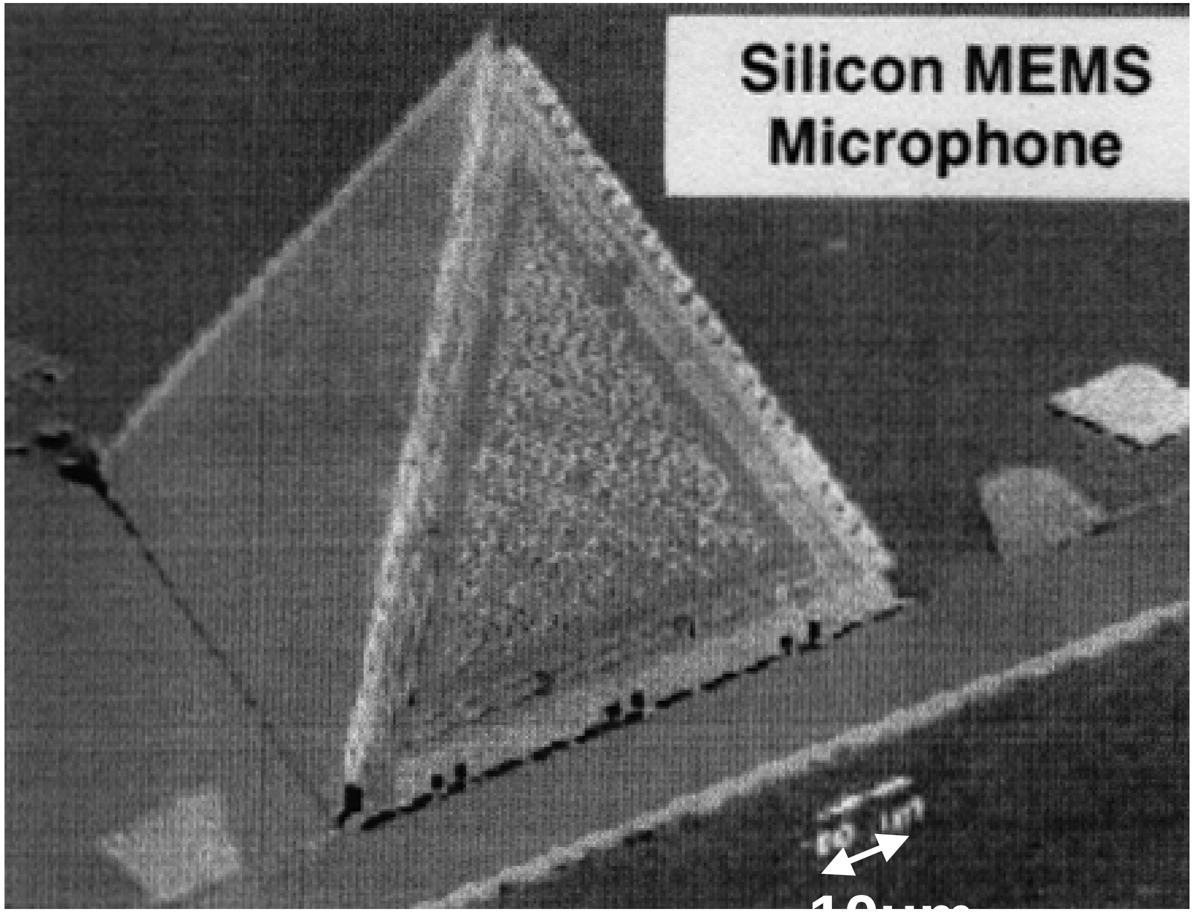
B.Floyd, K.Kim and Kenneth, “Wireless Interconnection in a CMOS IC with Integrated Antennas,” ISSCC, pp.328-329, Feb. 2000.

Suspended spiral inductor



H.Jiang J.Yeh, Y.Wang, N.Tien, “Electromagneticallt Shielded High-Q CMOS-Compatible Copper Inductor,” ISSCC, pp.330-331, Feb. 2000.

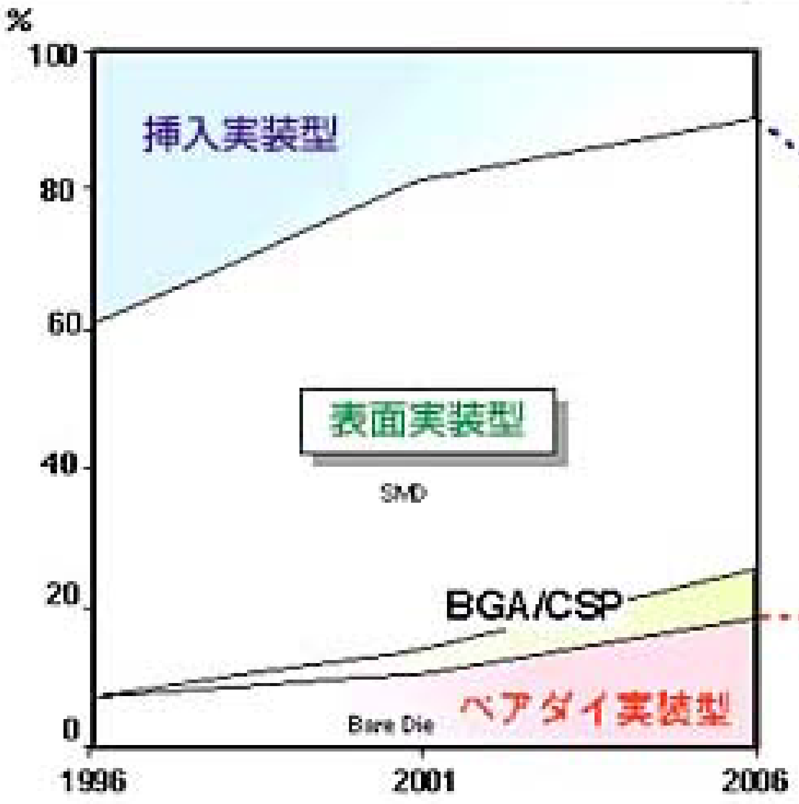
Silicon MEMS microphone



Will soon exceed the performance of the best commercial microphones, yet be inexpensive and potentially integrated with on-chip electronics.

M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

ICパッケージの世界市場動向



	1996	2001	2006
DIP	16.08	11.70	6.75
SIP/ZIP	4.20	3.40	2.70
PGA	0.49	0.74	0.60
Others	0.25	0.38	0.53
Total	21.02	16.22	10.57
SO	17.81	34.71	46.70
PLCC	2.70	1.70	0.60
PQFP	6.42	17.67	19.45
Hermetics	0.30	0.37	0.32
BGA / CSP	0.10	2.00	7.60
TAB	0.85	1.60	3.04
Others	0.25	0.38	0.53
Total	28.43	58.36	78.23
COB	3.25	5.65	12.41
Flip Chip	0.52	3.05	7.50
Total	3.77	8.70	19.91
合計 (単位:10億個)	53.22	83.27	108.71

（ソース： BPA 社）

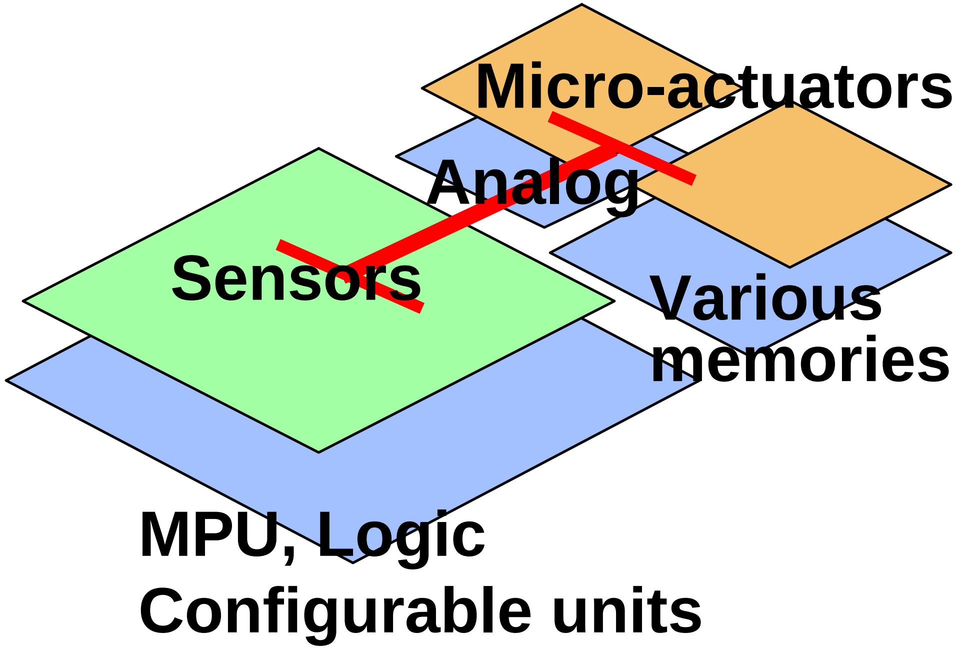
http://www.ic.nec.co.jp/pkg/japanese/jissou/1/1_1/1_1_2/

LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	µm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (µP)		21M	3.6G	170
DRAM capacity		1G	1T	256
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	µcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA) , International Technology Roadmap for Semiconductors: 1999 edition. Austin, TX:International SEMATECH, 1999.

Possible electronic system in 2014

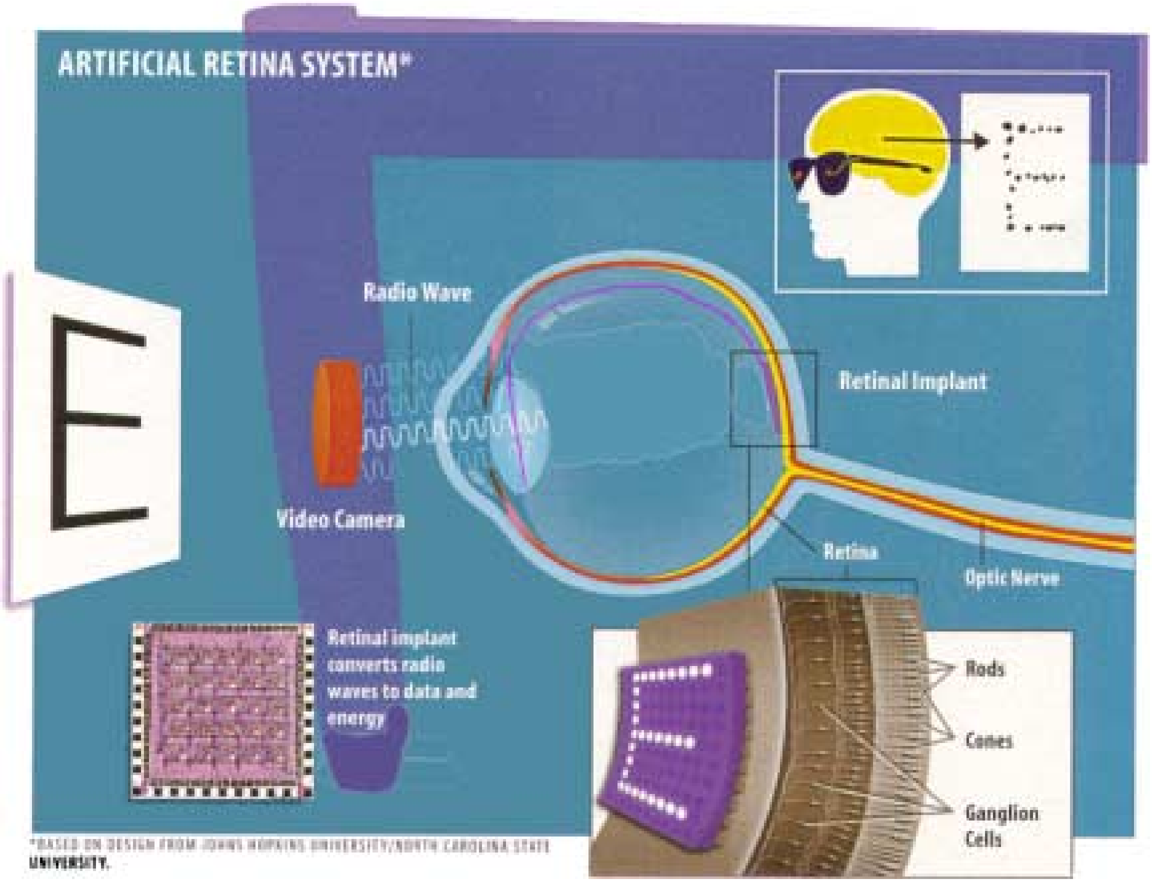


- Sensors/actutors
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)

Prosthesis - Dual Intraocular Units

NC STATE UNIVERSITY

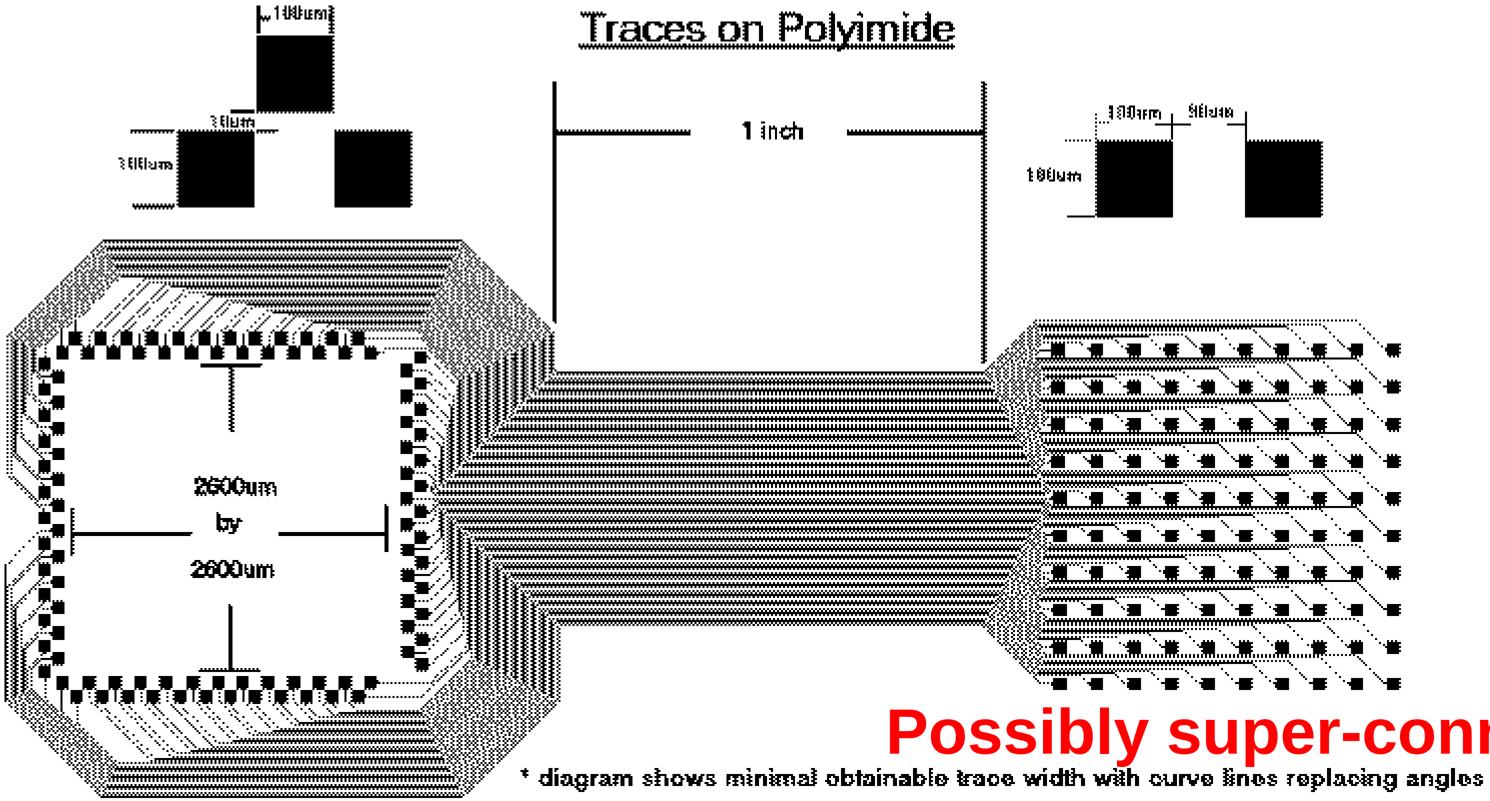
Retinal Prosthesis



Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Chip + Electrode Array on Polyimide

NC STATE UNIVERSITY



Possibly super-connect

Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Super-connect

P: Power, D: Delay, A: Area, T:Turn-around