第32回　日経マイクロデバイス・セミナー　’00/10

なぜシステム・イン・パッケージか？
システムLSIとの対比

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システムLSIとシステムインパッケージ

日本の大手半導体企業は、メモリの量産からより付加価値の高いシステムLSI生産にビジネスの重点を移行し始めている。システムLSIとは複雑なシステム機能を1つのシリコンチップに作りこんだものである。最近では、大容量のダイナミックメモリとプロセッサをワンチップ上に一緒に集積したシステムLSIまで開発されている。この例では、2チップ構成だとメモリとプロセッサ間のデータのやり取りに多大な電力がかかっていたが、システムLSI化することで消費電力を1/4にまで低減できた。このようにシステムLSIでは、今まで多数のチップで作られていた電子システムをワンチップ化することにより数倍高性能にしたり、低電力化したりできる。

しかし、システムLSIを実際に作ってみると、いくつかの問題点も明らかになってきた。システムLSIの設計には、すでに設計検証の終ったIPと呼ばれる大きな回路ブロックの設計データを組み合わせて作り上げる方式がとられる。数千万個に上るトランジスタを使ったシステムを一から設計していては、とても開発期限に間に合わないからだ。そのため、システムLSIの成否には多数のIPが市場に流通していることが重要であり、そのような流通市場もいくつか誕生した。

システムLSIとシステムインパッケージ（続）

ここで次のような場合を考えよう。性能や機能の観点から、どうしてもA社製のプロセッサとB社製のメモリをワンチップ化しシステムLSI化したいとする。これらの回路ブロックがIPとして流通していれば、A社とB社からこれらの回路ブロックの設計データを調達し、どこかの半導体製造会社に持ち込んでシステムLSIを作ることができる。ところが、A社がどうしてもプロセッサの設計データを一般の市場には出さないとしよう。理由としては自社で製造も行うことによって高付加価値の製品に仕上げたいといったことが考えられる。するとA社とB社の製品を使ったシステムLSIを作ることができなくなってしまう。今までは、A社とB社から独立にチップを購入して、プリント基板を使って高性能な電子システムが組めたものが、システムLSIではA社とB社の組み合わせは不可能となる。これでは所望の電子システムができない。

また、本質的にワンチップ化できないものもシステムLSI化の障害となる。例えば、ガリウム砒素という半導体基板を使った高速なチップとシリコン基板のチップをワンチップ化するのは不可能だ。高性能なアナログチップとデジタルチップをワンチップ化するのにも無理がある。デジタル回路から出されるノイズが基板を伝わってアナログ部分に悪影響を及ぼし、性能を低下させてしまうためである。その他、システムLSIの開発や検証には、年単位の期間がかかったり、億円単位のコストがかかるといった問題もある。システムLSIではチップサイズが大きくなって歩留まりが低下し、価格が跳ね上がるといった指摘もされている。

システムLSIとシステムインパッケージ（続）

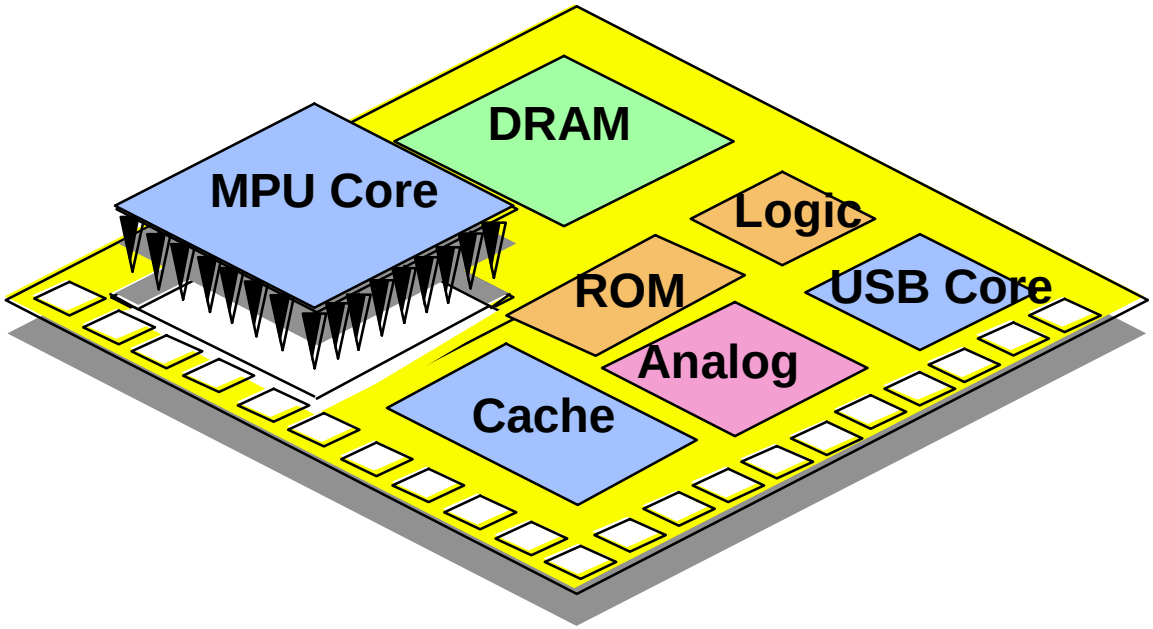
だからといって、今さらプリント基板に多数のチップを載せて電子システムを組むというのでは性能的に限界がある。このような問題を軽減するものとして、最近、システム・イン・パッケージという新しい三次元実装技術が注目されている。例えば、チップをインターポーザーと呼ばれる超薄型で小型な支持物に固定し、これらを複数個組み合わせて、システムを一つのパッケージの中に入れてしまおうというものである。半導体チップ以外にもコイルやコンデンサ、水晶発振子などもワンパッケージに収められる新しい三次元実装形態だ。こうすることによって速度、電力、実装面積などを従来のプリント基板で作った電子システムより数倍改善することができ、システムLSIにも匹敵する性能を実現できる場合も多い。このような新しい実装技術ではスーパーコネクトと呼ばれる0.01～0.1ミリ幅の配線技術が活躍する。

日本は半導体技術も実装技術も技術としては世界最先端を走っている。しかし、米国で設計しアジア諸国で製造するといった水平分業型のモデルに対してのコスト競争力の低下から、ここ数年ビジネスとして米国などに水をあけられる結果となってしまった。日本の有する各種の技術分野を有機的に連携させ、垂直統合的な色彩も加えながら半導体産業を再生することが、わが国の電子産業の将来の競争力をより確固なものにすると考えられる。新しいシステム・イン・パッケージといった三次元実装技術が未来を担う技術として注目されているゆえんである。システム・イン・パッケージの設計は半導体チップの設計と密接な連携を取る必要があり、従って、分野間の有機的な連携なくしては高性能な最終製品に仕上がらないためである。　日経産業新聞（桜井貴康）

System on a Chip (SoC)

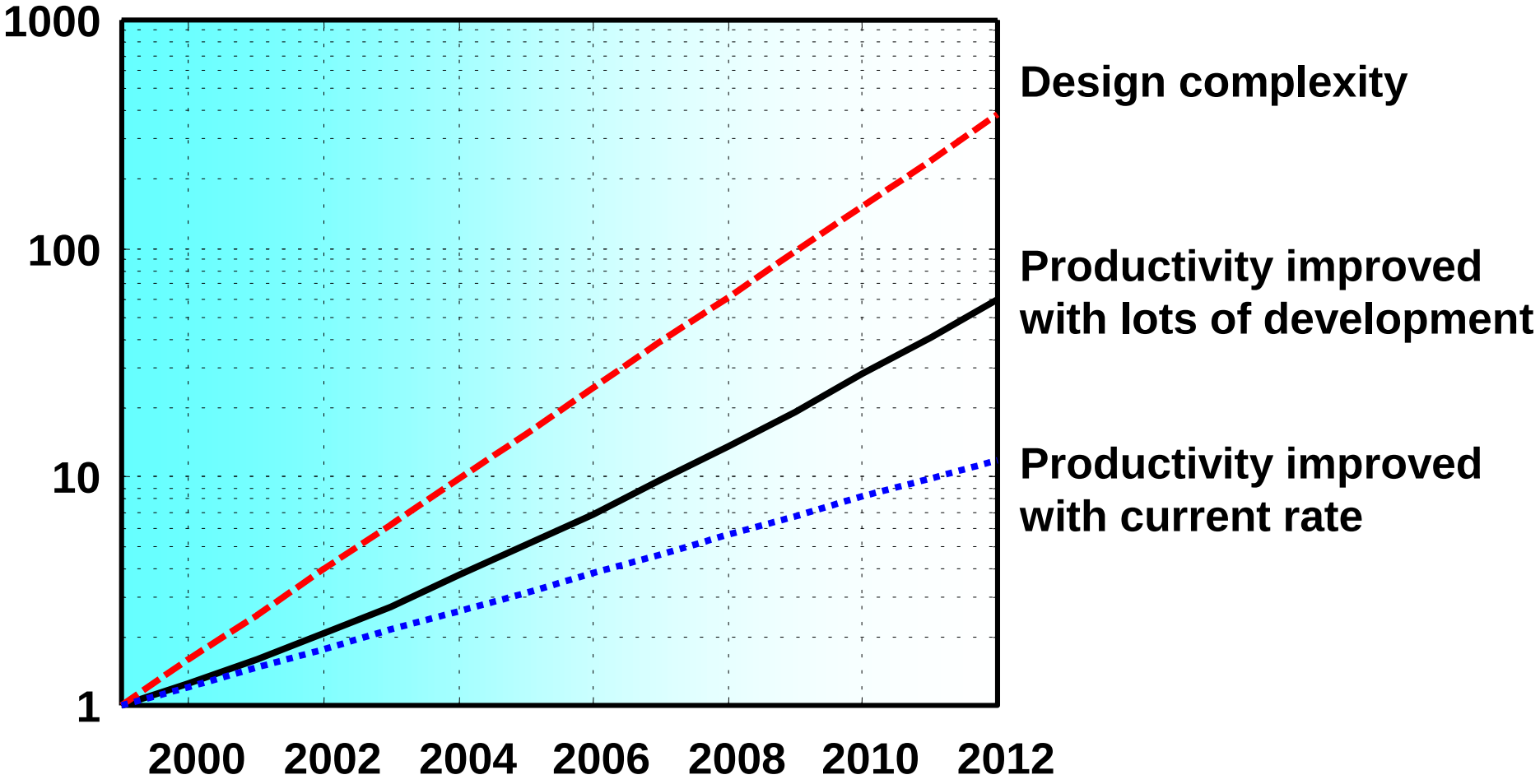
- Re-use and sharing of design
- Design in higher abstraction

IP (A inc.)
IP (B univ.)
IP (C inst.)
IP (D semi.)



IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

Complexity vs. Productivity

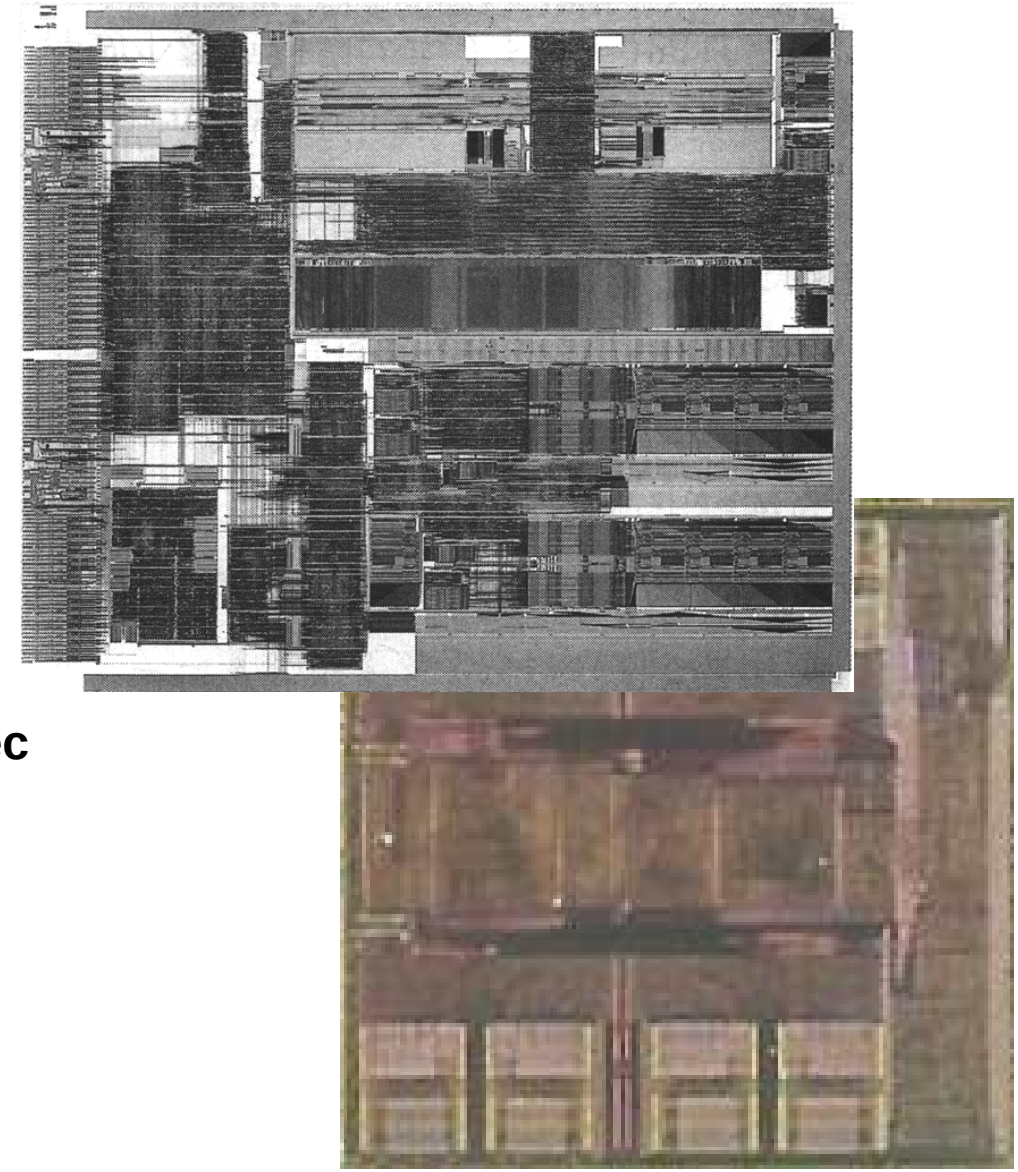


- System LSI design complexity increases faster than productivity. (http://notes.sematech.org/97melec.htm)

System LSI for Next Generation Games

- Clock freq. 300MHz
- 10M transistors
- Graphics synthesizer integrate

  40M tr. With embedded DRAM
- Memory bandwidth 3.2GB/s
- Floating operation 6.2GFLOPS/sec
- 3D CG 6.6M polygon/sec
- MPEG2 decode



T.Sakurai

System-in-Package

ELECTRONIC ENGINEERING
EE TIMES
eet.com The industry newspaper for engineers and technical management Monday November 8, 1999

Expanding role of packaging seen relegating SoC to niche status

System-chip may topple . . .

By Robert Ristelhueber

INDIAN WELLS, CALIF. – The wheels might be coming off the system-on-chip (SoC) bandwagon, if the chatter at last week's Dataquest Semiconductor conference is any barometer of industry sentiment. Heavyweights including IBM and Lucent Technologies indicated that costs may relegate SoC to niche status, with new packaging techniques stepping into the breach.

"A couple of years ago we really thought that the embedded DRAM model would be the panacea for many applications," said John Kelly, general manager of IBM Microelectronics. "It's not always the right thing. In many applications it still remains much cheaper to do it with multichip modules. It gives you satisfactory performance and often for lower cost."

"We have systems-on-chip now that are really 'system on chips,' " said John Dickson, president of Lucent Technologies' Microelectronics Group. "We do it that way because it's most cost-effective, and the customer will prefer it that way because it offers more flexibility."

The subject was broached at the conference here by a Dataquest analyst who claimed that SoC designs will increasingly be supplanted in coming years by multichip packaging as higher mask costs squeeze SoC profitability.

Chip designers have often been willing to add mask steps

▸CONTINUED ON PAGE 6

IBM's Kelly: 'In many apps, cheaper to do it with multichip modules.'

. . . as industry grapples with impact of cores mode

By Peter Clarke and Brian Fuller

EDINBURGH, SCOTLAND – Intellectual property cores were a hot topic last week, both here at the IP99 Europe conference and at Dataquest Inc.'s annual semiconductor conference in Indian Wells, Calif. But as the industry struggles with new business models, new customer-supplier relationships and fast-moving technology, there was scant agreement on either side of the Atlantic on how the cores market will unfold.

On one thing there was agreement: IP cores and design reus

In some apps, multichip modules do the job more cheaply, conference told

'System-in-package' could make SoC a niche

▸CONTINUED FROM PAGE 1

and complexity to their logic devices in order to place analog and memory functions onto chips. "But when we get below 0.2 micron we get a cost shock, and the [return on investment] will be diminished or even eliminated in many cases," said Clark Fuhs, vice president and director of Dataquest's Semiconductor Manufacturing Programs.

Mask costs will dramatically rise at deep submicron because of the use of phase-shift and optical proximity correction techniques as well as more expensive, 193-nm lithography equipment, putting low-volume SoC at a cost disadvantage, Fuhs said.

Militating against SoC designs for many applications is the wide disparity in revenue per square inch among the various blocks in the chip, Fuhs said. "The DSP or microprocessor block can be getting $150 or $200 per square inch, the FPGA about $120, the analog block about $35, the memory block about $50 to $60 . . . You're basically diluting your high-value logic pieces with all these other low-value pieces, yet you're adding cost because you're adding mask levels."

An alternative is to fabricate the different blocks as discrete chips, placed close together using chip-scale packaging, Fuhs said. "This enables you to build the pieces in fabs that are optimized for those pieces. You can build analog in a 0.7-micron fab, standard logic can be done in 0.35 or even 0.5 micron, and for the memory you can buy a wafer from somebody and break it up. The package is more expensive, but the overall system cost is going to be substantially less.

"The concept here is to take some level of interconnect . . . and simply move [it] from the chip into the package."

Fuhs noted that Intel's Pentium III is actually an 11-level-metal device—six levels of aluminum inside the chip and five levels of copper outside. And he showed a photograph of a Sony digital Handycam, which he said contains 20 chip-scale devices, "so this technology is here, it's real."

National's Halla touts 'integrated disintegration.'

In the not-too-distant future, he said, wafer foundries will give customers a choice of implementing a design either as a system-on-chip or as several discrete devices using chip-scale packaging.

To survive, the SoC must evolve to fit a more standard-product model that would allow it to increase volume and become more cost-efficient, Fuhs said. He predicted that within five years, multichip packaging will be growing faster than SoC designs.

That view has its detractors. "Mask sets cost in excess of a couple hundred thousand dollars, whether you do small chips or large chips," said National Semiconductor Corp. chief executive officer Brian Halla, who has championed the notion of an information appliance-on-a-chip. "I can get tremendously more performance out of the same square inches of silicon by having it all together instead of having it two inches apart on a board.

"SoC isn't a marketing crusade anymore; it's something you can do because the technology allows it," Halla added. "A very small die can contain an awful lot of functionality."

Halla noted that Intel used to say graphics shouldn't be combined with the microprocessor, because the pace of innovation differs between those parts; but Intel's upcoming Timna processor, he said, combines both functions.

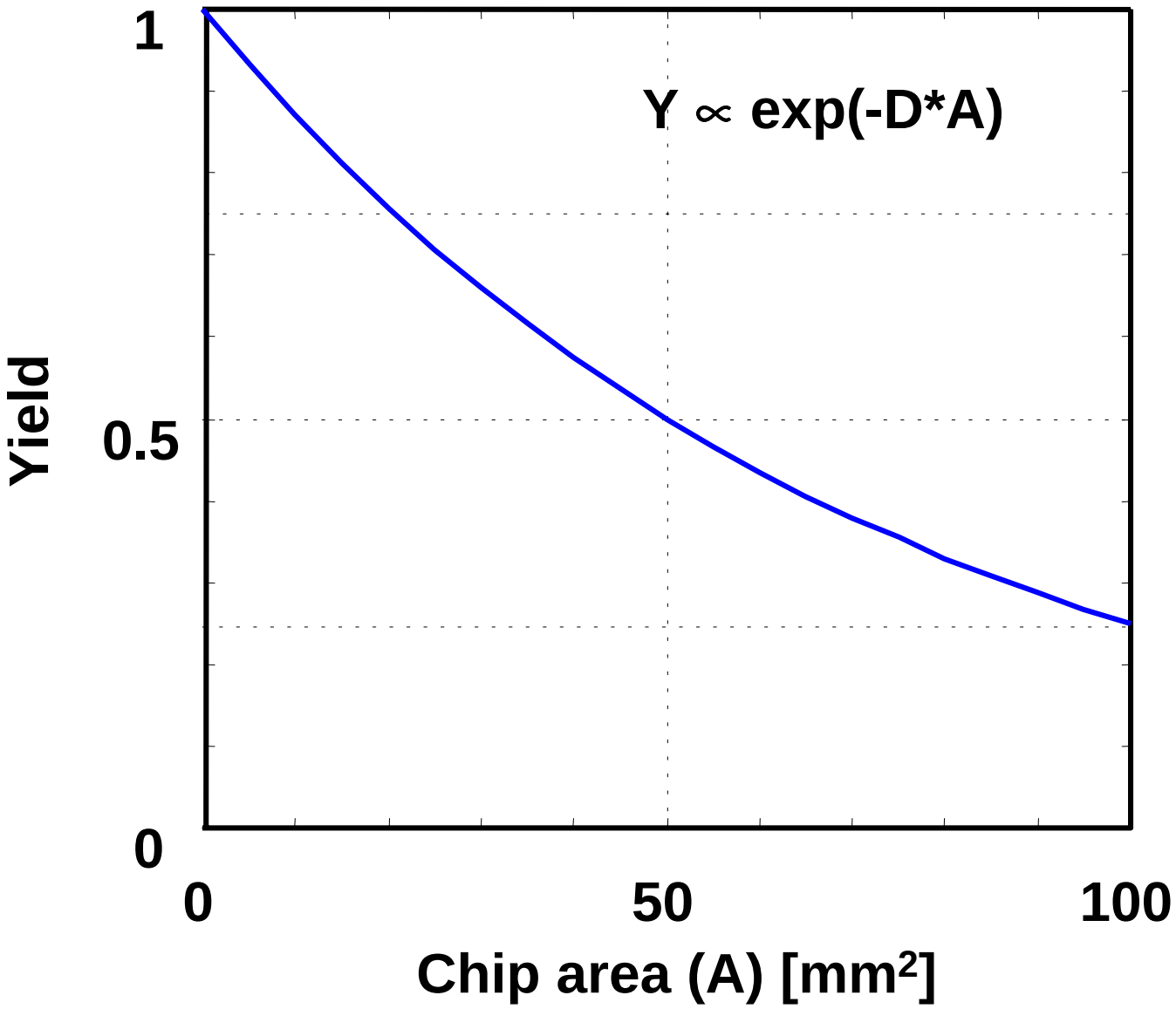
"Having said all that, there are cases where we agree [about putting a system on a package]," he said. "There is a substrategy of ours called integrated disintegration, which means there are analog functions you can pull off the chip because they are such a tiny portion of the overall chip, and yet they are the most difficult thing to port to the next-generation [process] technology."

IBM's Kelly said that "SoC integration has to be done se-

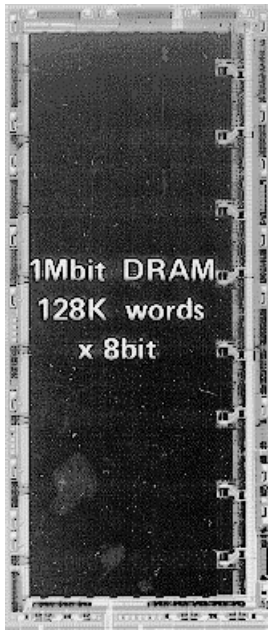
Issues in System-on-Chip

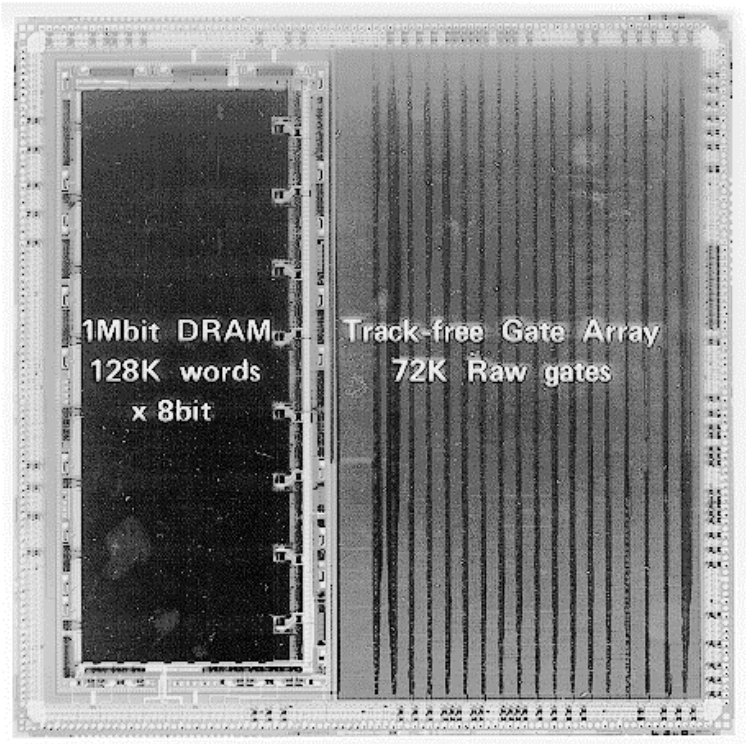
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

Yield



DRAM embedding





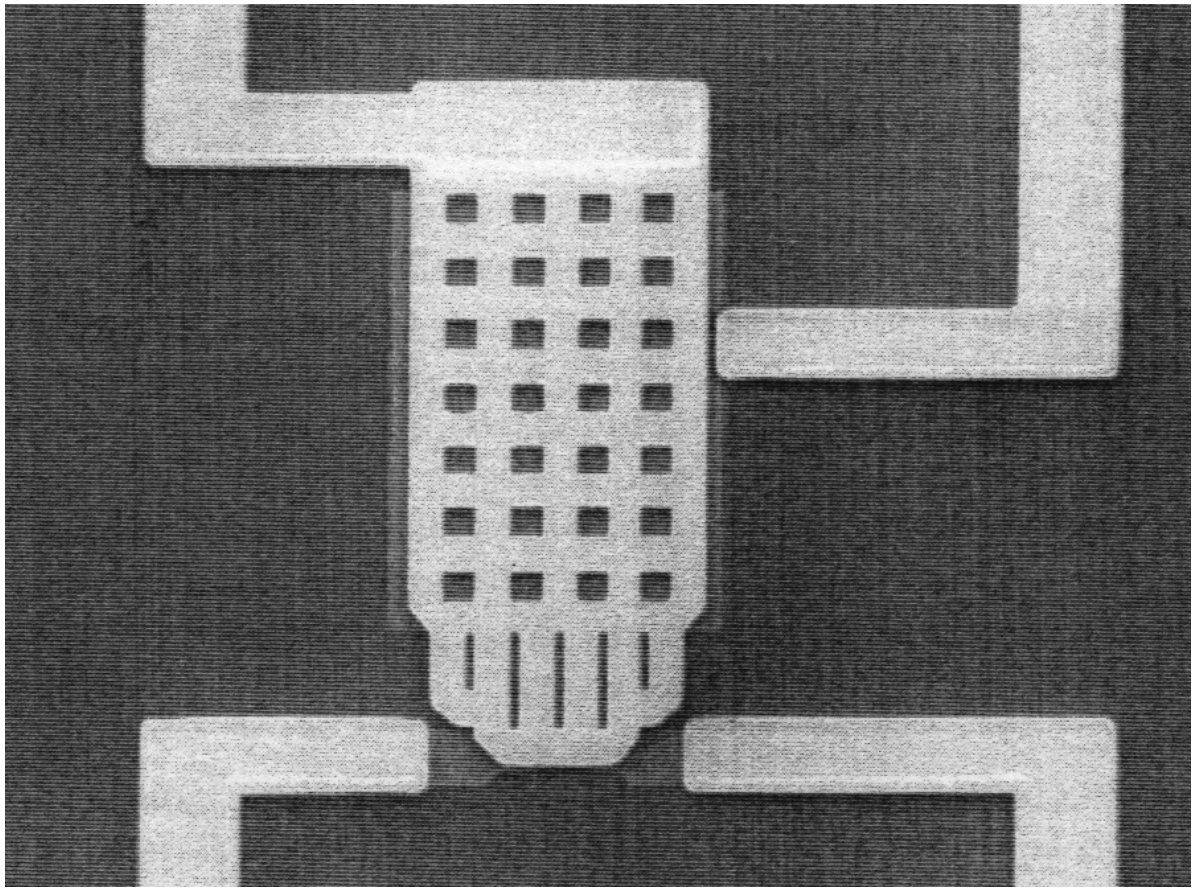
DRAM **Processor** **System LSI**

K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- **Two orders of magnitude improvement in bandwidth and power**

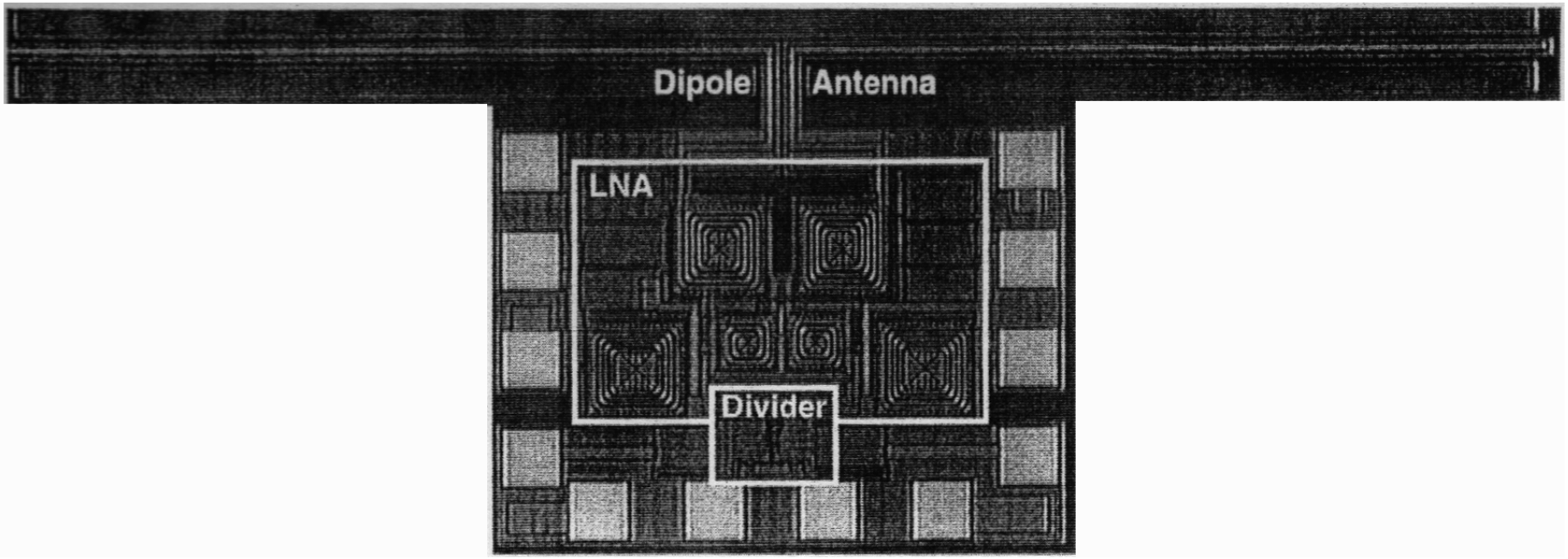
BUT EXPENSIVE!

Micro-machined mechanical switch



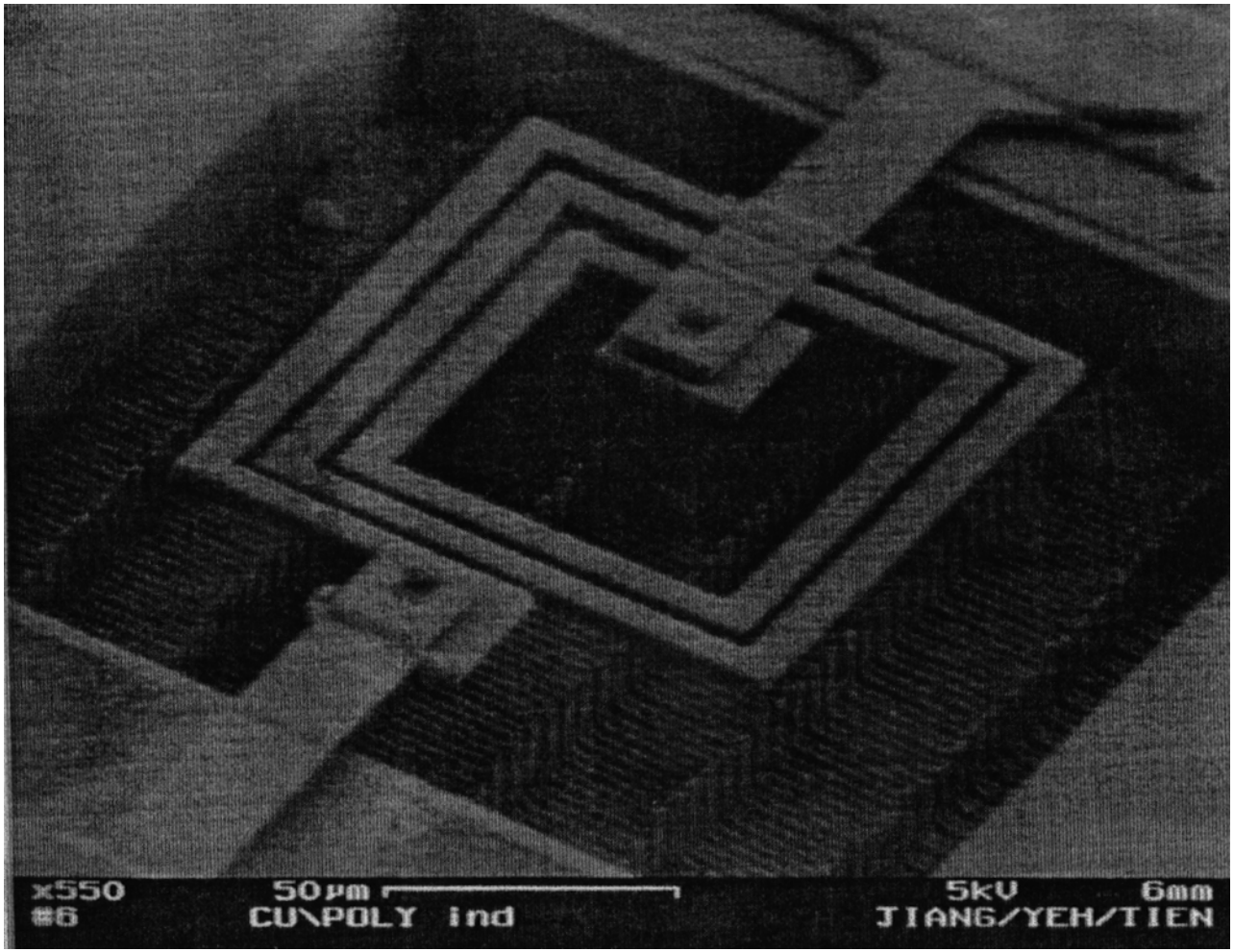
G.Weinberger, “The New Millennium: Wireless Technologies for a Truly Mobile Society,” ISSCC, pp.20-24, Feb. 2000.

Antenna on chip



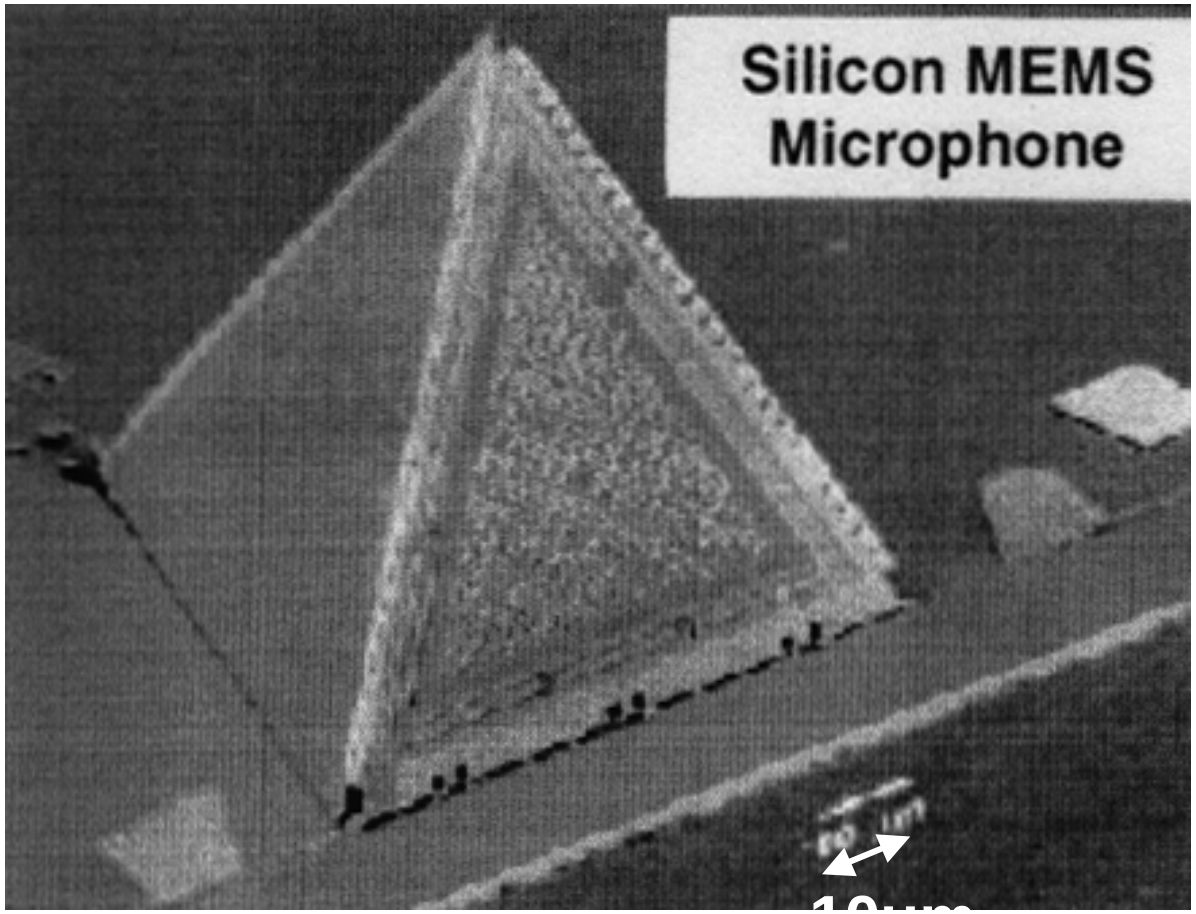
B.Floyd, K.Kim and Kenneth, “Wireless Interconnection in a CMOS IC with Integrated Antennas,” ISSCC, pp.328-329, Feb. 2000.

Suspended spiral inductor



H.Jiang J.Yeh, Y.Wang, N.Tien, “Electromagneticallt Shielded High-Q CMOS-Compatible Copper Inductor,” ISSCC, pp.330-331, Feb. 2000.

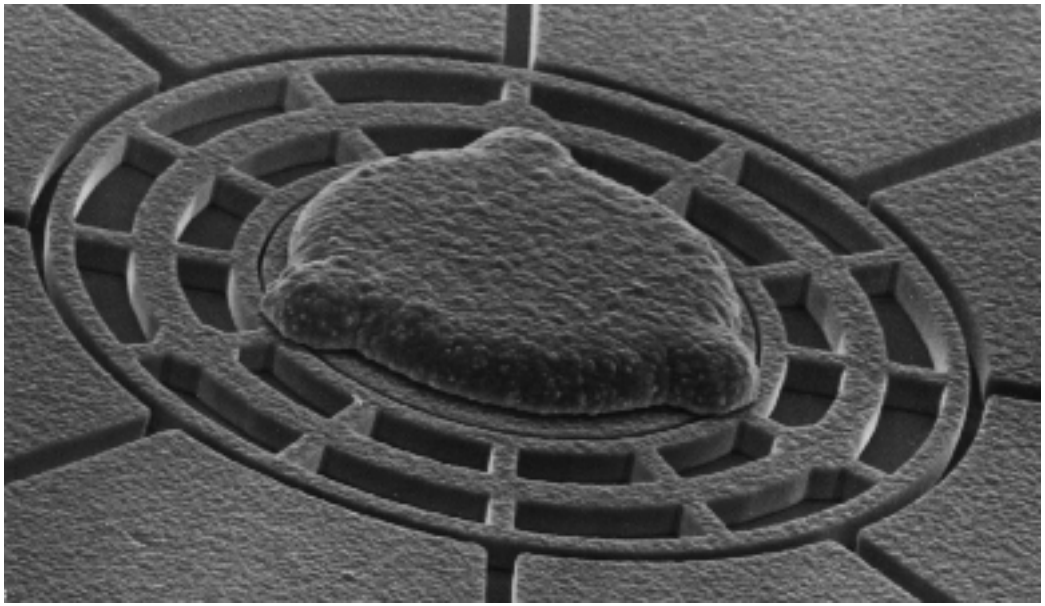
Silicon MEMS microphone



Will soon exceed the performance of the best commercial microphones, yet be inexpensive and potentially integrated with on-chip electronics.

M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

Silicon MEMS motor



マイクロマシン技術で作った0.1ミリのモーター
東京大学、生産技術研究所、藤田博之教授提供

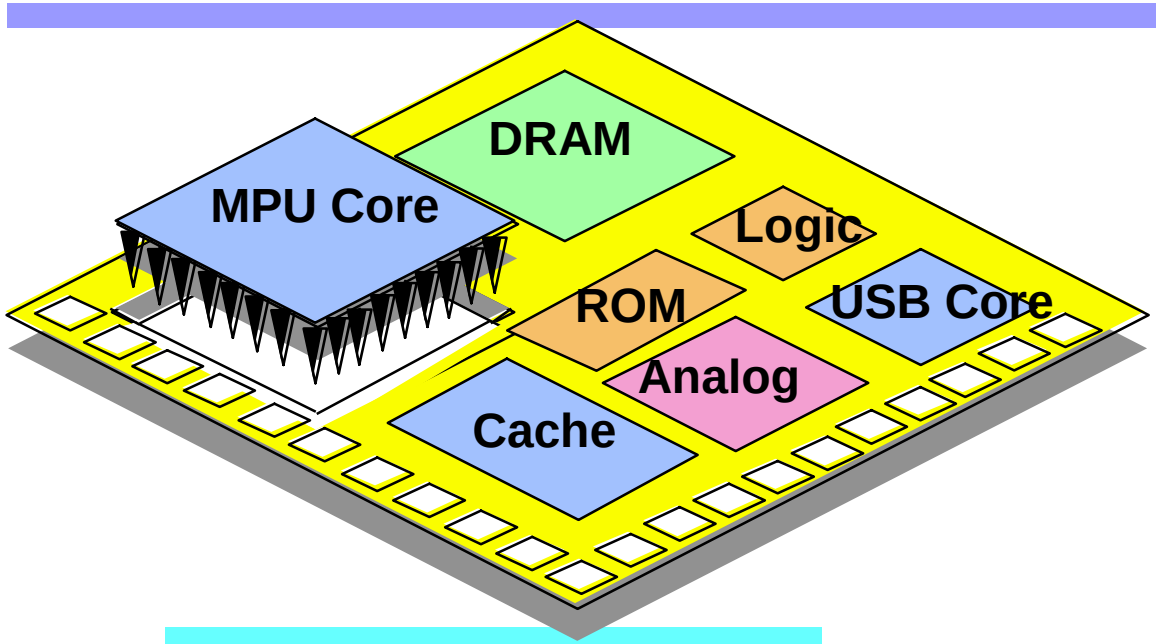
マイクロマシン

もう一つの重要な技術がシリコンを使ったマイクロマシン技術である。このようなマイクロマシン技術で作られた0.1ミリ径のモーターである。このようなモーターとコントロールチップを一緒にできれば、血管の中を掃除するチップなどが実現できる。また、シリコン・イメージセンサと組み合わせて、どの方角でも検査できる血管や臓器のワイヤレス内視鏡などが実現できる。モーター以外でもマイクロマシン技術で作られた0.1ミリ径のマイクロフォンなども発表されている。大変特性が良く、耳に埋め込む人工内耳などにも応用できそうだ。

マイクロマシン技術でタービンエンジンを作ると、コインのサイズ以下のタービンエンジンが実現できる。それを使って、少量のガソリンで発電する携帯発電機の研究が始まっている。このような研究が成功すれば、電池のいらない携帯機器ができる可能性がある。ただし、ライターのように燃料を供給する必要がある。一方、全く燃料の不要な電源の研究もなされている。これもマイクロマシン技術を使うが、機械振動を電気に変えて電源とするものである。例えば、加工機械などは常に振動しているので、その振動エネルギーを電気エネルギーに変えて使おうという発想だ。このように環境に存在するエネルギーだけで動く環境エネルギー動作の超低電力チップも研究され始めた。エネルギー問題に一石を投ずることになるだろう。

日経産業新聞（桜井貴康）

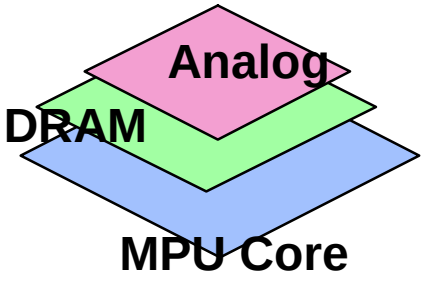
Stacked chips



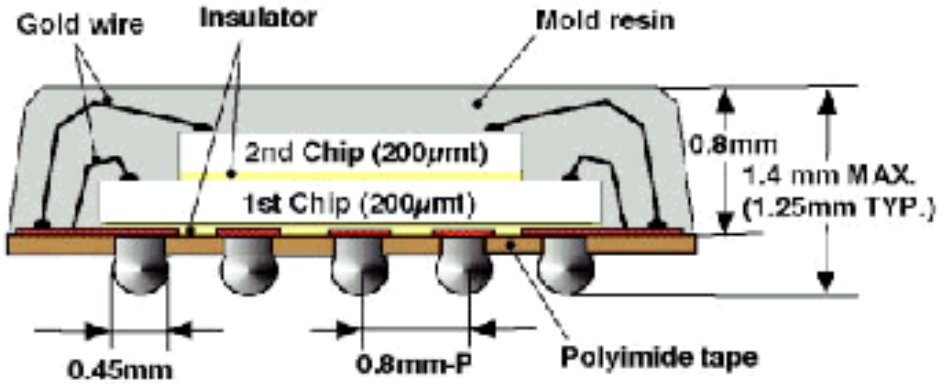
System on a chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation

- Heat dissipation is an issue



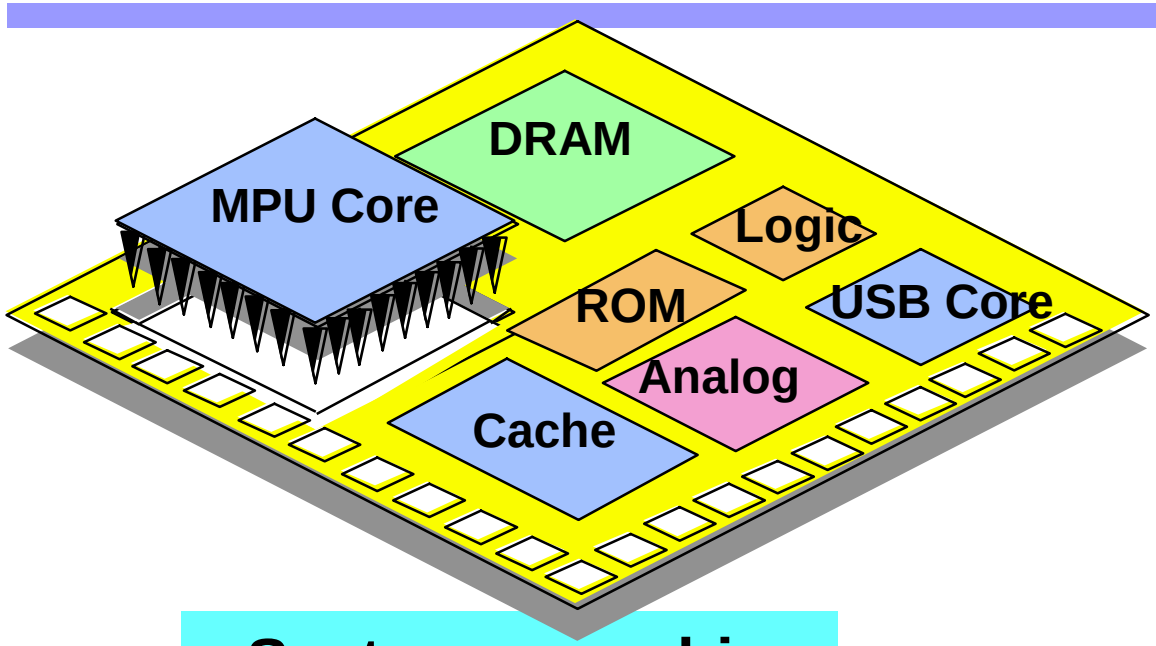
Stacked chips



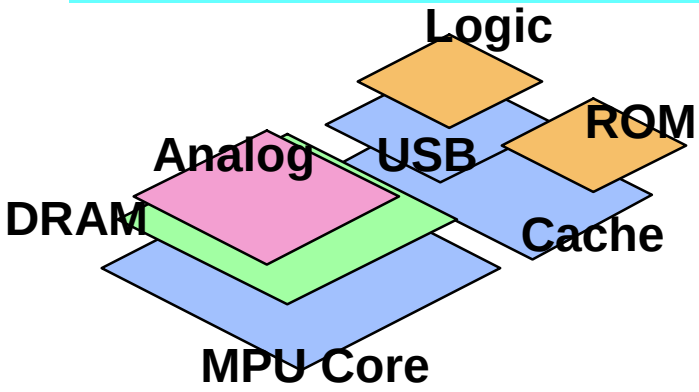
藤田他、「スタックドCSP技術」、シャープ技法、1998.8

T.Sakurai

3-Dimensional assembly



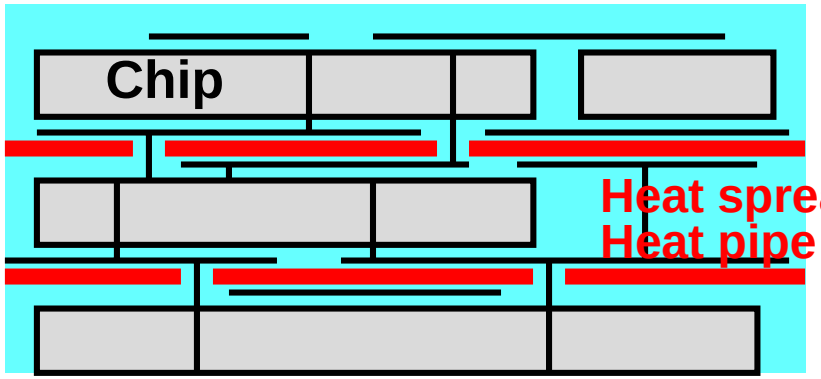
System on a chip



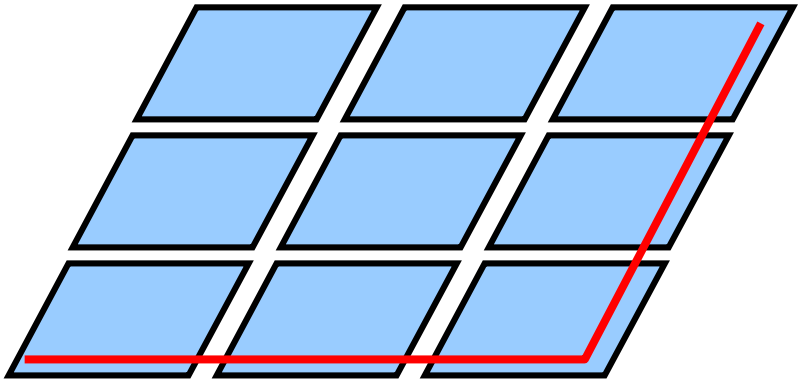
3-D assembly

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

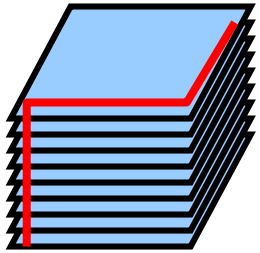
- Heat dissipation is an issue



Shorter interconnect in 3-D assembly



System on a chip



3-D assembly

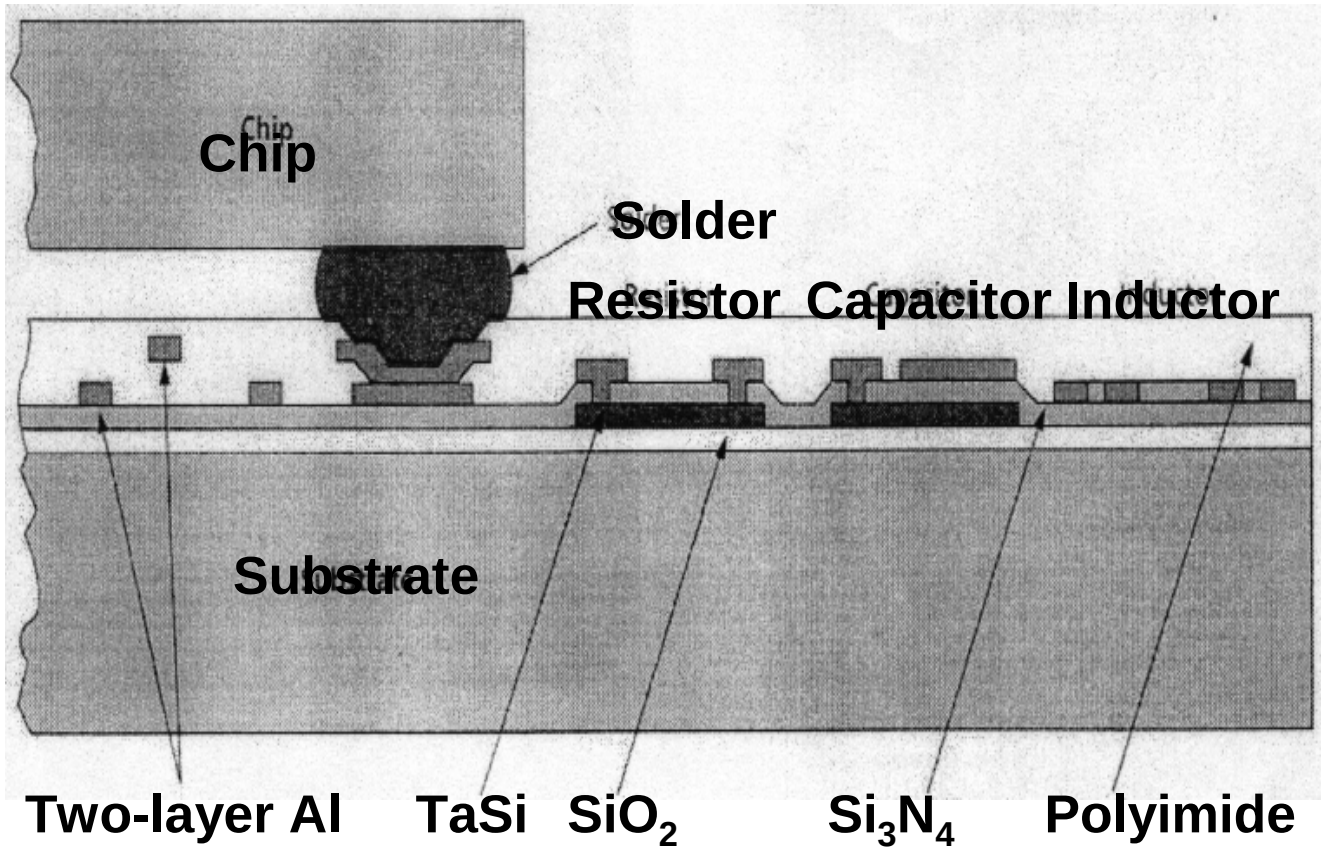
$$\frac{\#\textit{of devices in d}\,(3D)}{\#\textit{of devices in d}\,(2D)} = \frac{1}{3}\left(2\frac{d}{h}+\frac{h}{d}\right)$$

$$\approx \frac{2}{3}\left(\#\textit{of stacked chips in d}\right)$$

d: Manhattan distance

h: Height between chips

System-in-Package (SIP)

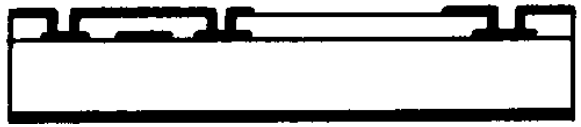


K.L.Tai, "System-In-Package (SIP): Challenges and Opportunities," ASPDAC, pp.191-196, Jan. 2000

ビルドアップ基板

両面銅張積層板→第１信号回路形成

第１絶縁層塗布→ファトバイアホール形成



銅めっき→第２信号回路形成

第２絶縁層塗布、バイアホール形成

銅めっき→電源層形成

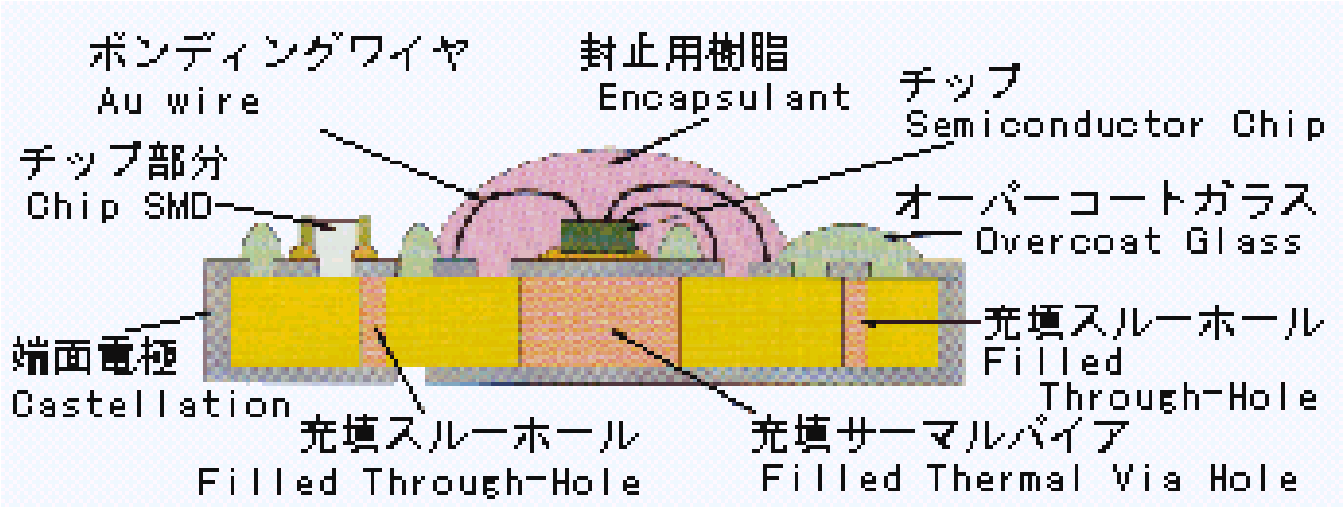
はんだ保護膜塗布

日本ビクター，10層のビルドアップMCM基板を展示，ライン／スペースは30μm／30μm
http://ne.nikkeibp.co.jp/NE/1998/eleshow98/42556.htm

出典：プリント回路技術便覧、プリント回路学会編、日刊工業新聞社

T.Sakurai

Thermal via

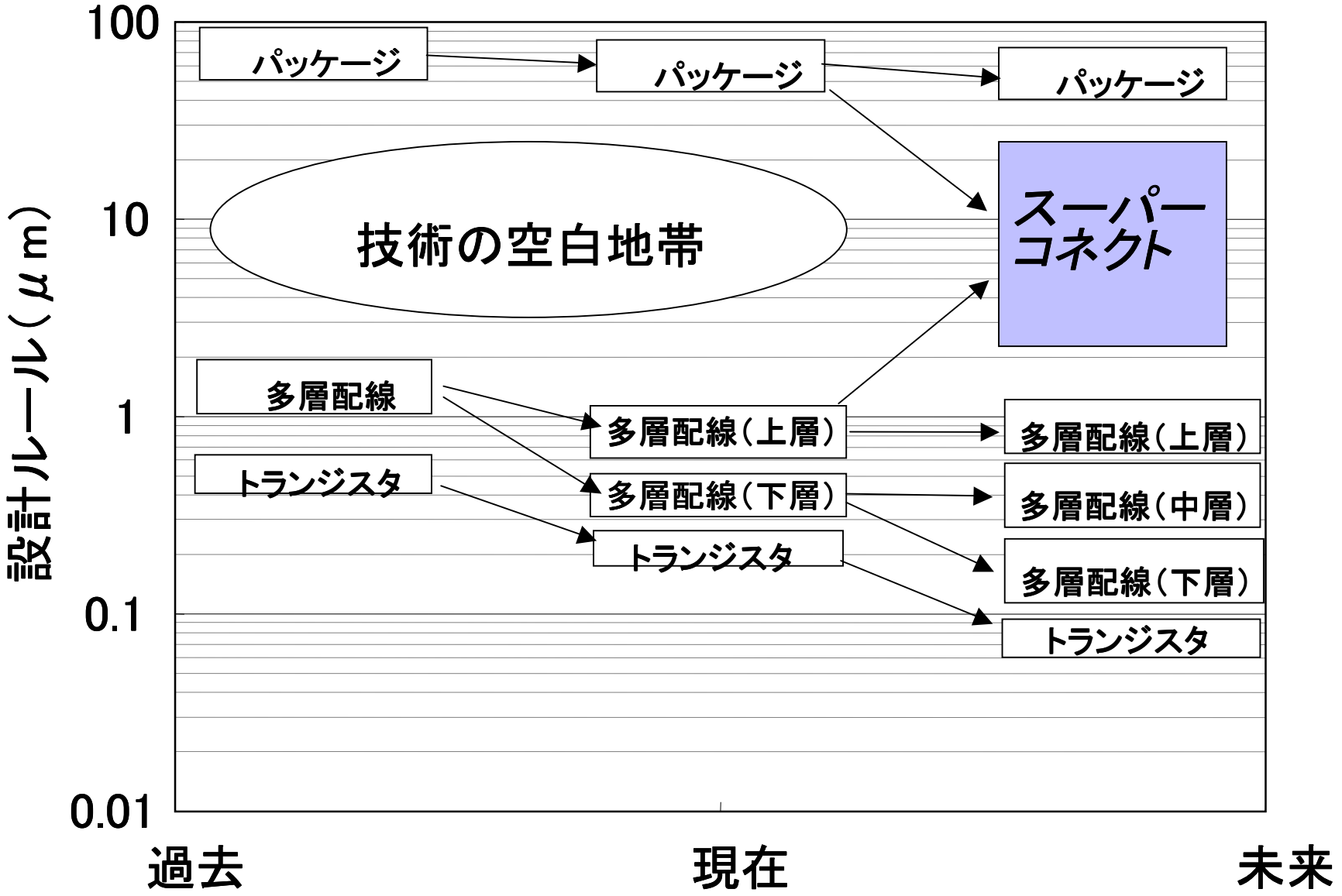


ミヨシ電子工業：http://www.elec.co.jp/1_kaisya/Page1410.html

System-in-Packageの課題

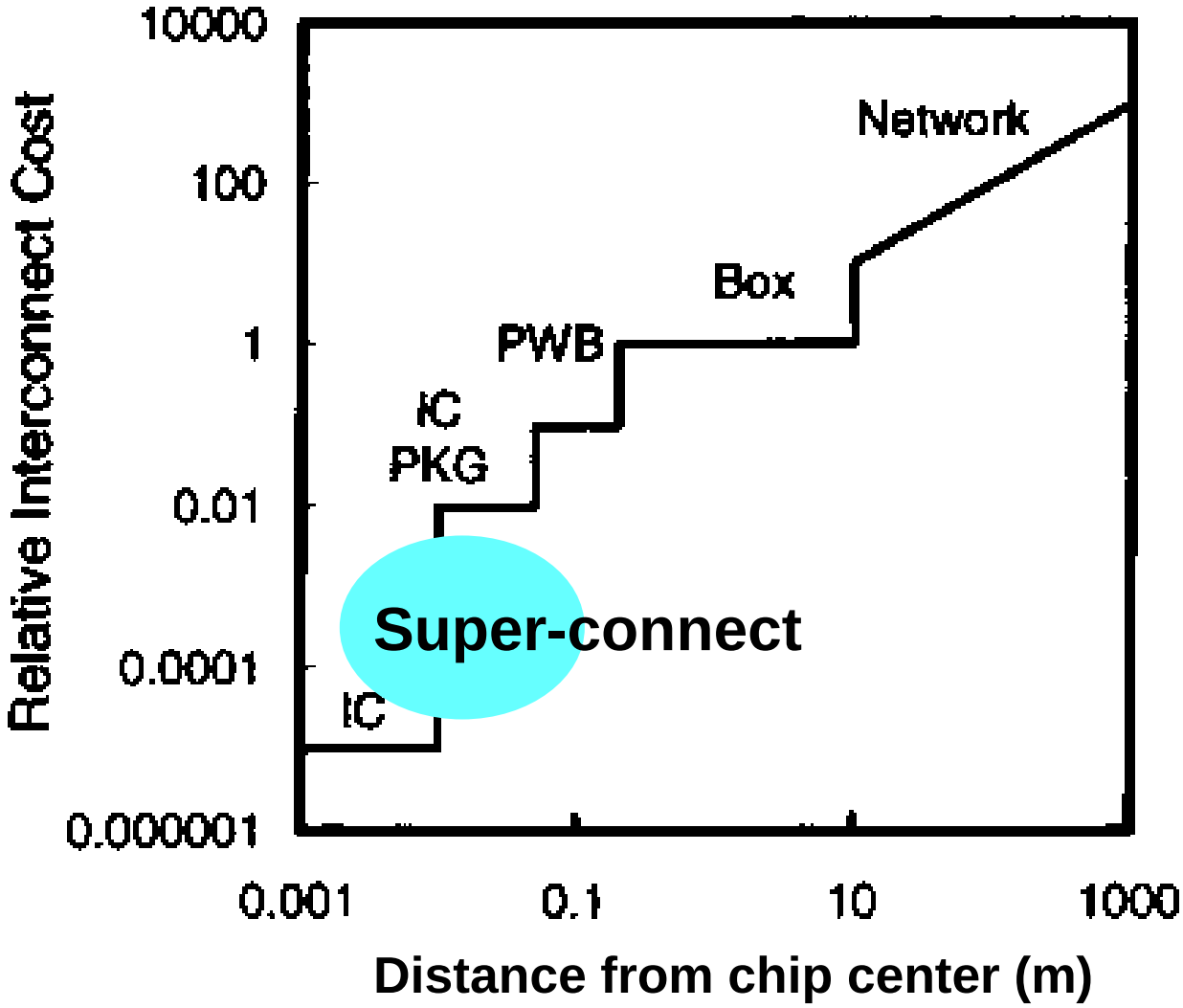
- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

スーパーコネクト



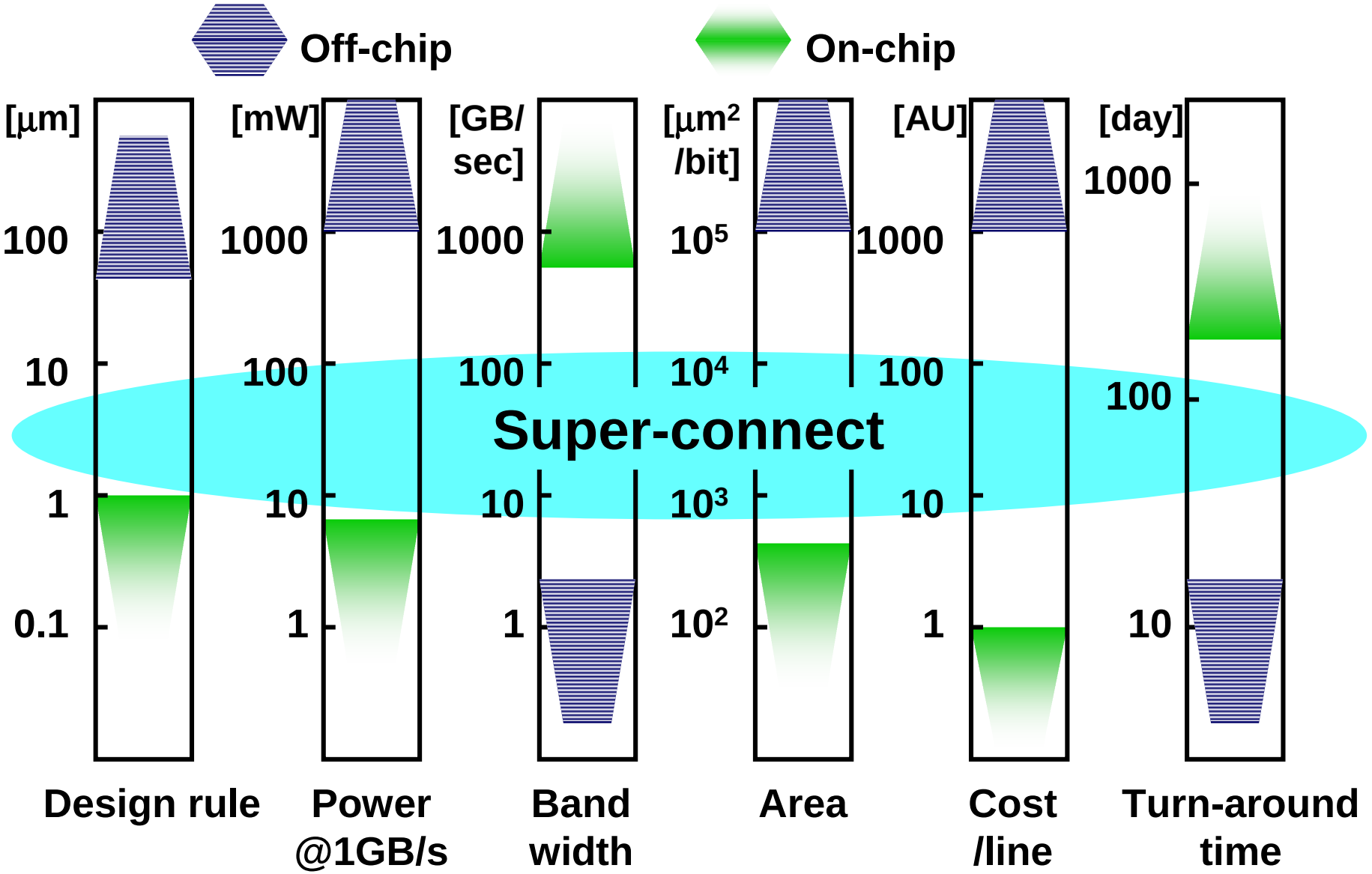
出典：日経マイクロデバイス

Cost of interconnect



M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

Super-connect



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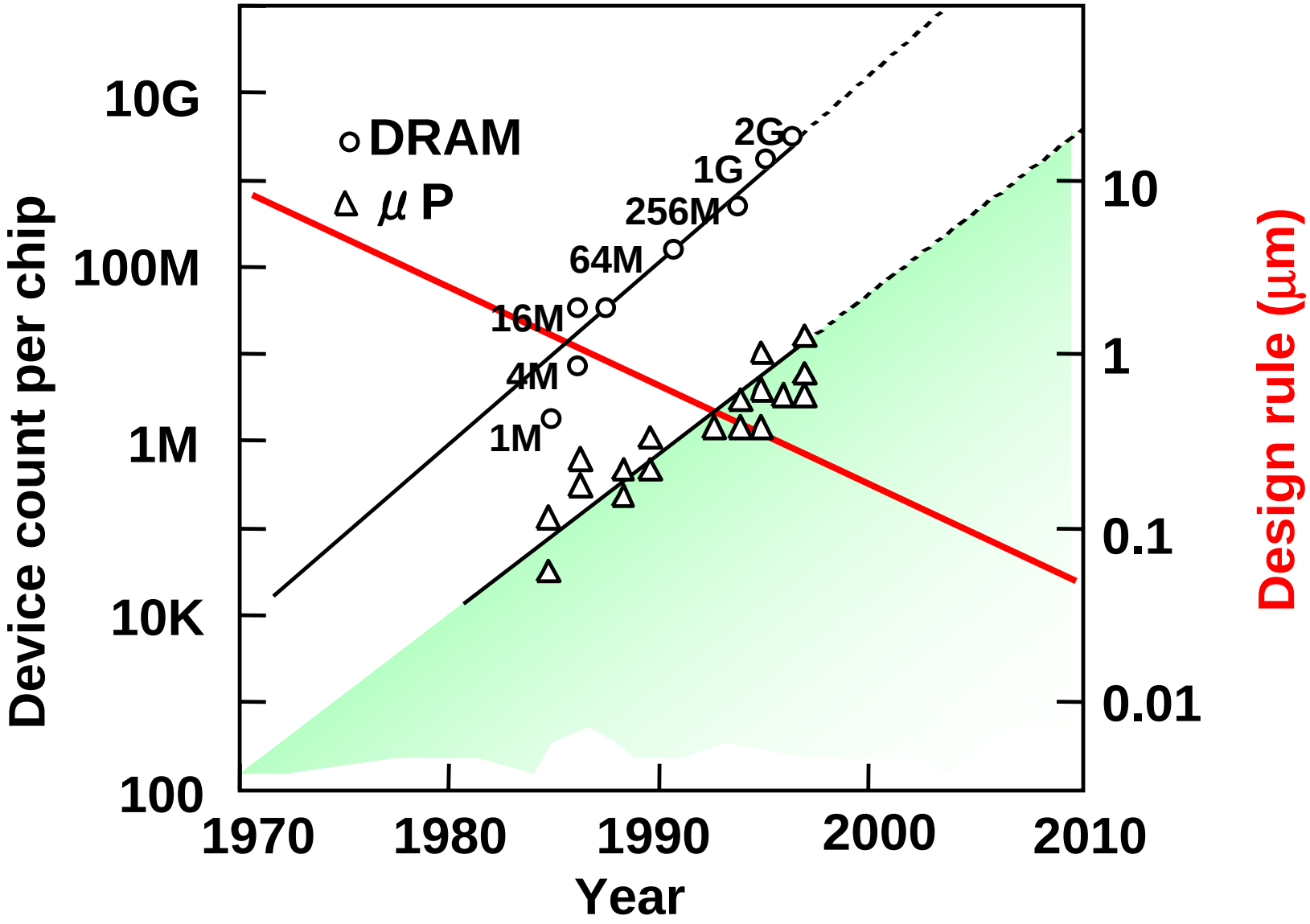
Moore's Law



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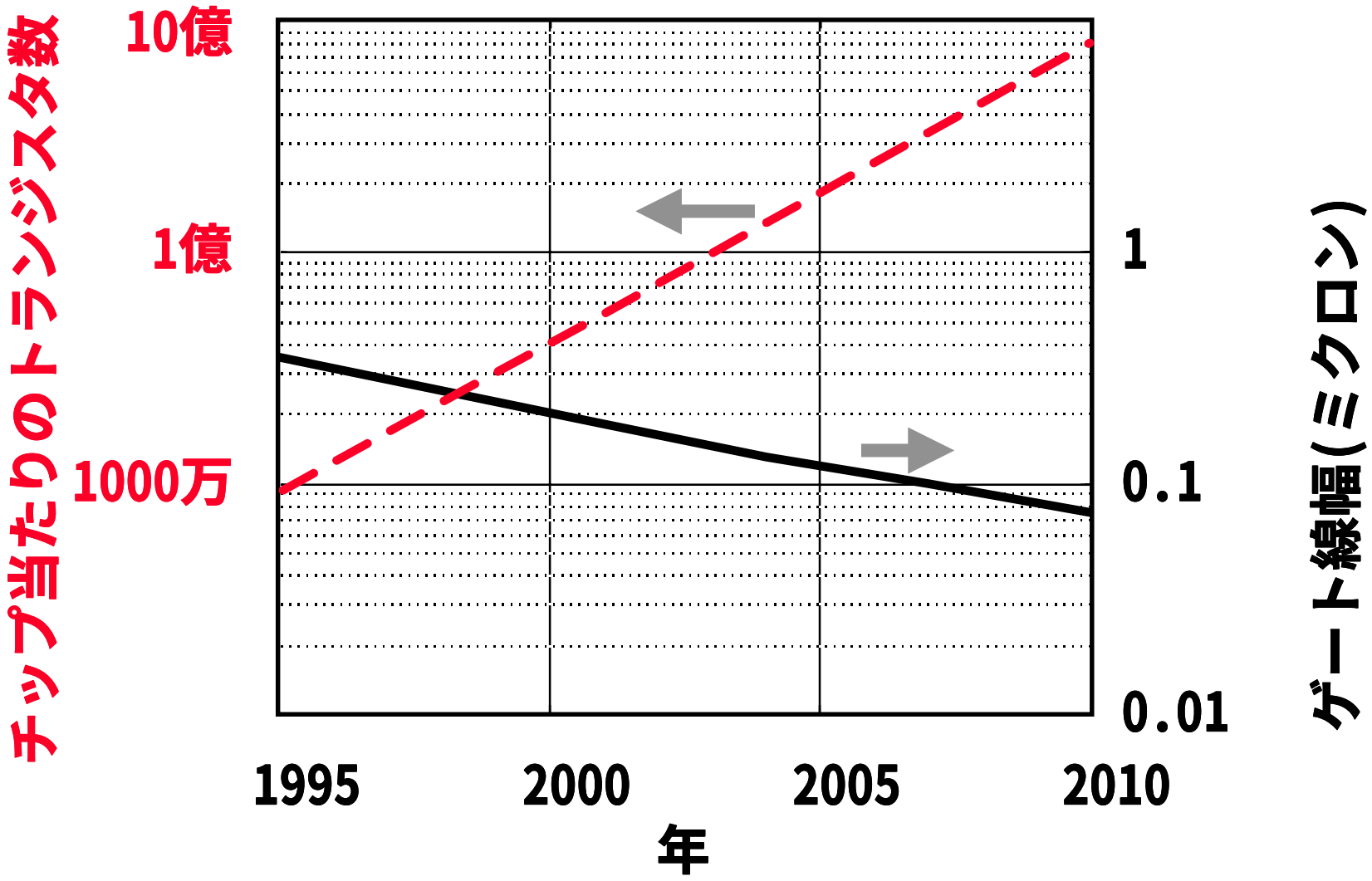
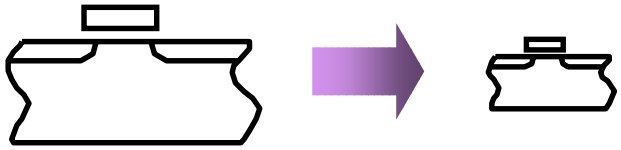
微細加工技術の進展


チップ当たりのトランジスタ数
10億
1億
1000万
1
0.1
0.01
ゲート線幅(ミクロン)
1995
2000
2005
2010
年

Scaling Law

Transistor		Numbers are exponent to k (k^n)			
Voltage	[V]	-1			
Tr. size	[x]	-1			
Oxide thickness	[t]	-1			
Current	[I~$V^{1.3}$/t]	- 0.3			
Tr. capacitance	[Cg~x^2/t]	-1			
Tr. delay	[Tg~CgV/I]	-1.7			
Tr. power	**[Pg~CgV^2/Tg]**	-1.3			
Tr. power density	**[p~Pg/x^2]**	0.7			
Tr. desity	**[n~ 1/x^2]**	2			
Interconnection		Local	Middle	Global	VDD/VSS
Length	[L]	-1	- 0.5	0	0
Width	[W]	-1	- 0.5	0	1
Thickness	[T]	-1	- 0.5	0	1
Height	[H]	-1	- 0.5	0	0
Resistance	[R_m~L/W/T]	1	0.5	0	-1
Capacitance	[C_m~LW/H]	-1	- 0.5	0	1
RC Delay/Tr. delay	**[T_m~R_mC_m/Tg]**	1.7	1.7	1.7	–
Current density	**[J~pLW/V/W/T]**	–	–	–	0.7
Dc Noise	**[SN_{dc}~JWLR_m/V]**	–	–	–	1.7

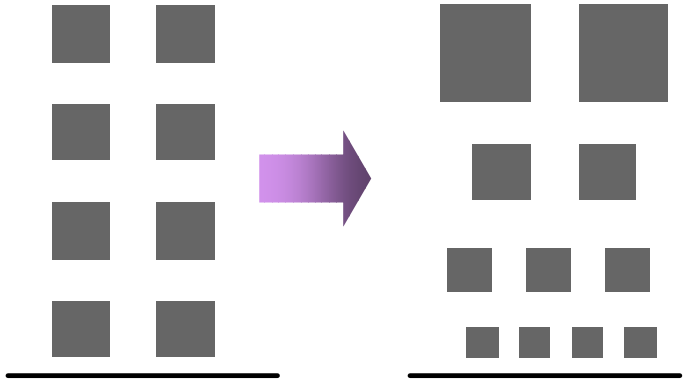


K=2

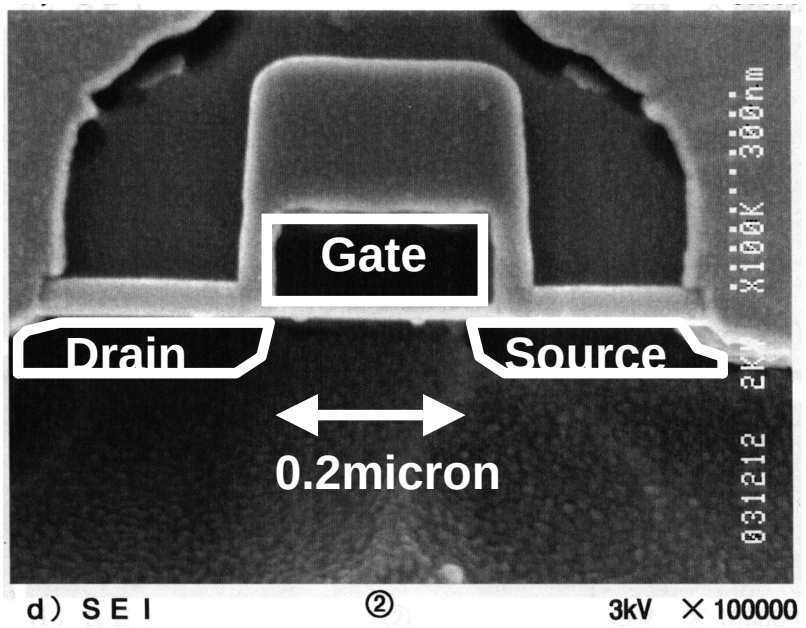
$$I_{ds} = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)\frac{(V_{gs}-V_t)}{2}^{\alpha} \sim [V^{\alpha}/t]$$

$$\alpha = 1.3$$

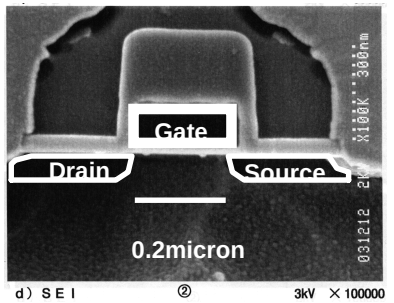
T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no,2, pp.584-594, Apr. 1990.



Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

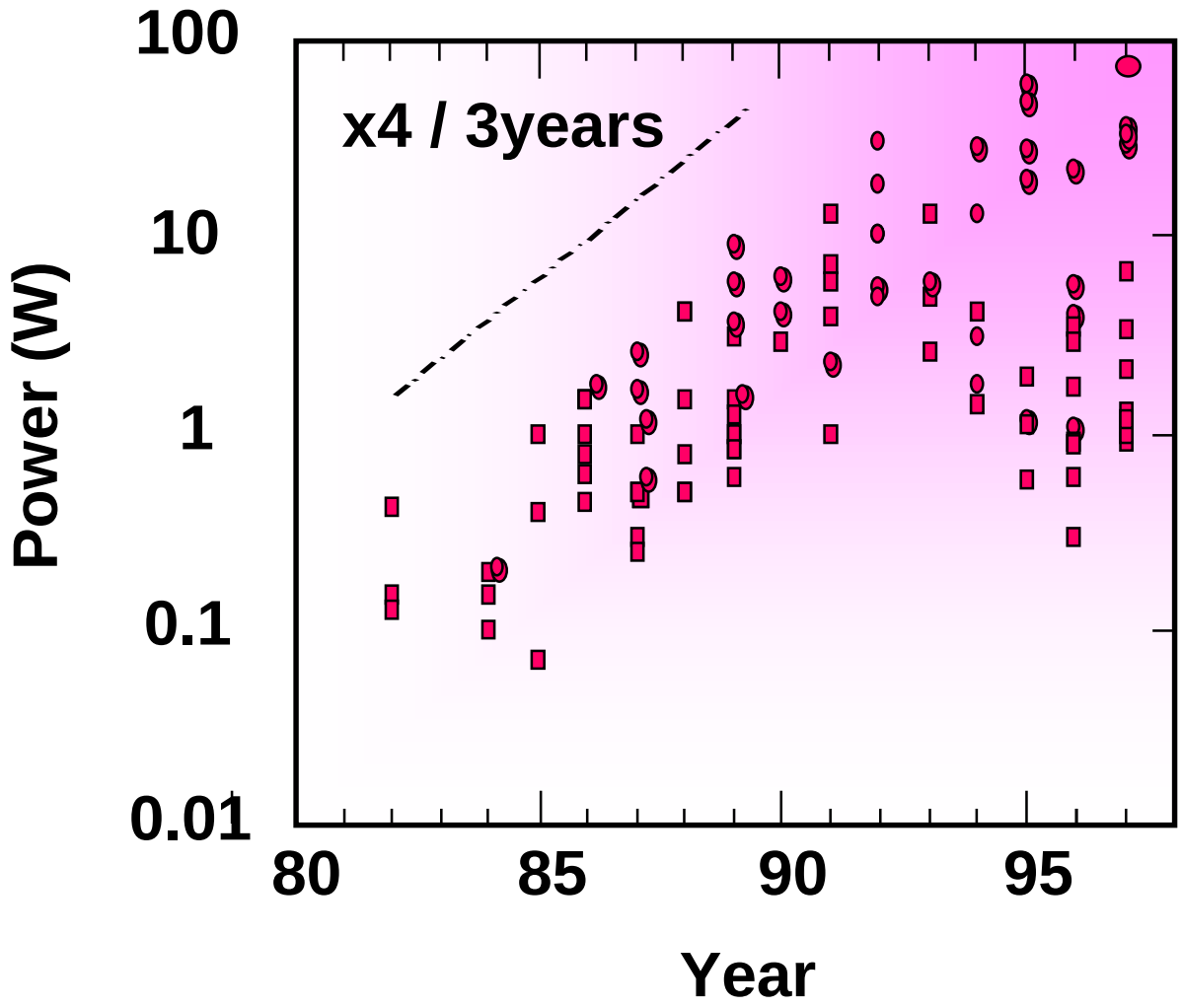
T.Sakurai

Three crises in VLSI designs

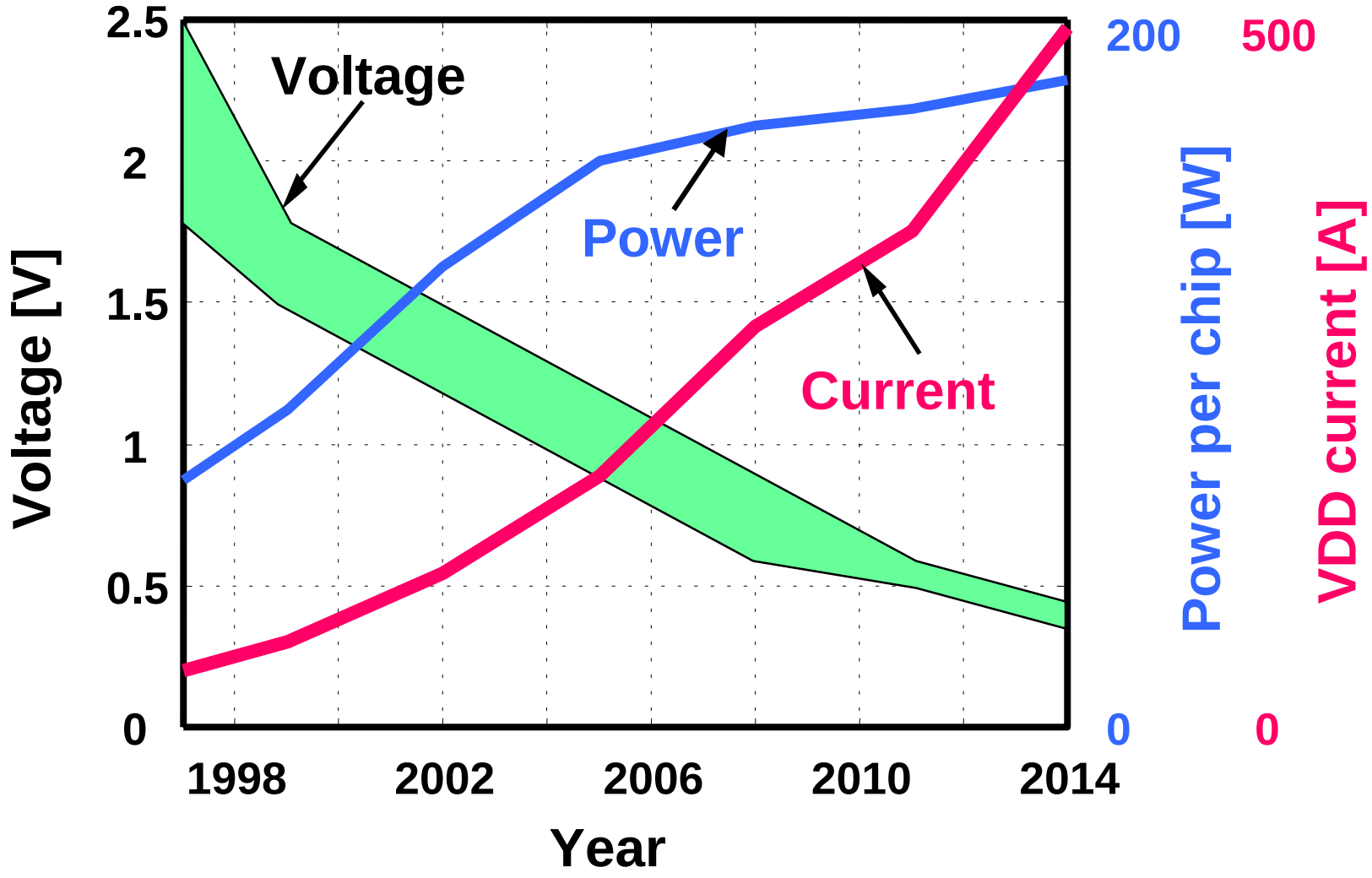
- Power crisis
- Interconnection crisis
- Complexity crisis

Ever Increasing VLSI Power

(Power consumption of processors published in ISSCC)



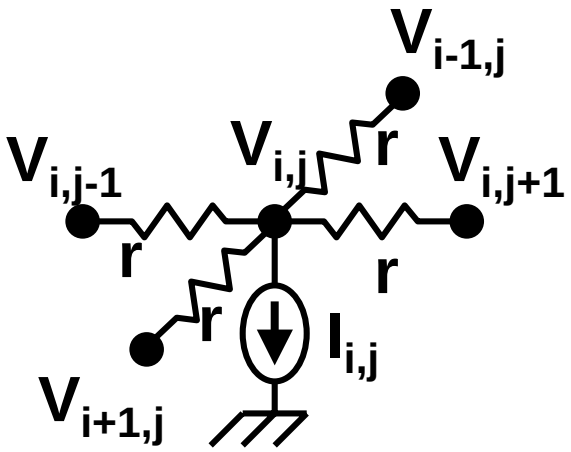
VDD, Power and Current Trend



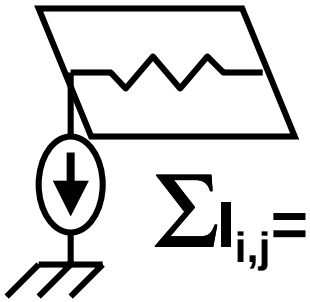
International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

T.Sakurai

IR Drop

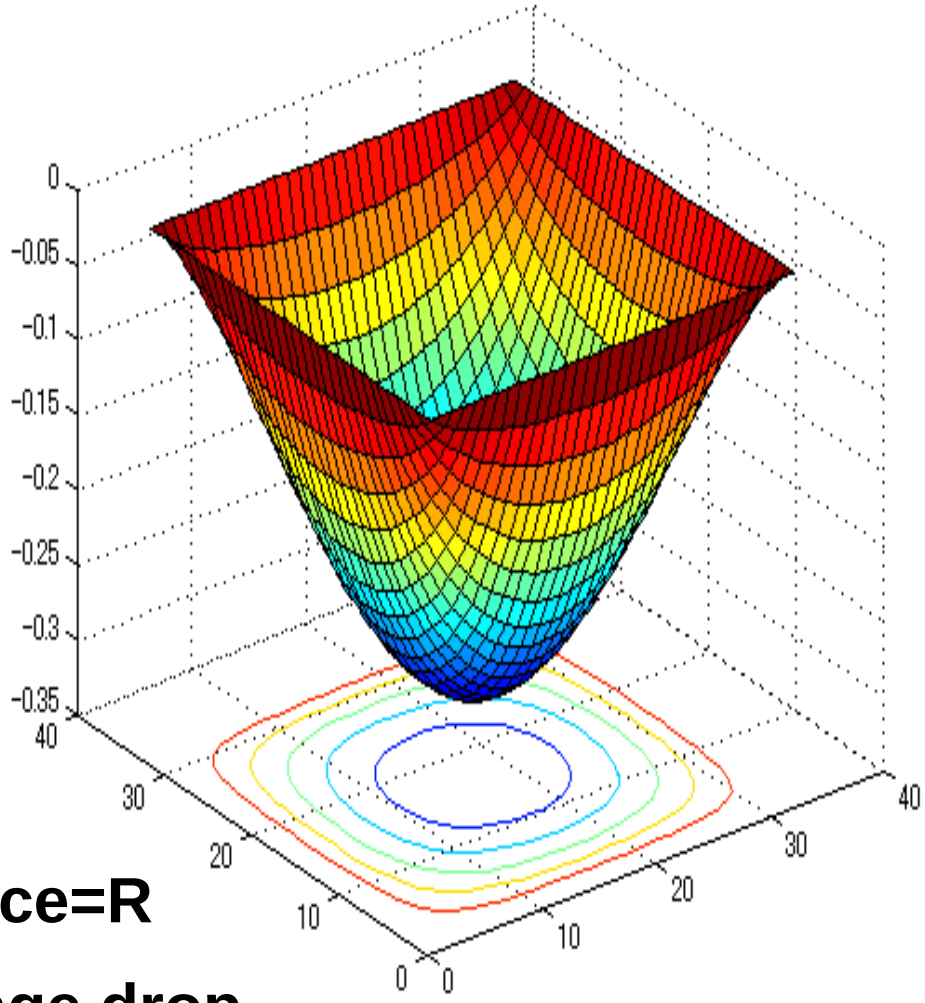


$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\,I_{i,j}$$

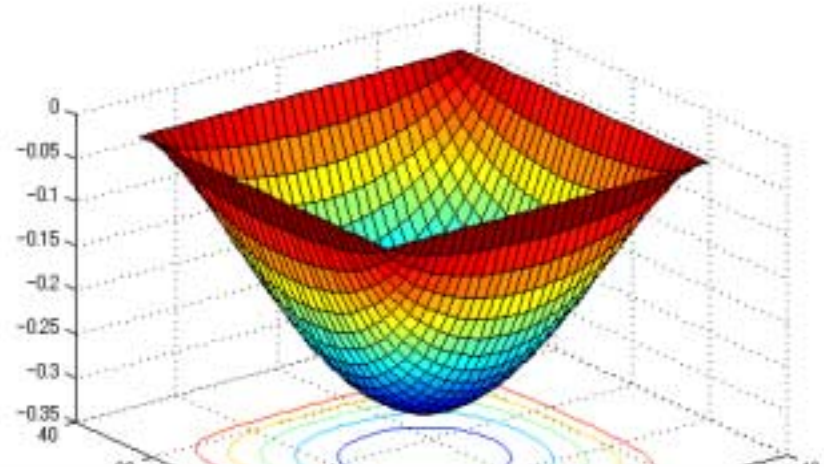


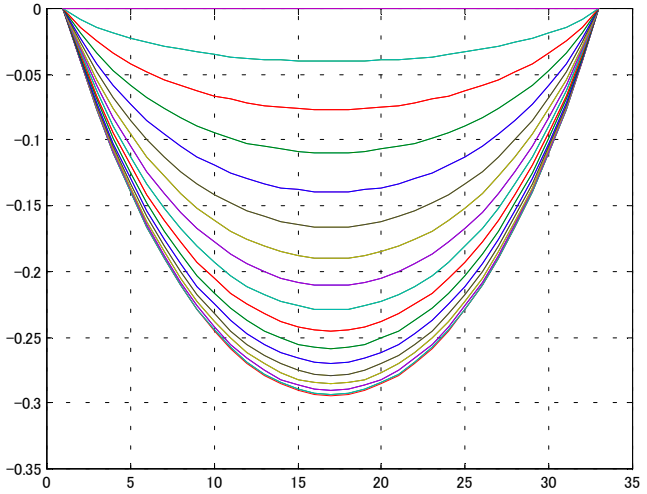
$\sum I_{i,j}=I$, Sheet resistance=R

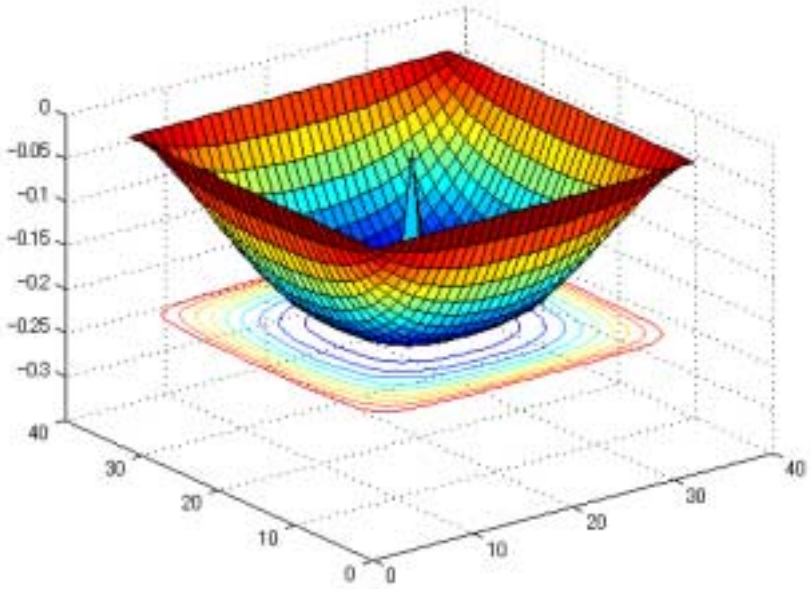
Take IR as unity voltage drop

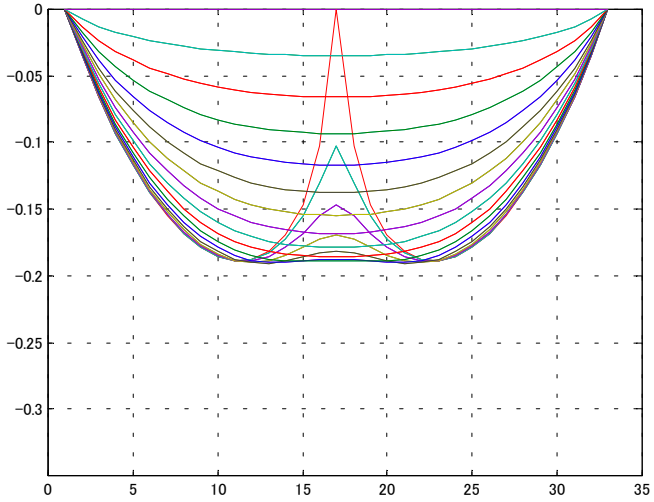


IR Drop


0
−0.05
−0.1
−0.15
−0.2
−0.25
−0.3
−0.35
40


0
−0.05
−0.1
−0.15
−0.2
−0.25
−0.3
−0.35
0
5
10
15
20
25
30
35

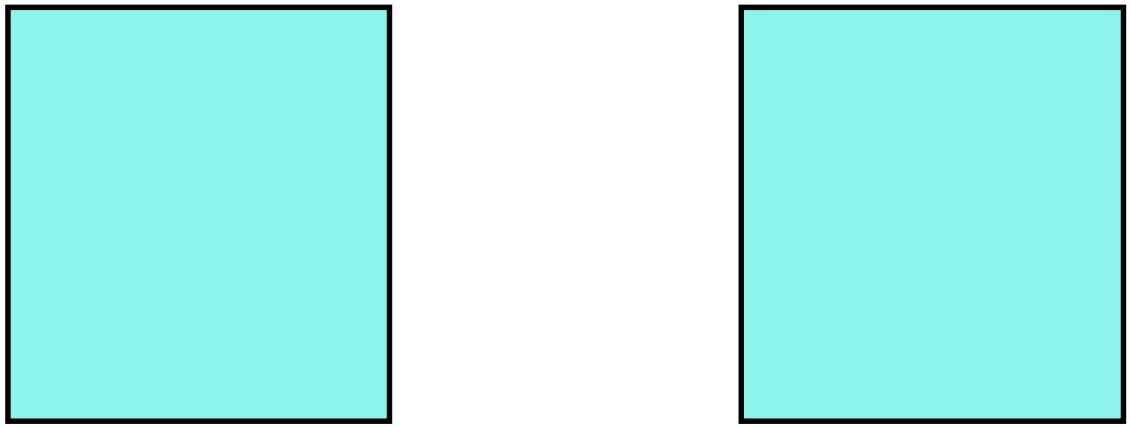

0
−0.05
−0.1
−0.15
−0.2
−0.25
−0.3
40
30
20
10
0
0
10
20
30
40


0
−0.05
−0.1
−0.15
−0.2
−0.25
−0.3
0
5
10
15
20
25
30
35

Interconnect Cross-Section and Noise

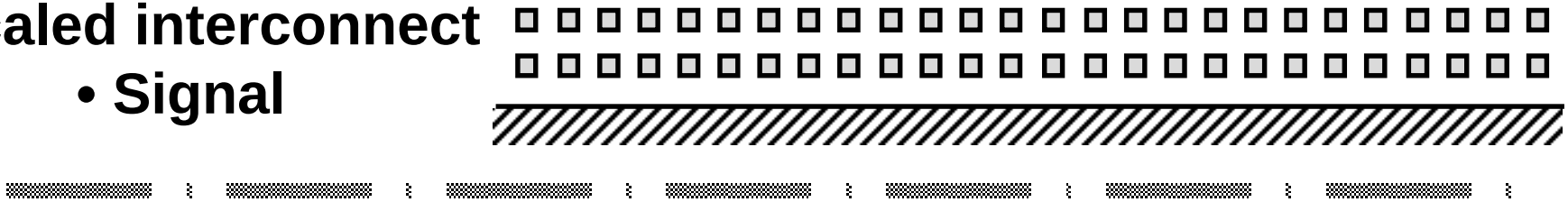
Unscaled / anti-scaled

- **Clock**
- **Long bus**
- **Power supply**



Scaled interconnect

- **Signal**

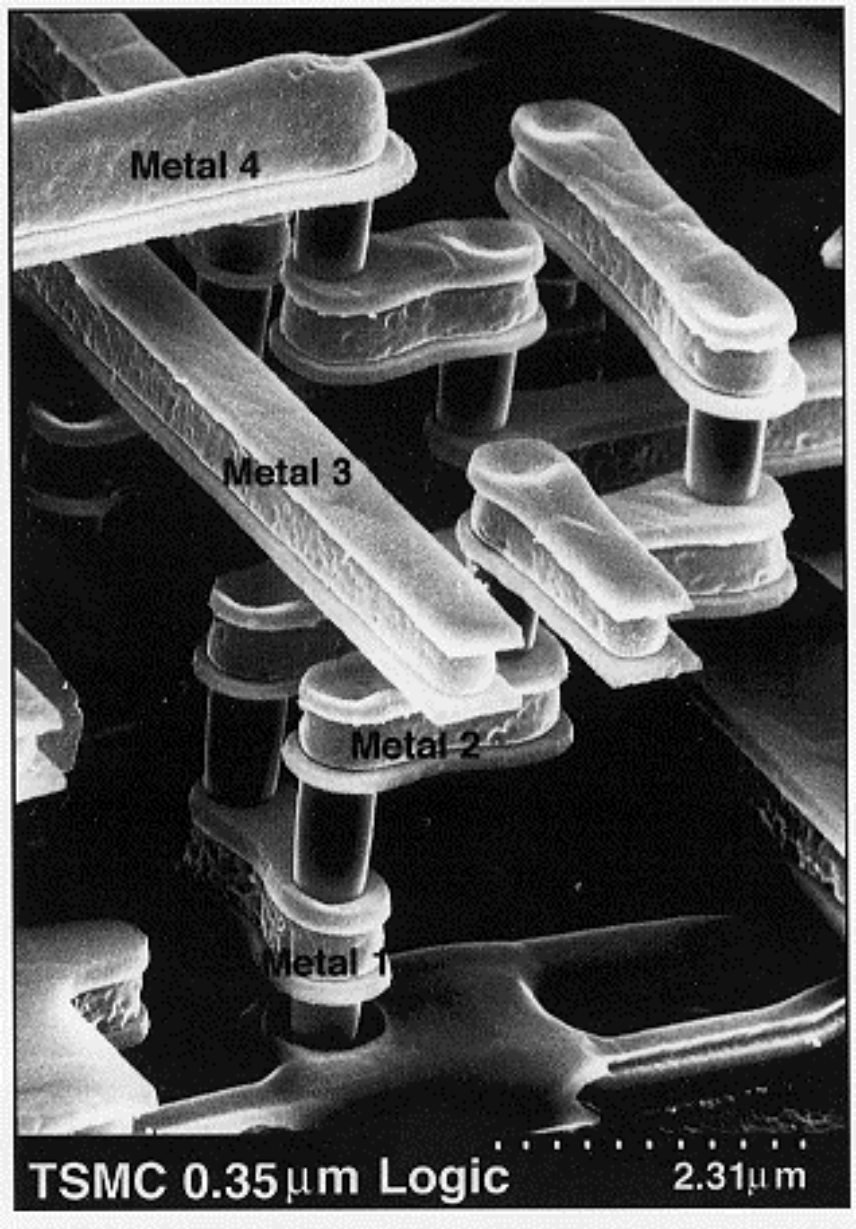


1V 20W -> 20A current

2% noise on VDD & VSS -> ~0.02V / 20A -> ~10μm thick Cu

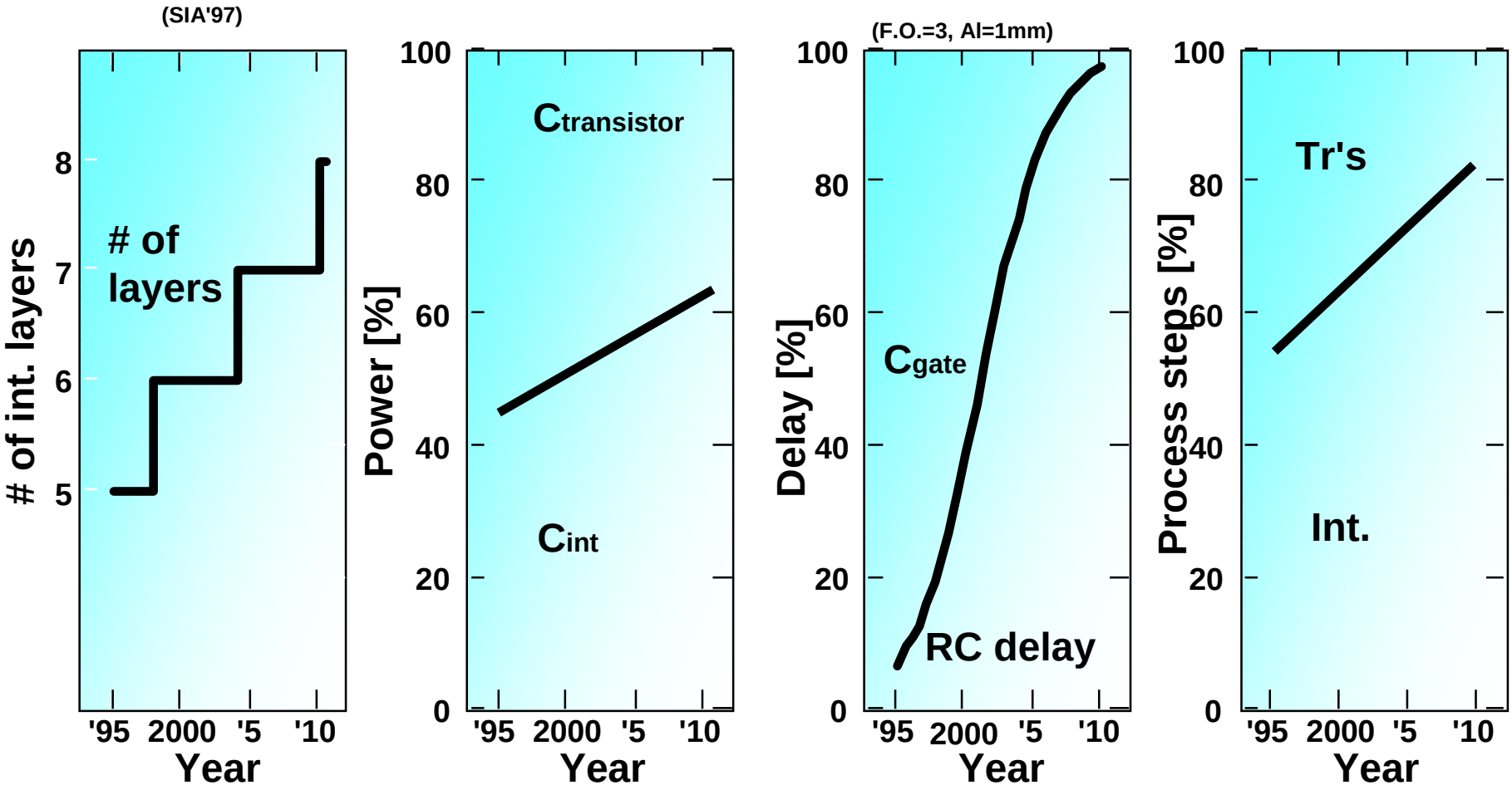
Thick layer on LSI, area pad, package are co-designed.

Complex interconnect



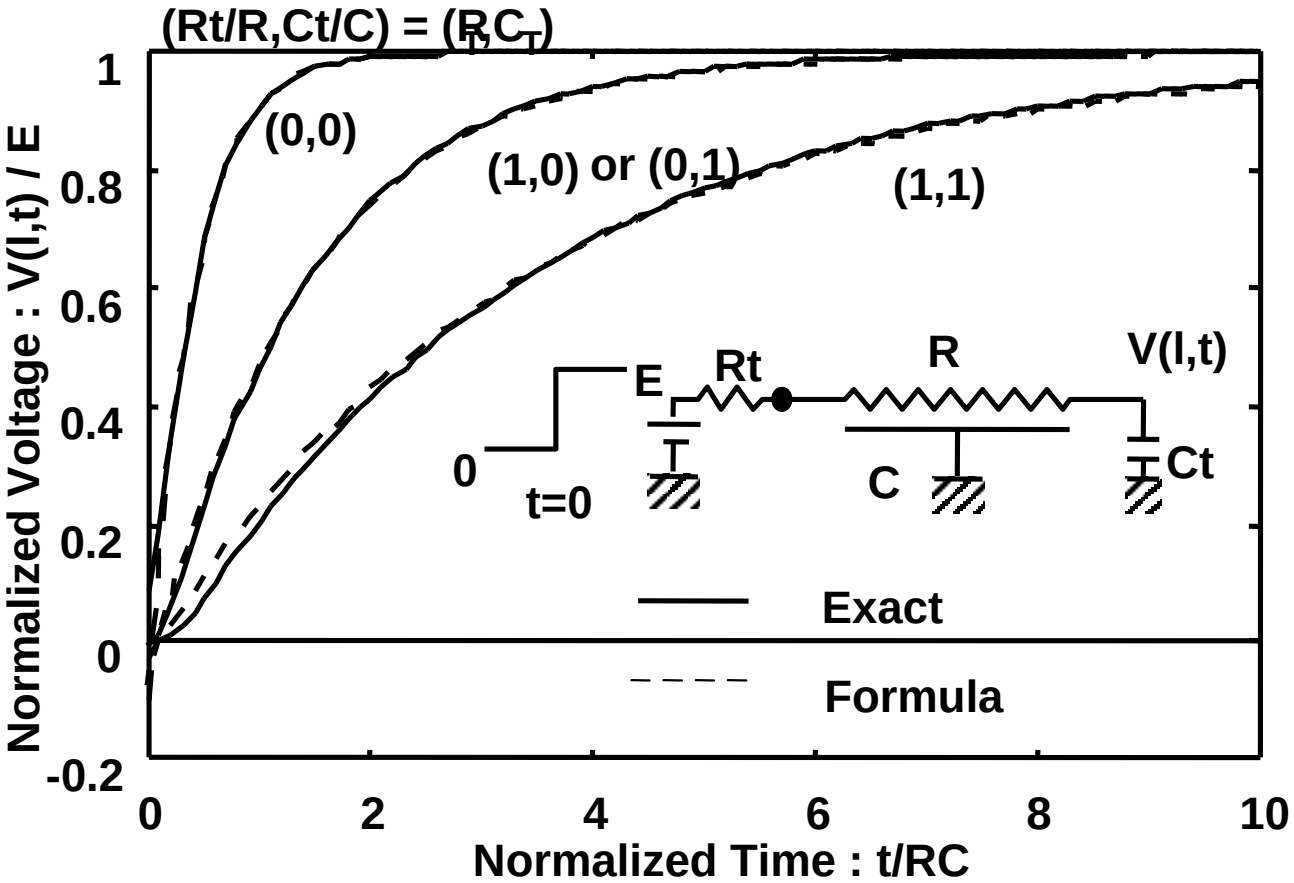
Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around



T.Sakurai

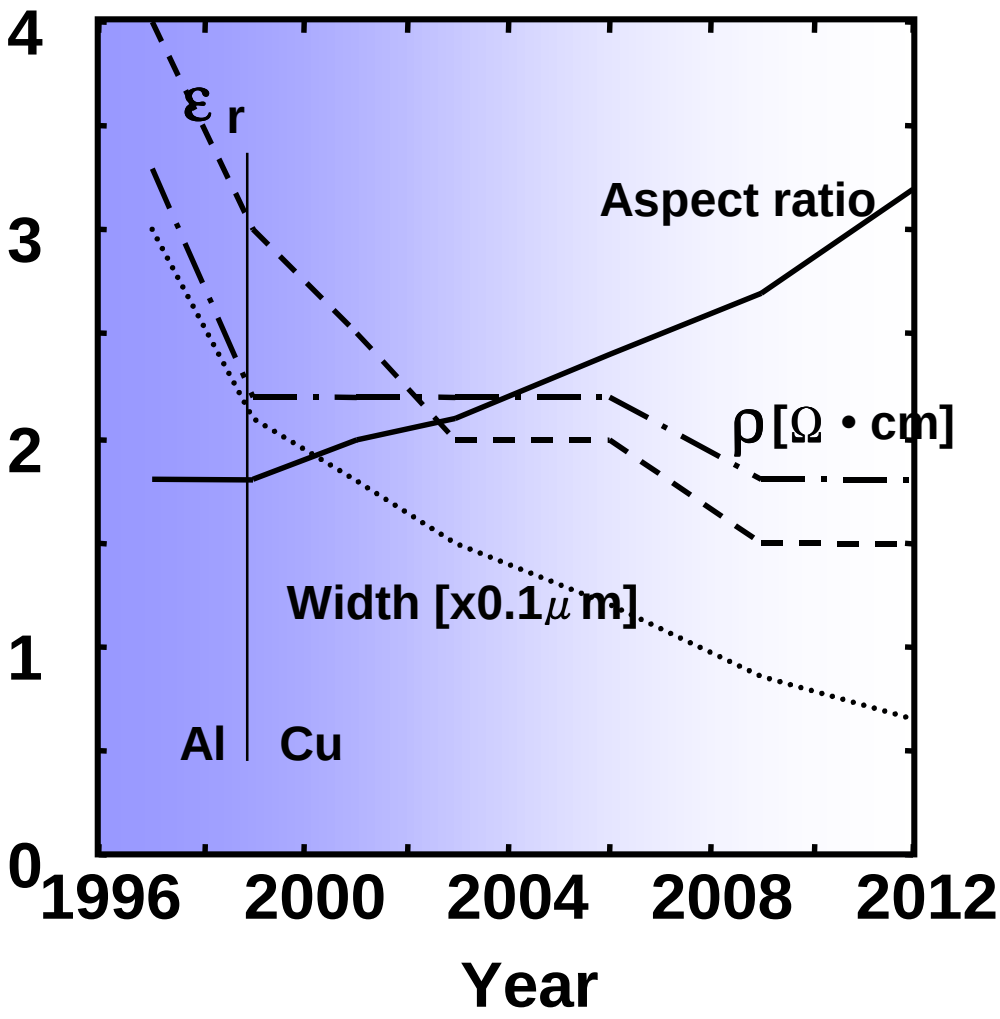
Voltage waveforms of a distributed RC line



$$\frac{V(l,t)}{E} \approx 1 - \exp\left(-\frac{t/RC - 0.1}{R_T C_T + R_T + C_T + 0.4}\right)$$

T.Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling and Crosstalk in VLSI's," IEEE Trans. on ED, Vol.40, No.1, pp.118-124, Jan.1993.

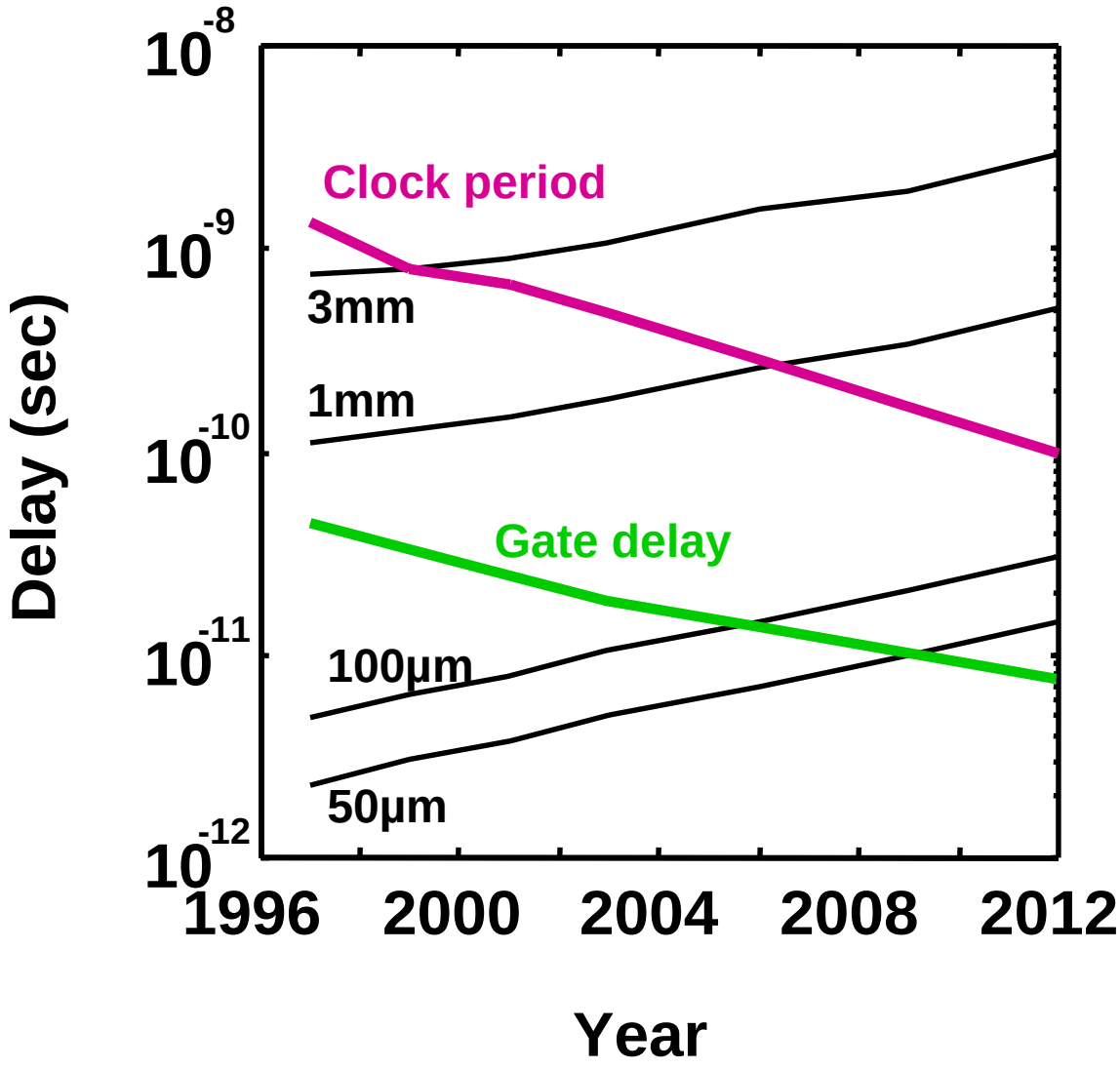
Interconnect parameters trend



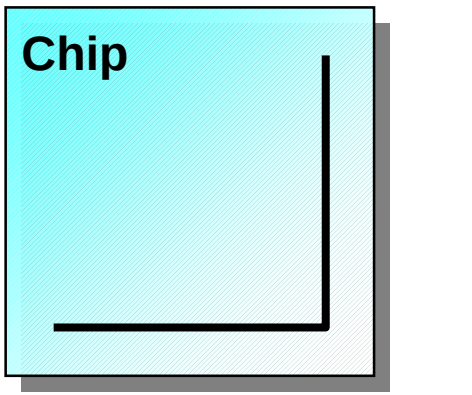
Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

T.Sakurai

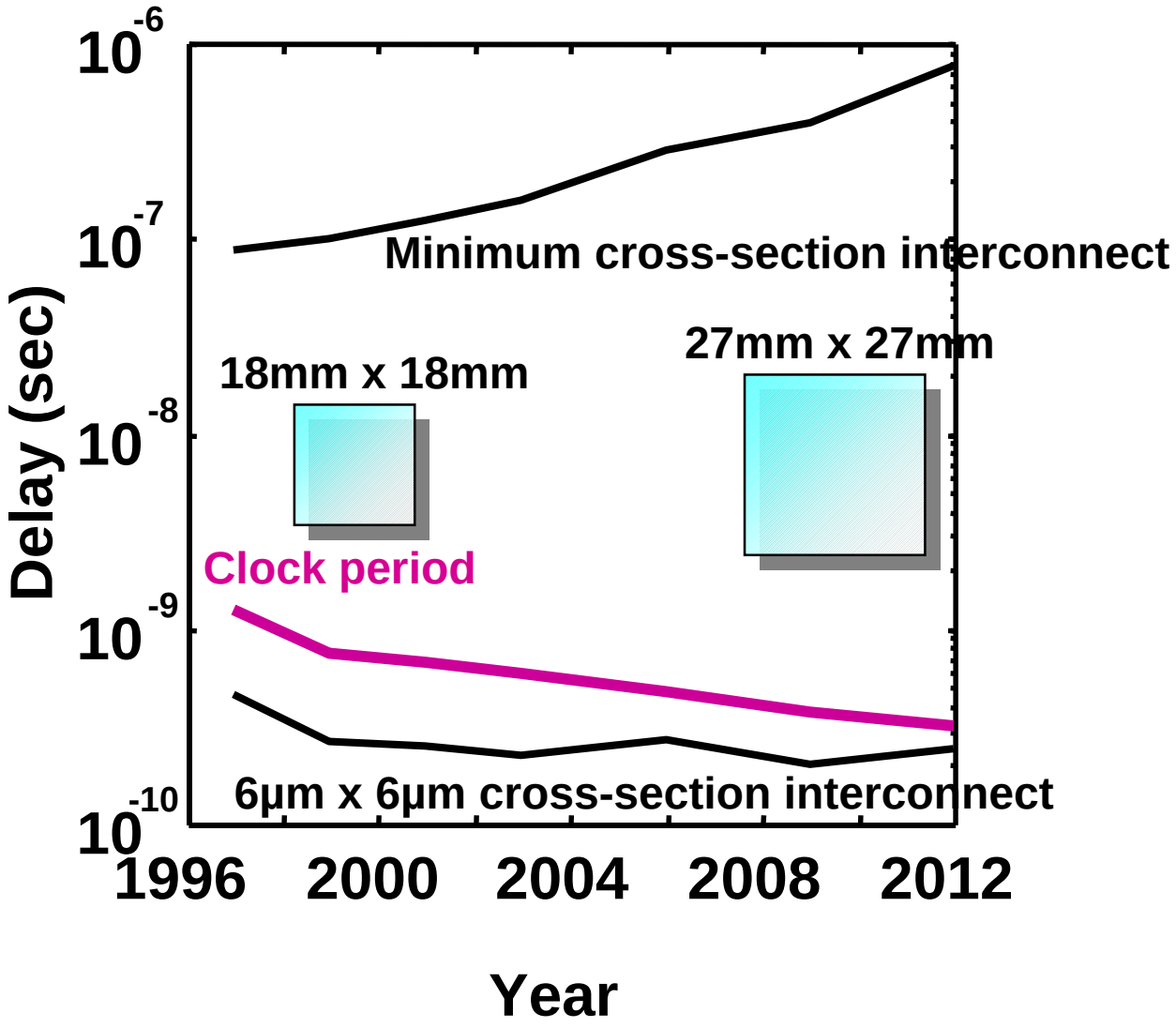
RC delay and gate delay



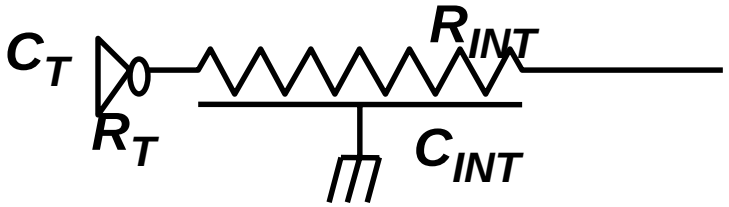
RC delay of global interconnections



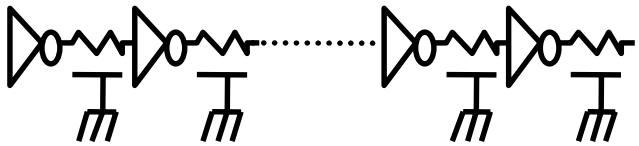
Global interconnect



Repeaters



a) Without repeaters



b) With repeaters

$$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693 (R_T C_T + R_T C_{INT} + R_{INT} C_T)$$

C_0 :Gate capacitance of minimum MOSFET

R_0 :Gate effective resistance of minimum MOSFET

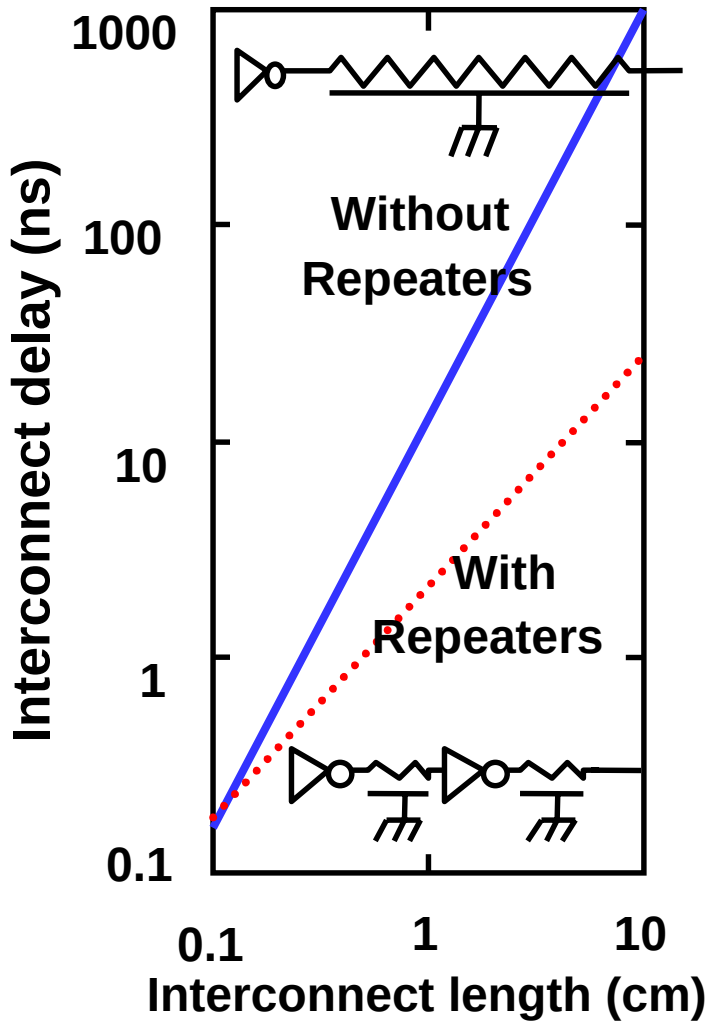
$$Delay \approx k\left[p_1 \frac{R_{INT}}{k} \frac{C_{INT}}{k} + p_2 \left(\frac{R_0}{h} h C_0 + \frac{R_0}{h} \frac{C_{INT}}{k} + \frac{R_{INT}}{k} h C_0 \right) \right] : \text{Buffered}$$

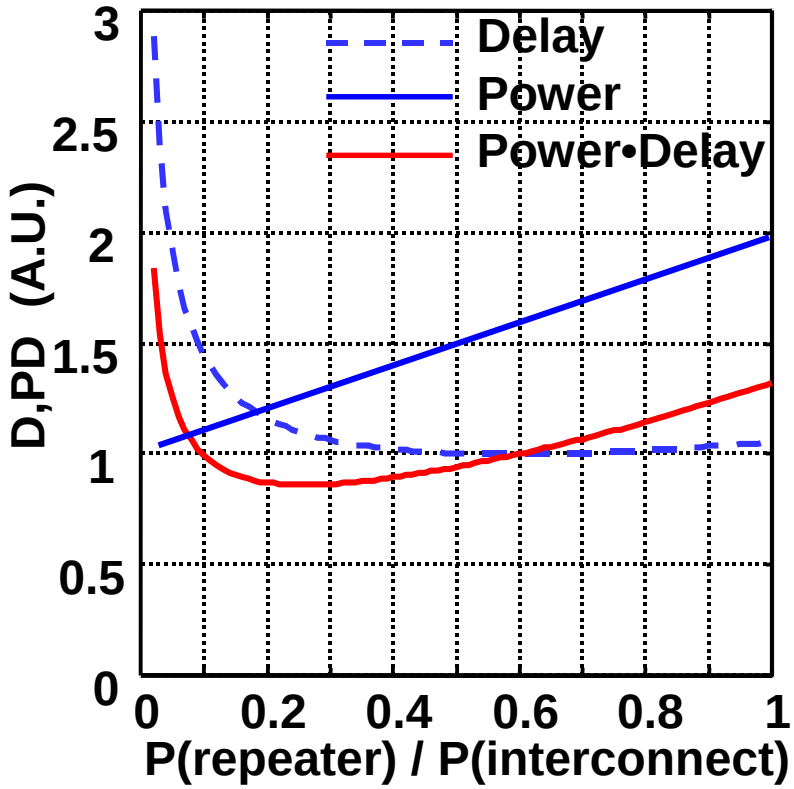
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT} R_0}{R_{INT} C_0}} : \text{Optimized size of buffer inverter}$$

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}} \sqrt{\frac{R_{INT} C_{INT}}{R_0 C_0}} : \text{Optimized number of stages}$$

$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right) \sqrt{R_{INT} C_{INT} R_0 C_0} \approx 2.4 \sqrt{\tau_{INT} \tau_{MOS}}$$

Delay and Power Optimization for Repeaters





Delay optimized

→P: P(repeater)=0.60 P(interconnect)

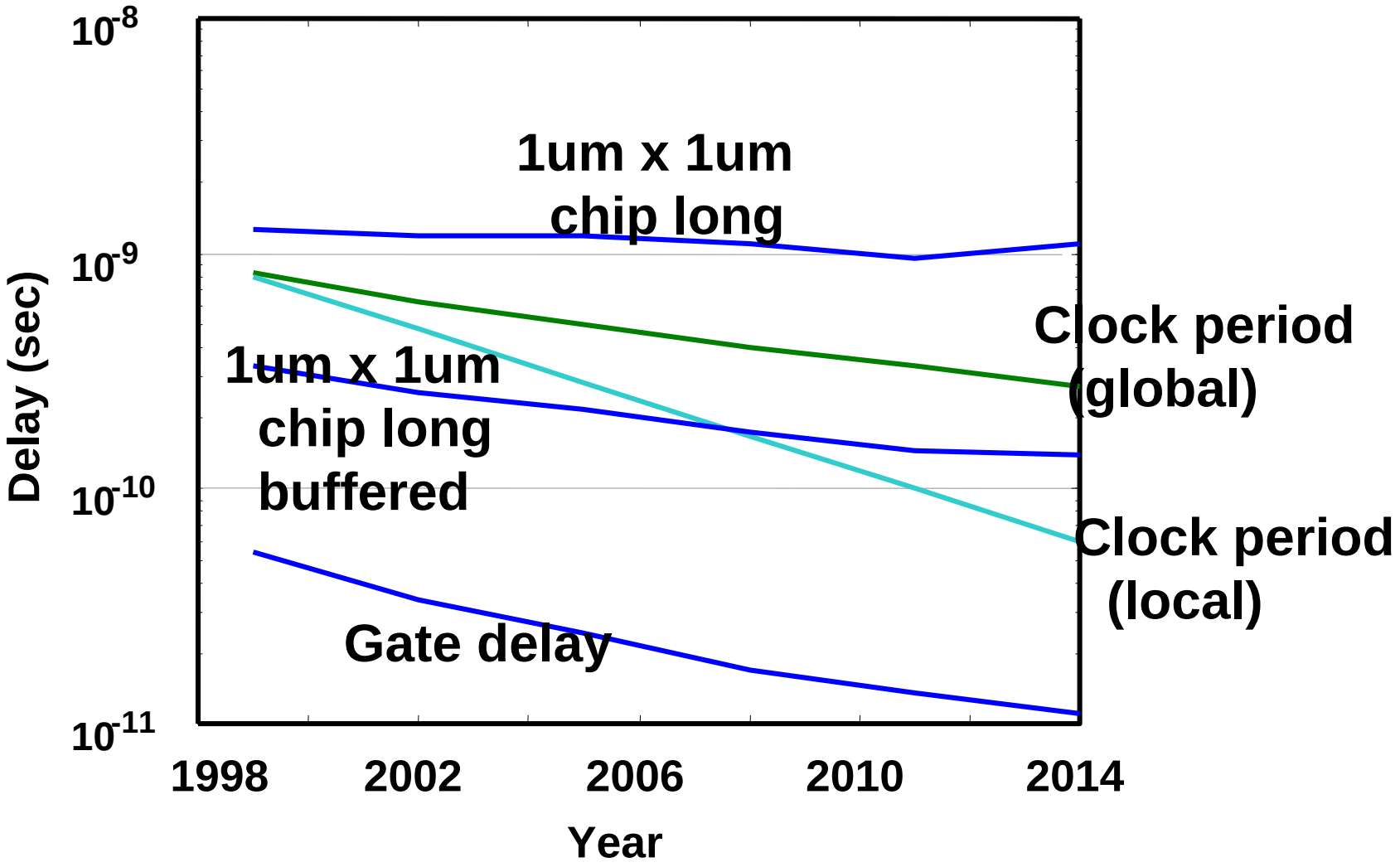
Power•Delay optimized

→D: 1.09 Dopt

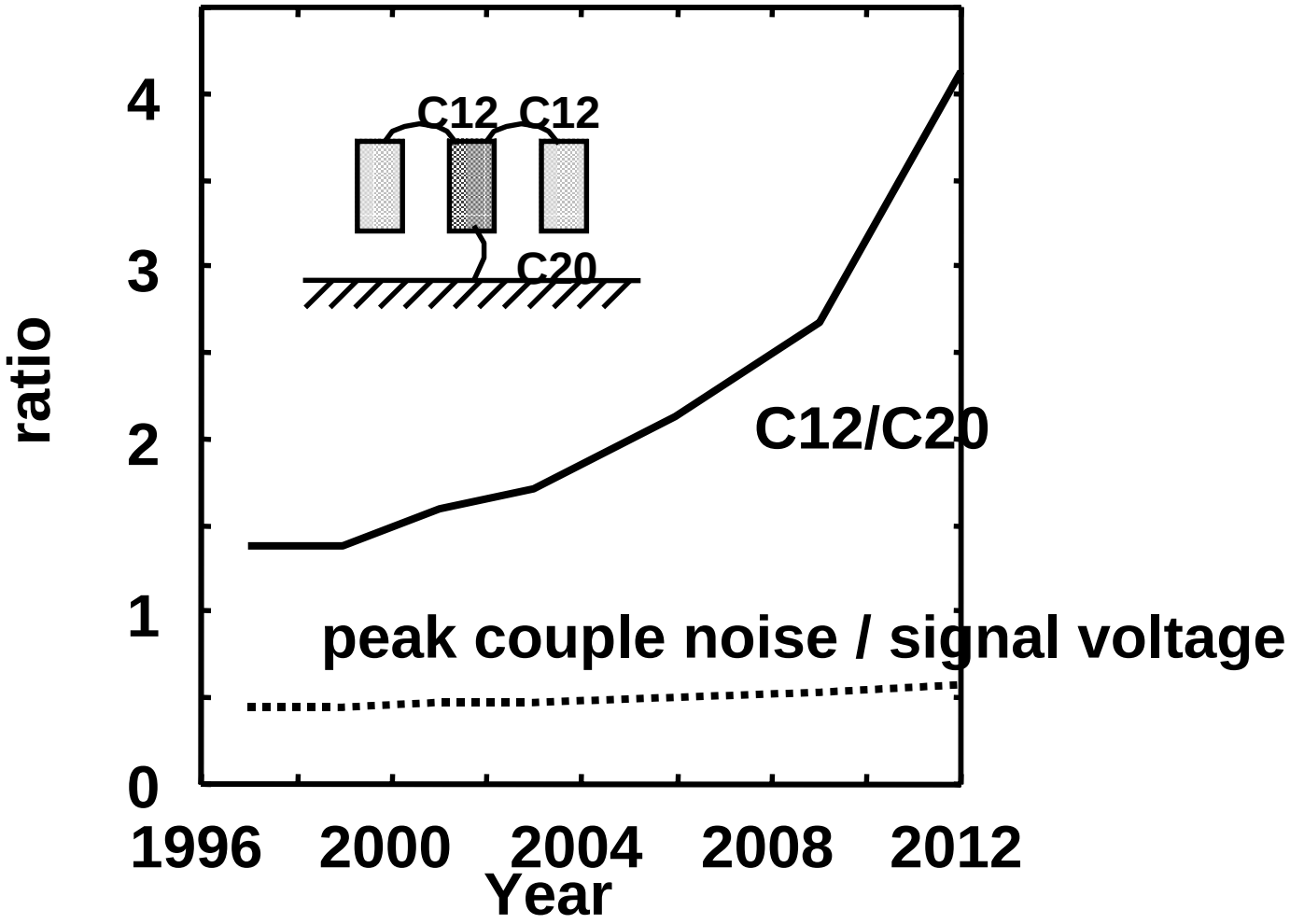
→P: P(repeater)=0.26 P(interconnect)

→PD: 0.86 of Dopt case

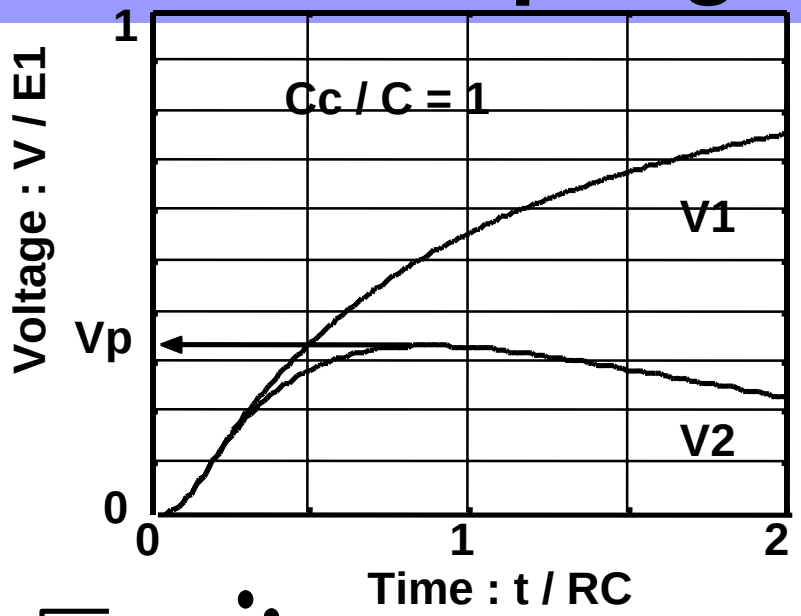
Buffered interconnect delay

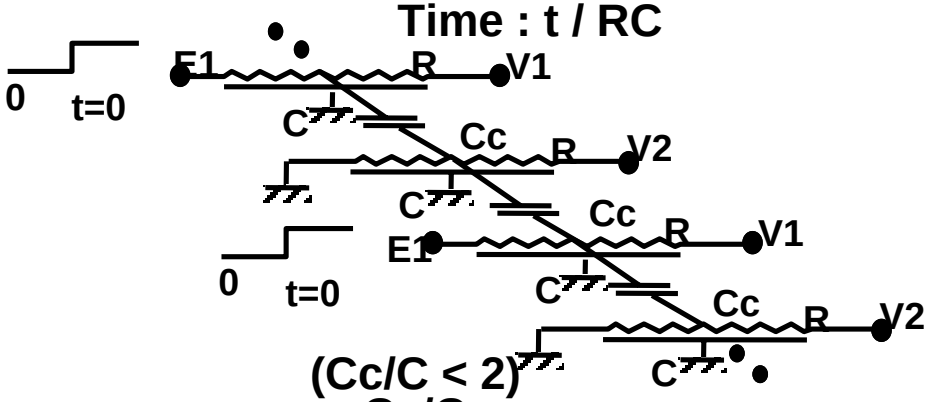


Capacitive Coupling Noise



Coupling noise in RC bus

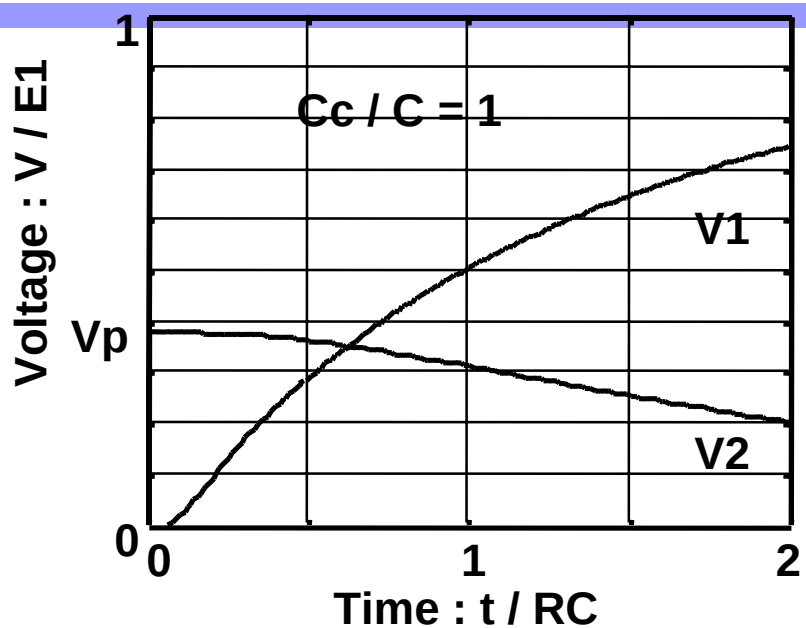


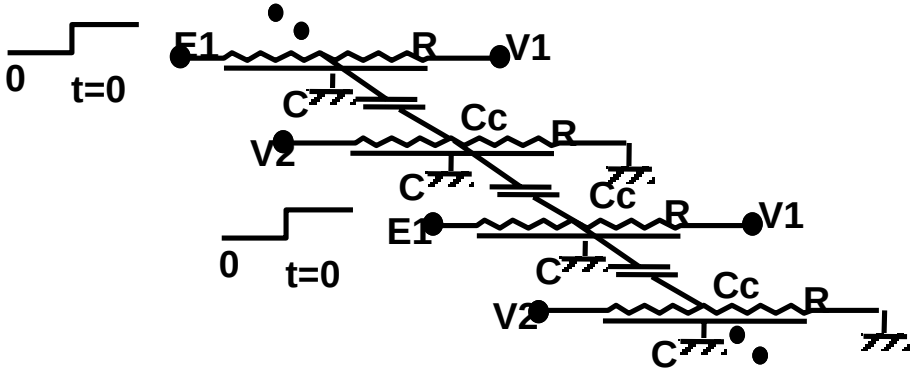


(Cc/C < 2)

$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$

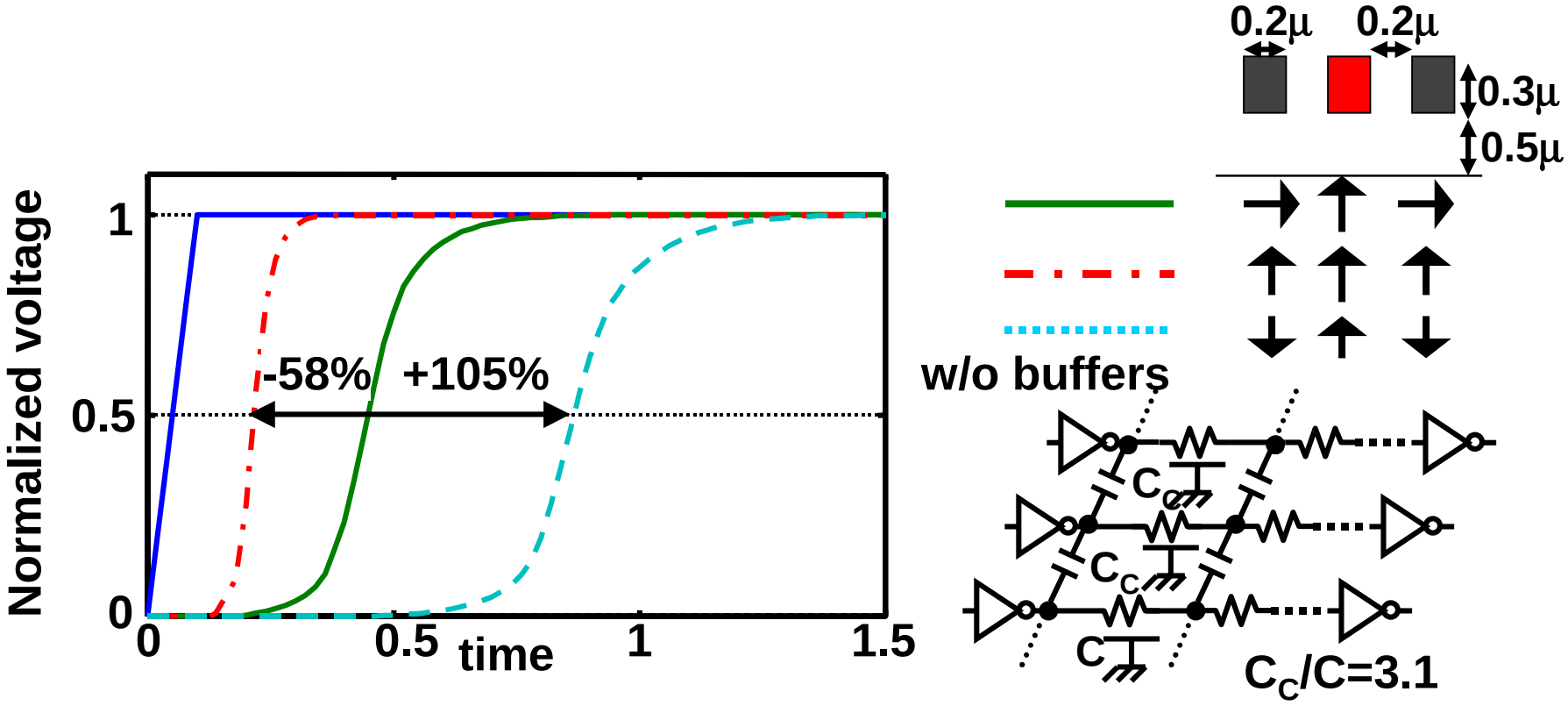




$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnections

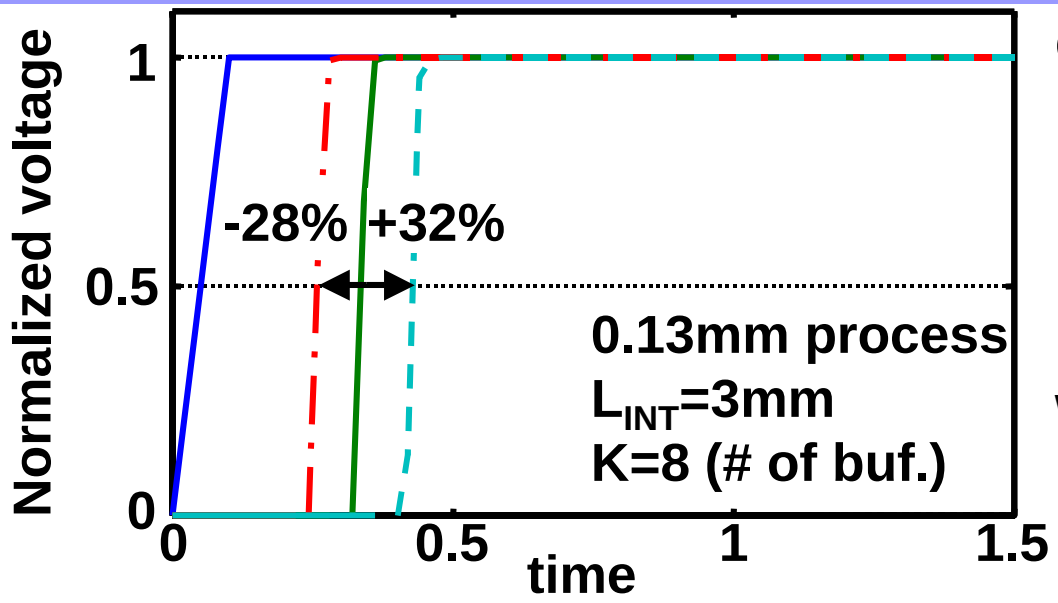


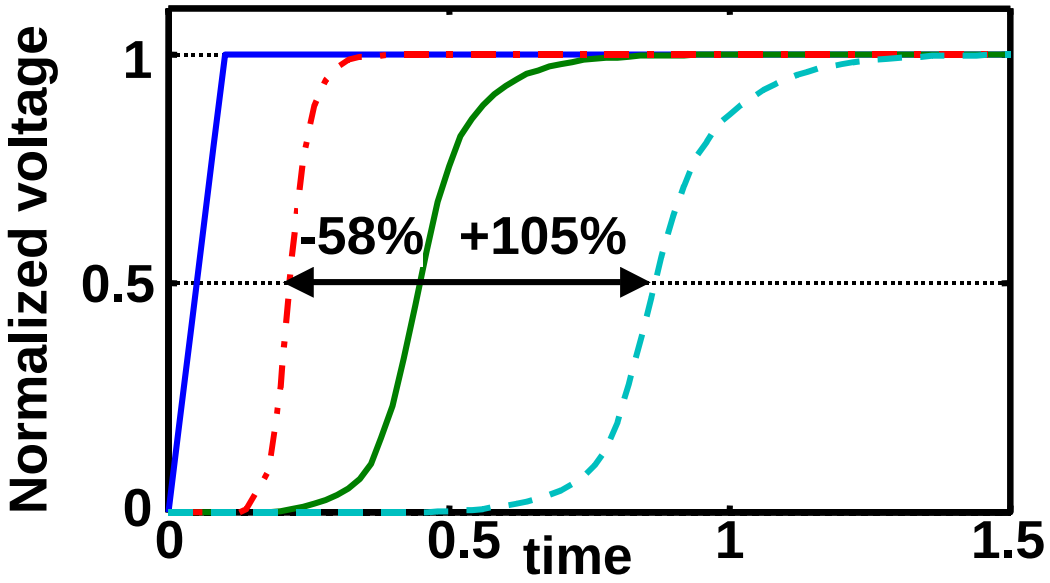
$$\frac{t_{pd}}{RC} = \frac{1}{2} + 2\eta - \frac{1}{\sqrt{6}} \log \frac{e}{2} \sqrt{1 + 8\eta + 6\eta^2}$$

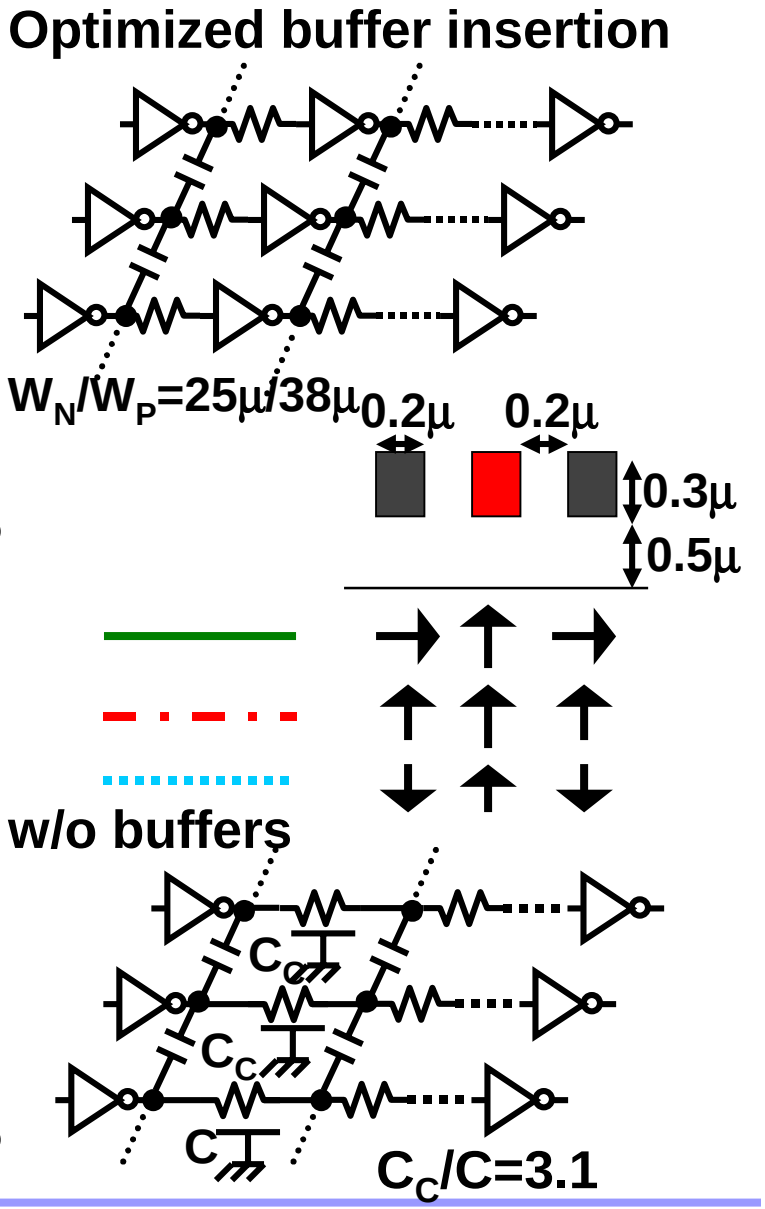
$$\approx 1.63\eta + 0.37 (\eta \le 2)\ (\eta = C_C / C)$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," 1998 ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

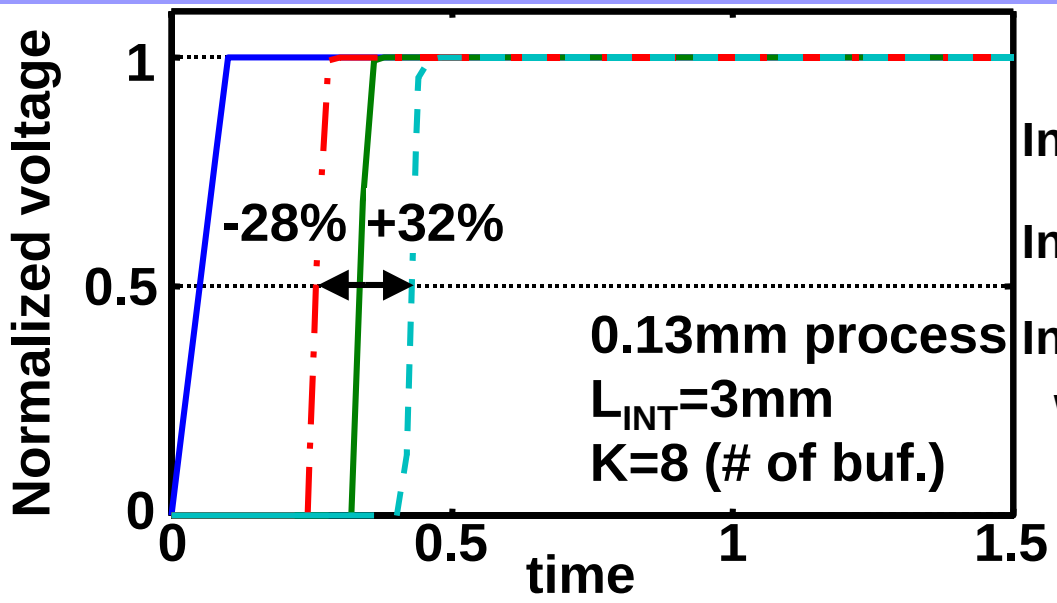
Coupling among Interconnections



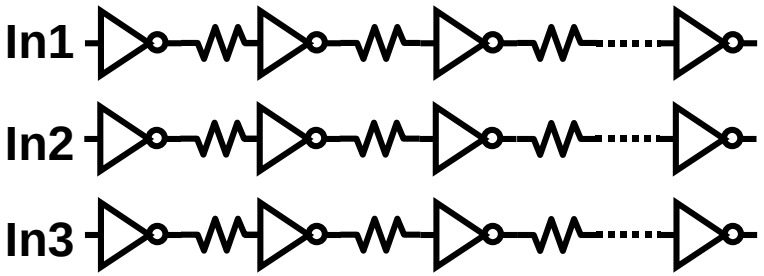




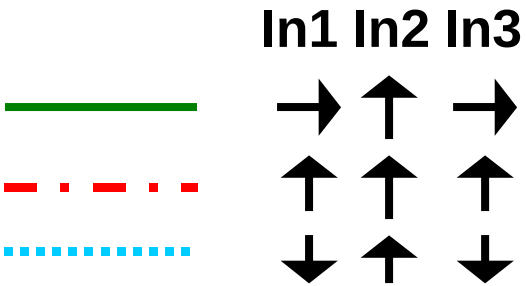
Coupling among Interconnections

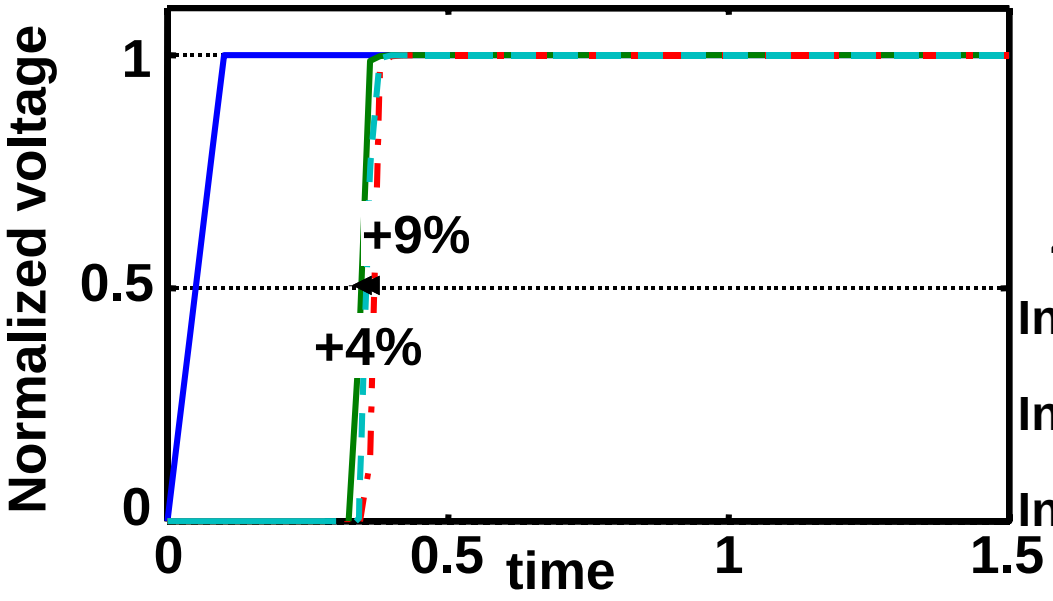


Normal buffer insertion

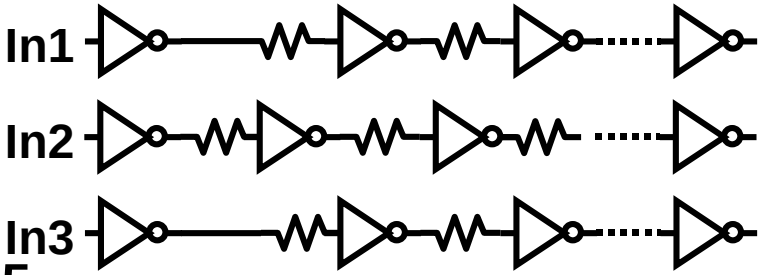


W_N/W_P=25μ/38μ

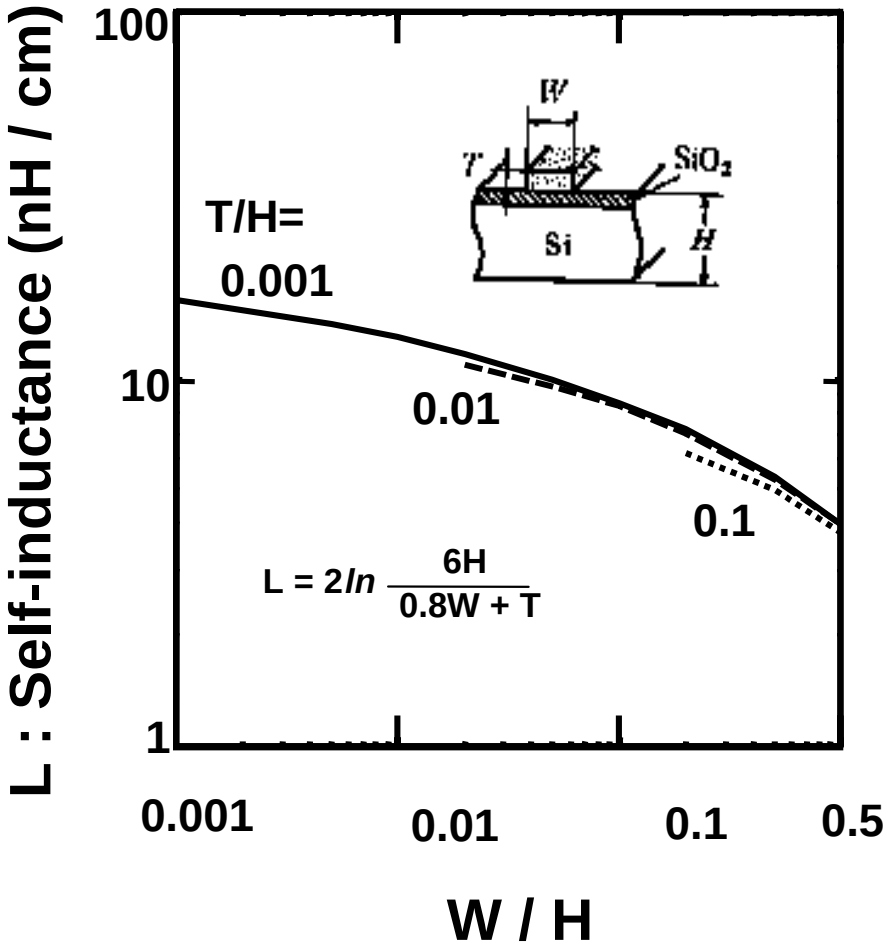




Zigzag buffer insertion



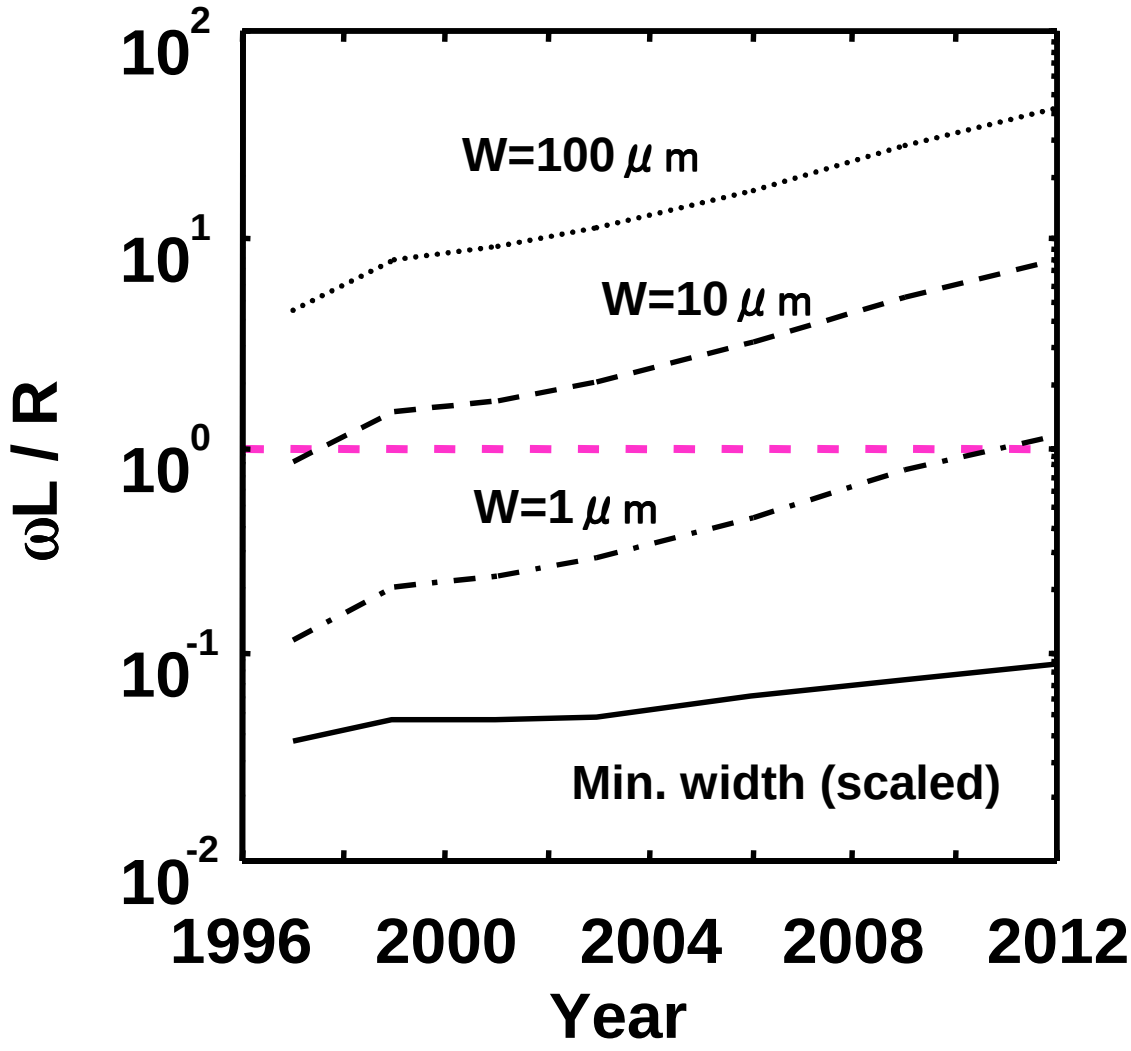
Inductance?



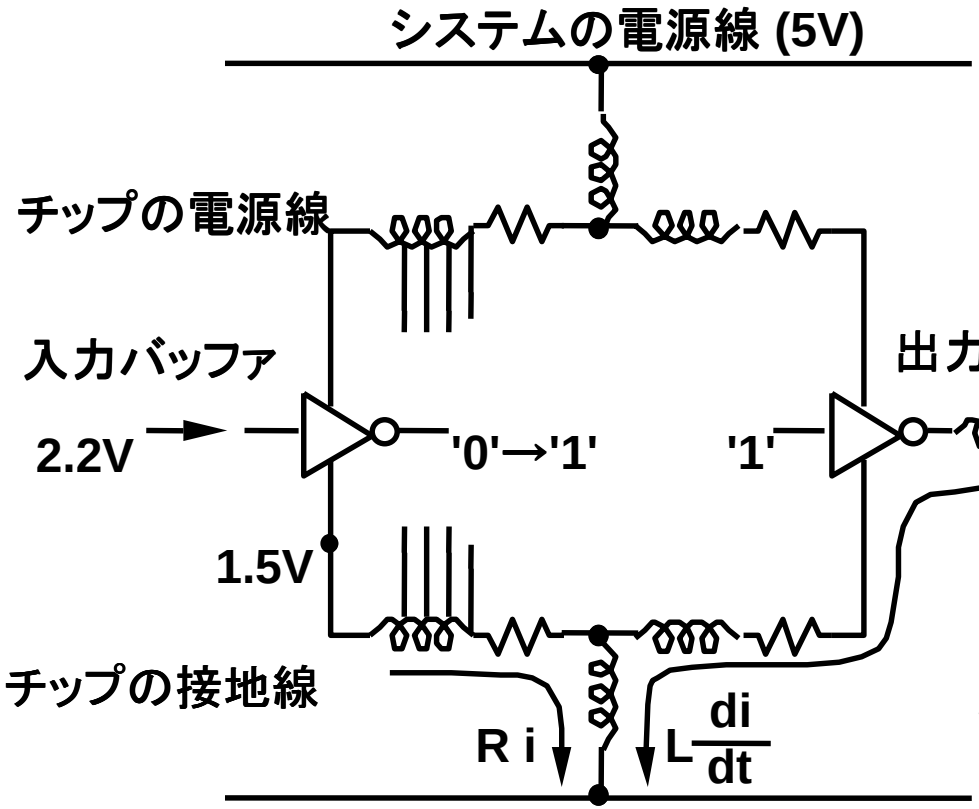
- Now RC effects surmounts LC effects because R > |jωL|.
- In the future, both of R and ωL increase (R increases more rapid?).
- Exception in low-R lines
- Inductive effects in wide clock lines in a fast processor are claimed to be observed in simulation.
- Clock lines are placed on power plane to reduce inductive effects.

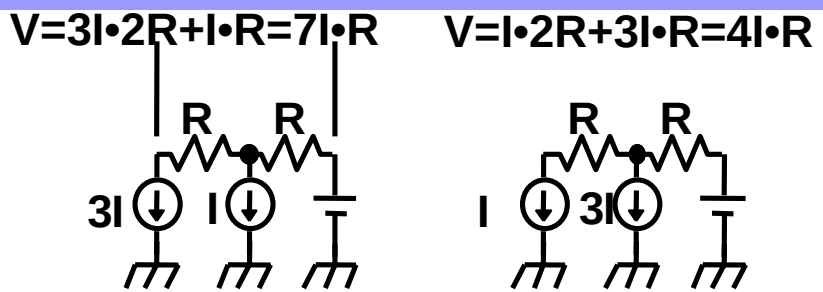
[1] D.A.Priore, "Inductance on Silicon for Sub-micron CMOS VLSI," Symp. on VLSI Circuits, 1993.

Inductive Effects

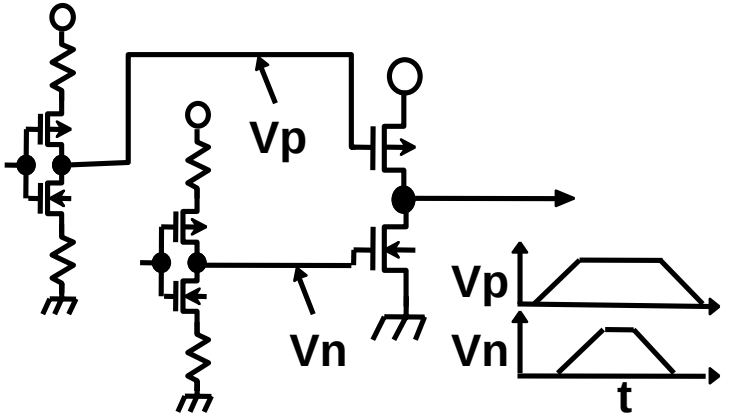


電源ノイズ

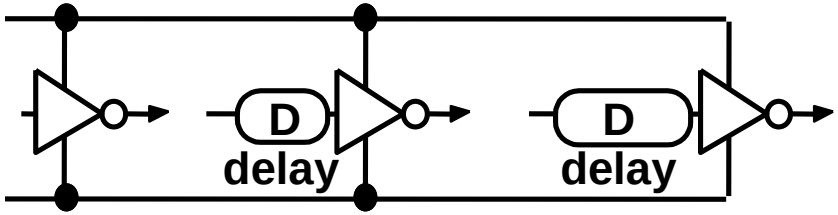




電流を多く食うブロックは電源線の根元に

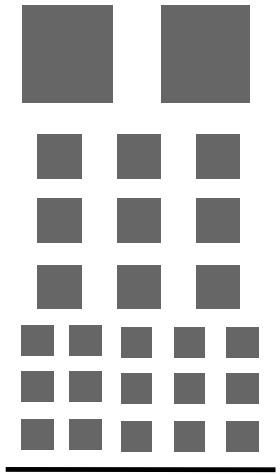


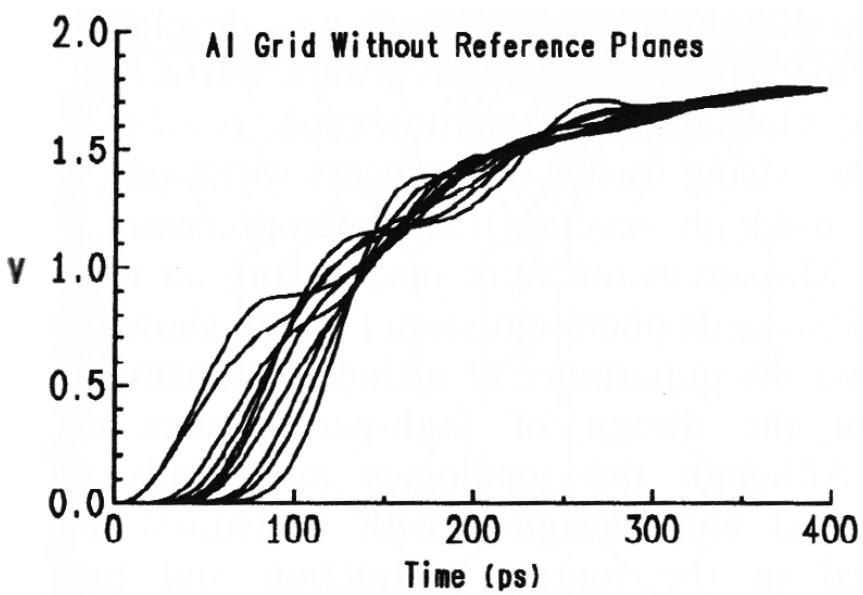
Slew-rate controlled buffer（di/dtを小さくする）

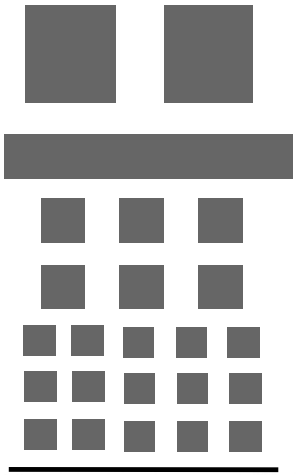


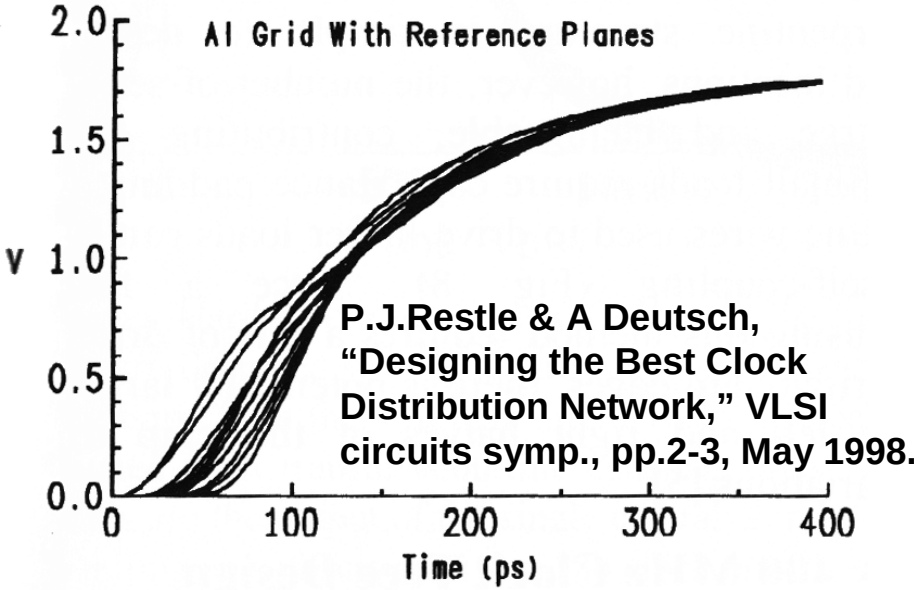
Staggered firing (電流のピーク時刻をずらす)

Inductive Effects in Clock Lines







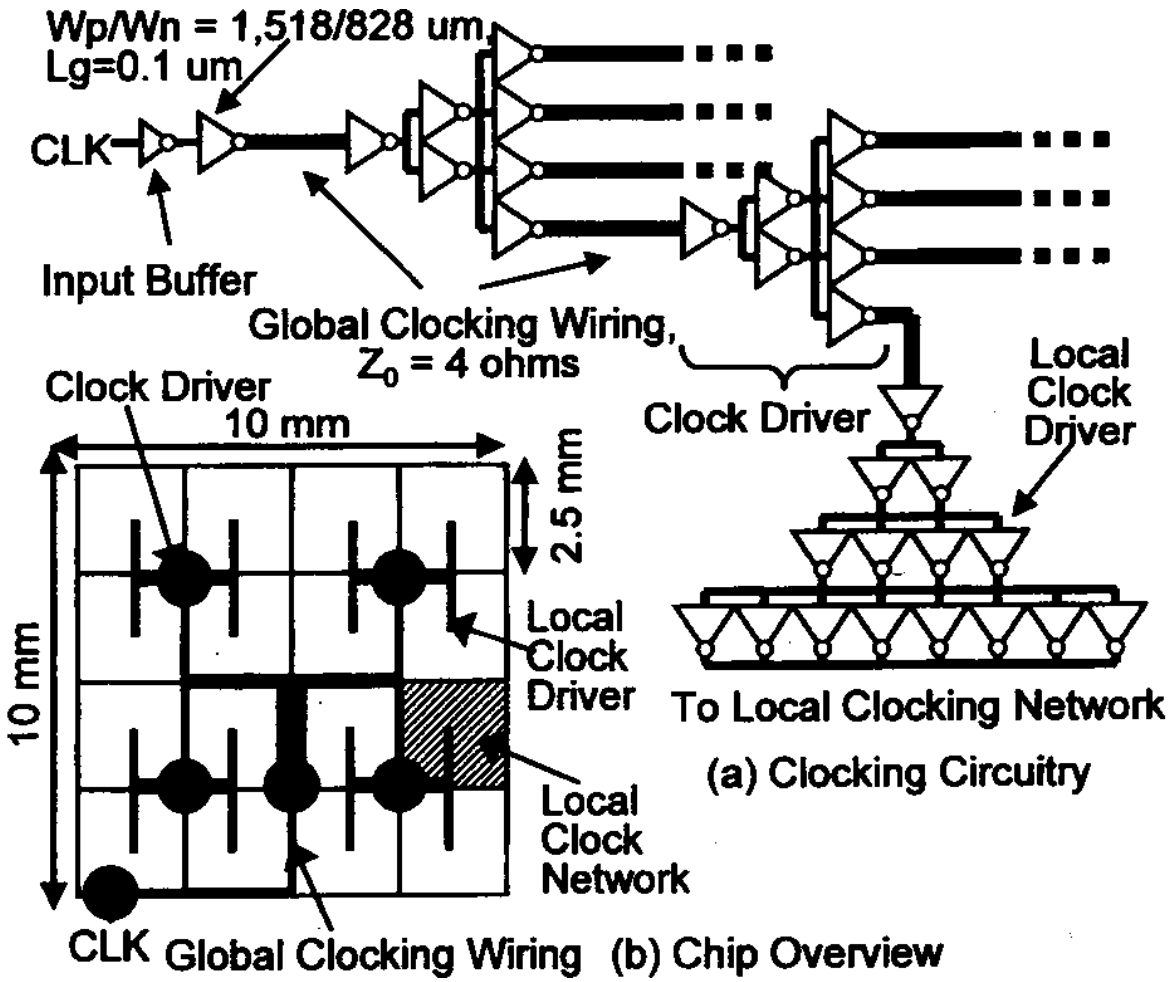


P.J.Restle & A Deutsch, "Designing the Best Clock Distribution Network," VLSI circuits symp., pp.2-3, May 1998.

Board design practice is imported in LSI.

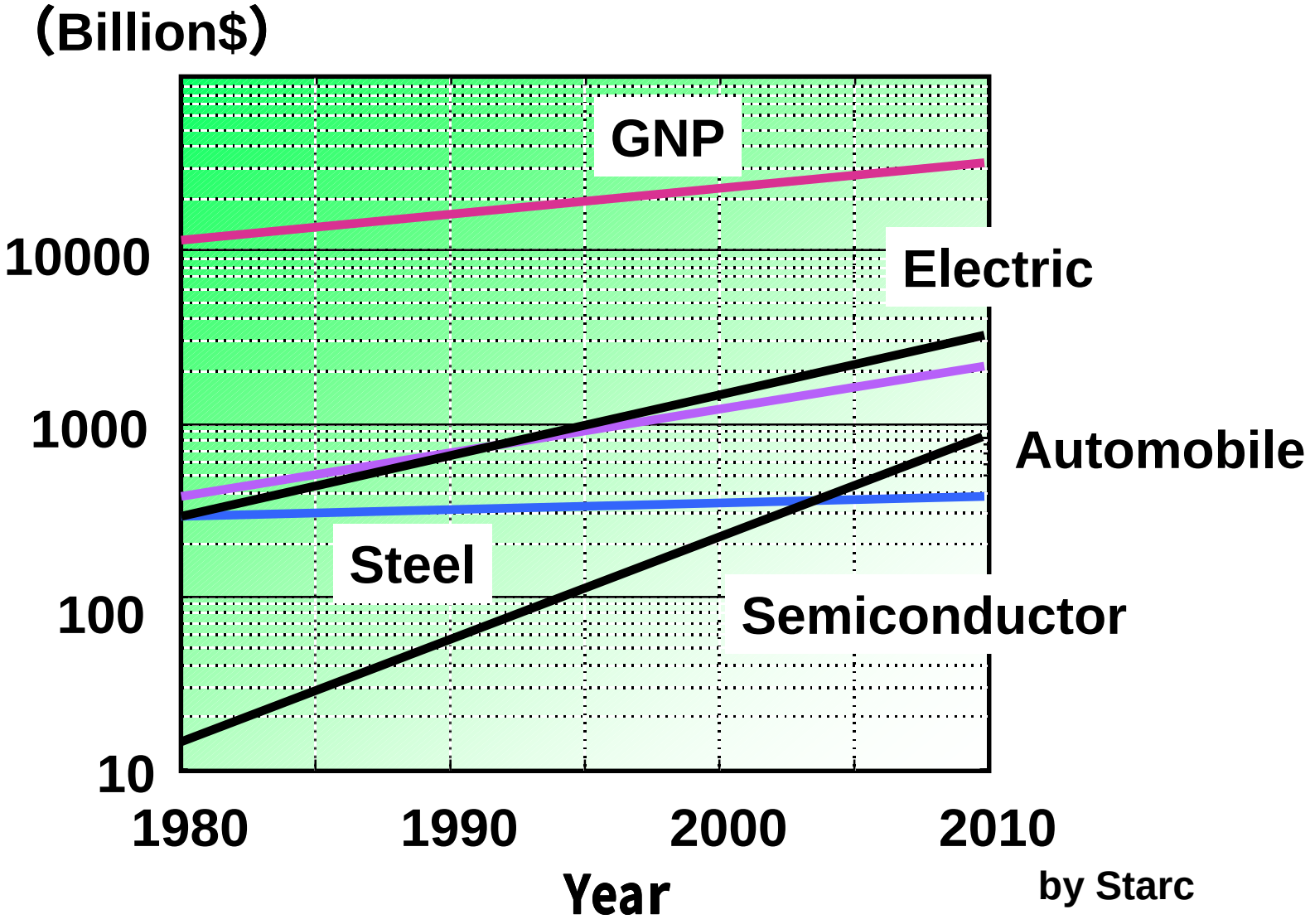
T.Sakurai

H-tree clock distribution

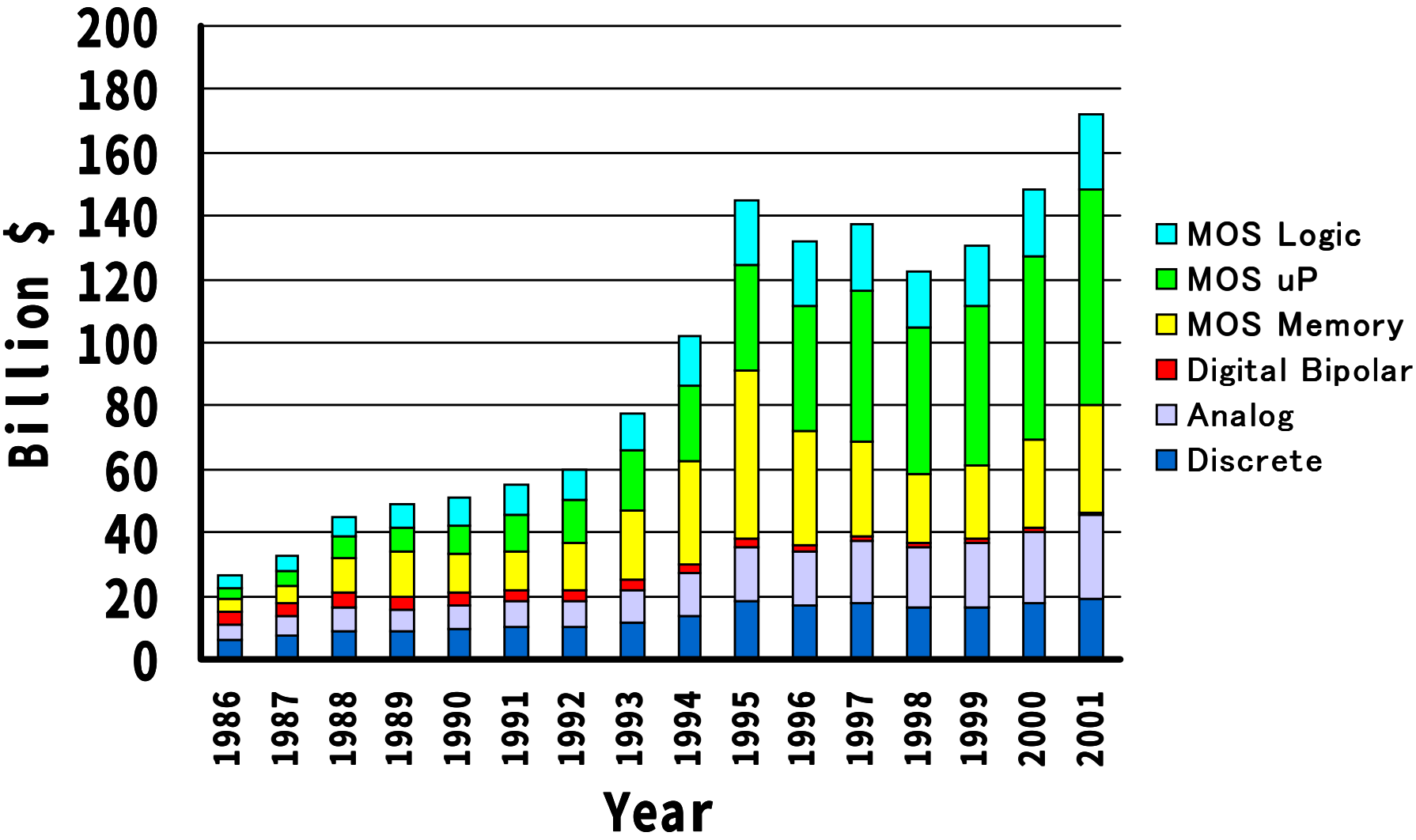


M.Mizuno, K.Anjo, Y.Sumi, H.Wakabayashi, T.Mogami, T.Horiuchi, M.Yamashina, "On-Chip Multi-GHz Clocking with Transmission Lines," ISSCC, pp.366-367, Feb. 2000

World-Wide Semiconductor Market



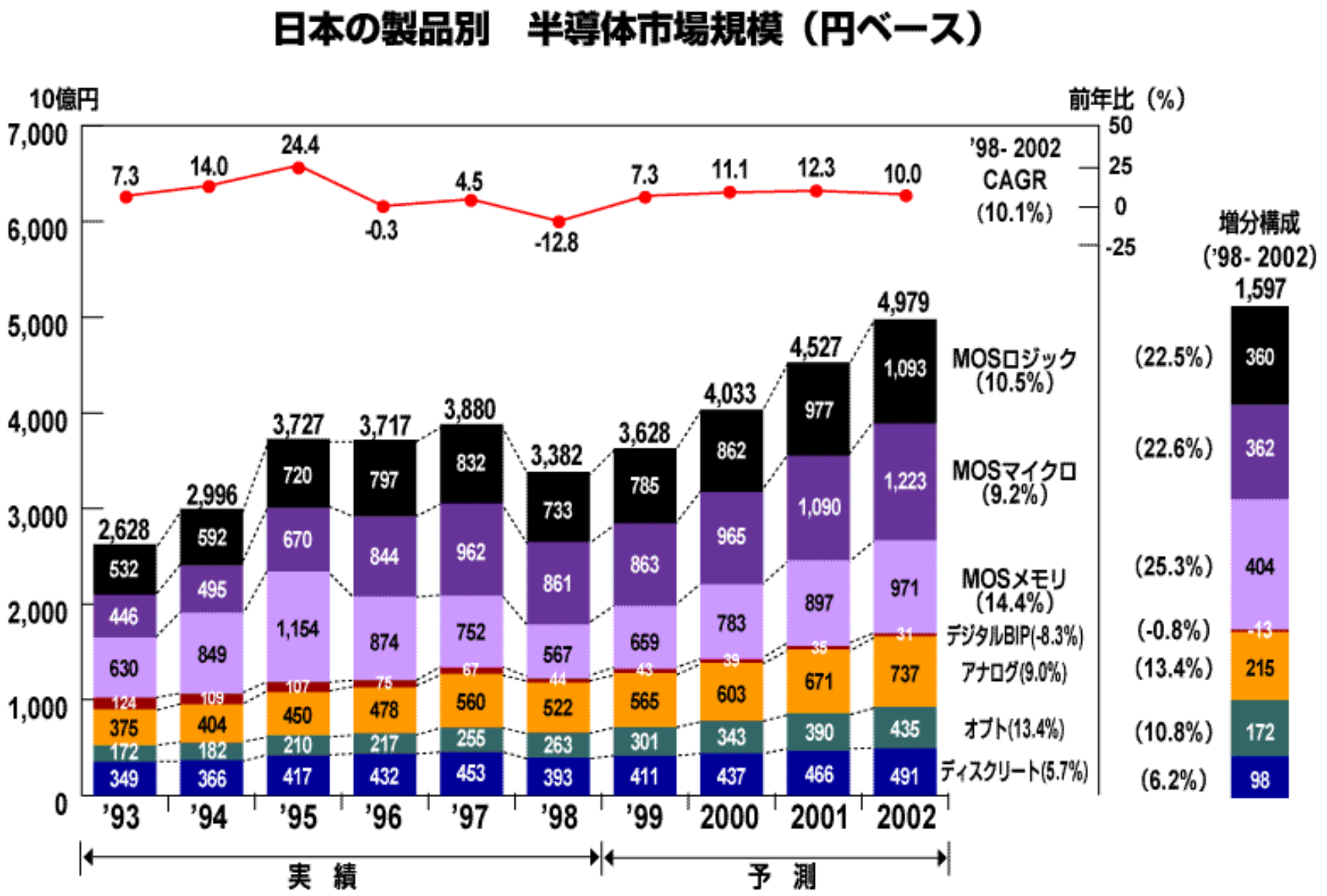
World semiconductor market



Data : World semicon market statistics

T.Sakurai

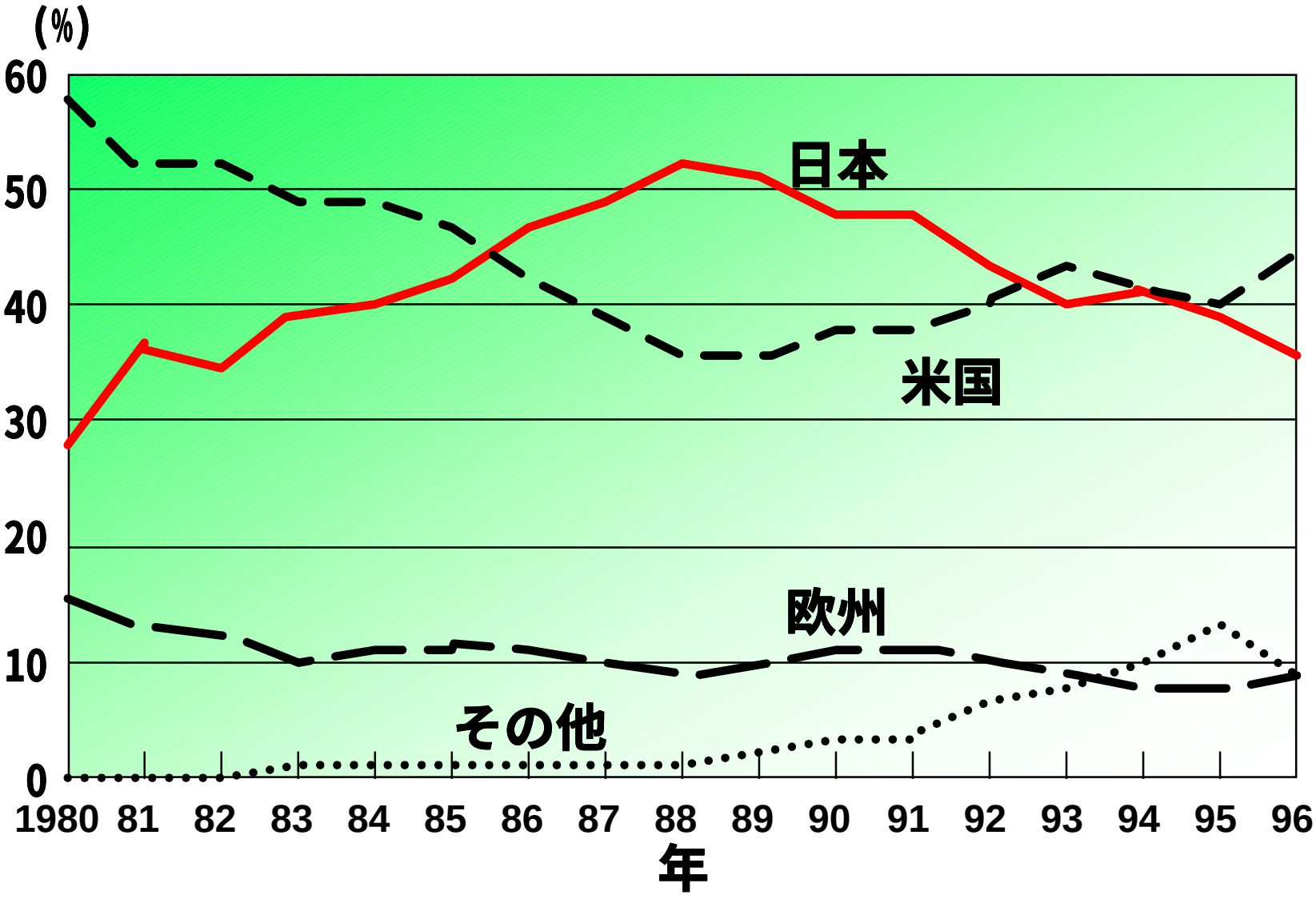
日本の半導体市場



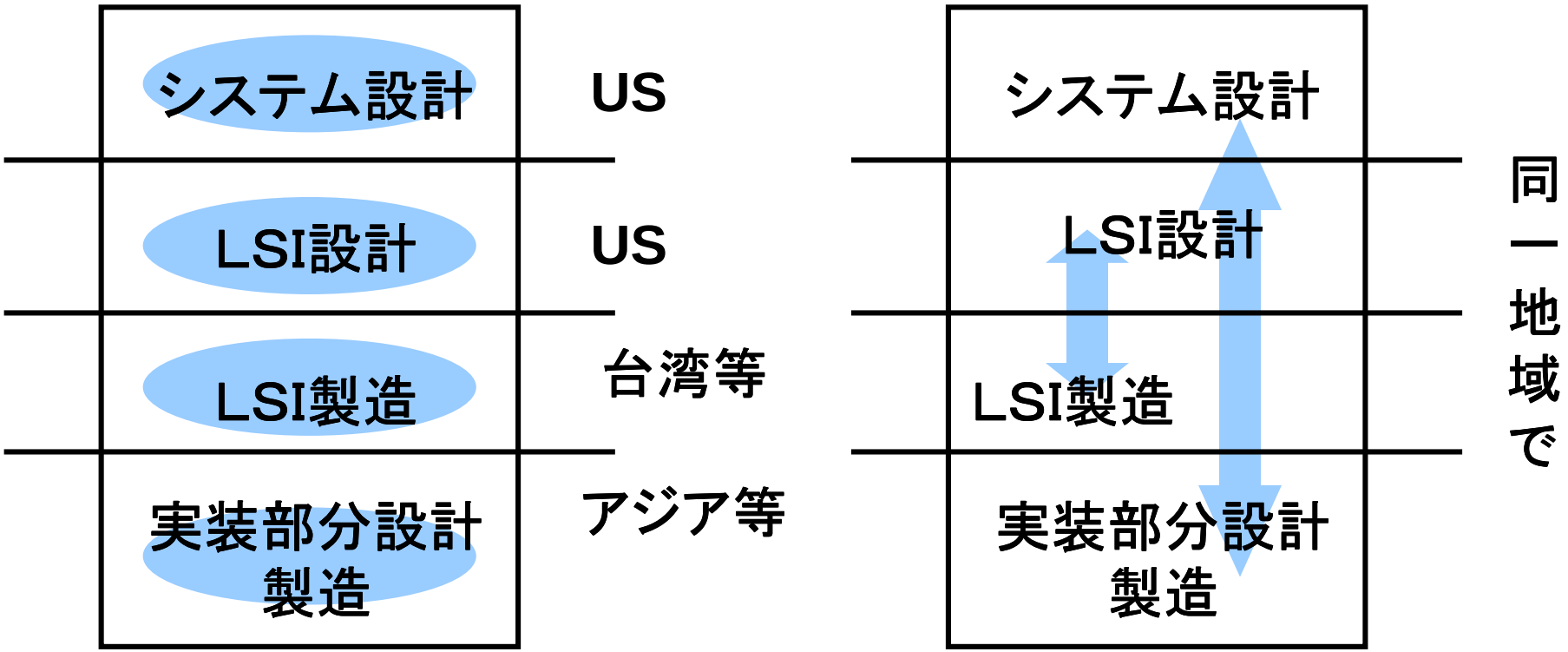
http://www.eiaj.or.jp/japanese/press/pre64/index_2.htm

T.Sakurai

地域別半導体メーカシェア



水平分業と垂直統合


システム設計
LSI設計
LSI製造
実装部分設計
製造
US
US
台湾等
アジア等
ASIC、デジタル、SoC
システム設計
LSI設計
LSI製造
実装部分設計
製造
同一地域で
メモリ
アナログ
CPU
SoC
SiP

Assembly & Packaging

“There is an increased awareness in the industry that assembly and packaging is becoming a differentiator in product development.”

International Technology Roadmap for Semiconductors, ITRS’99 p.213

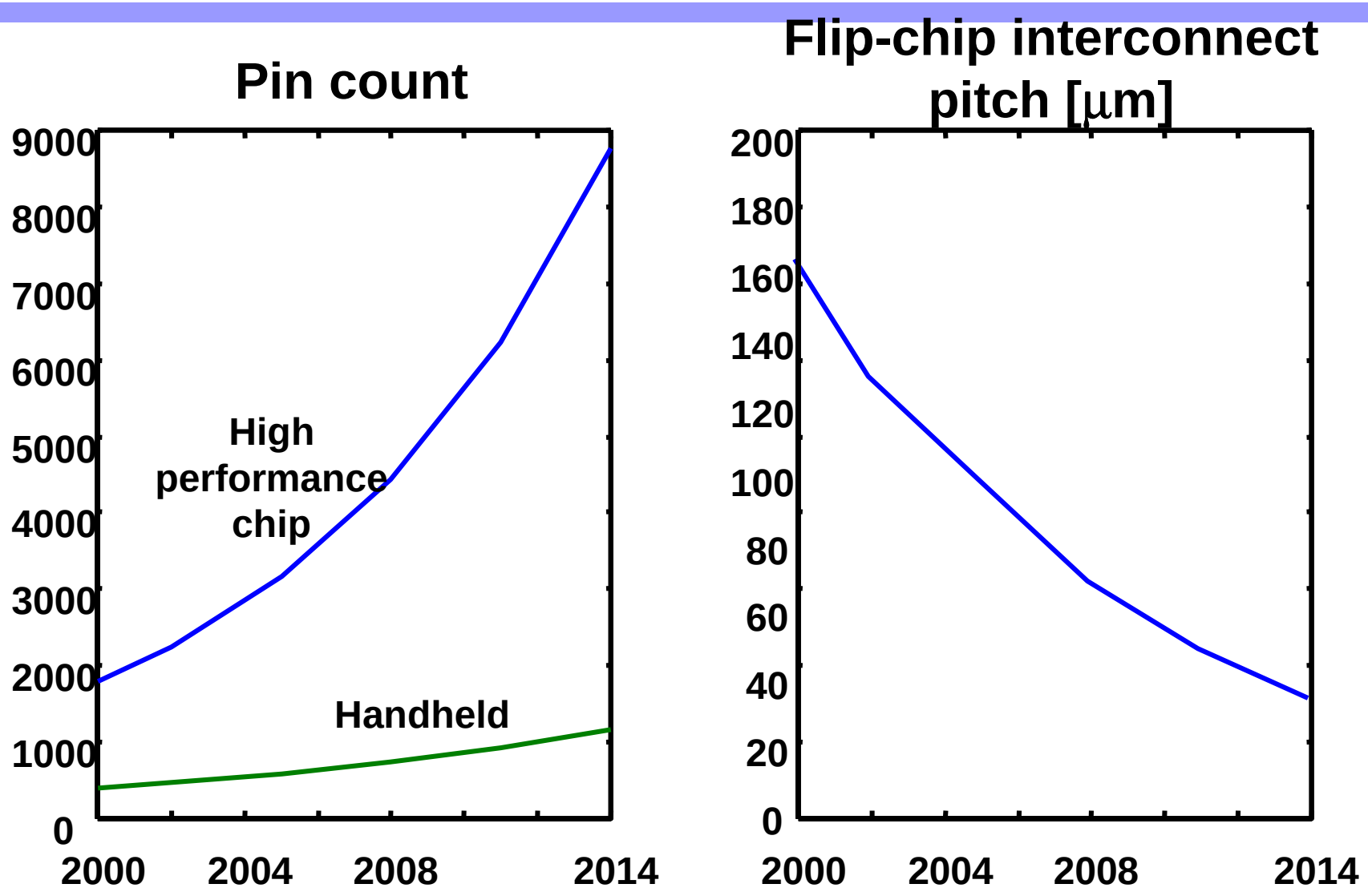
LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	μm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (μP)		21M	3.6G	170
DRAM capacity		1G	1T	256
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	μcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA) , International Technology Roadmap for Semiconductors: 1999 edition. Austin, TX:International SEMATECH, 1999.

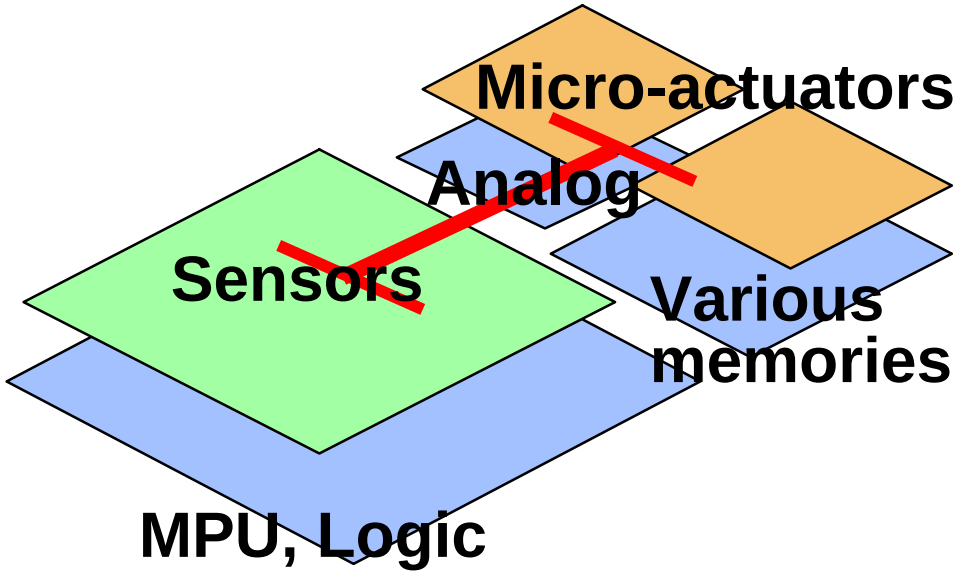
T.Sakurai

Trend in packages



ITRS'99

Possible electronic system in 2014

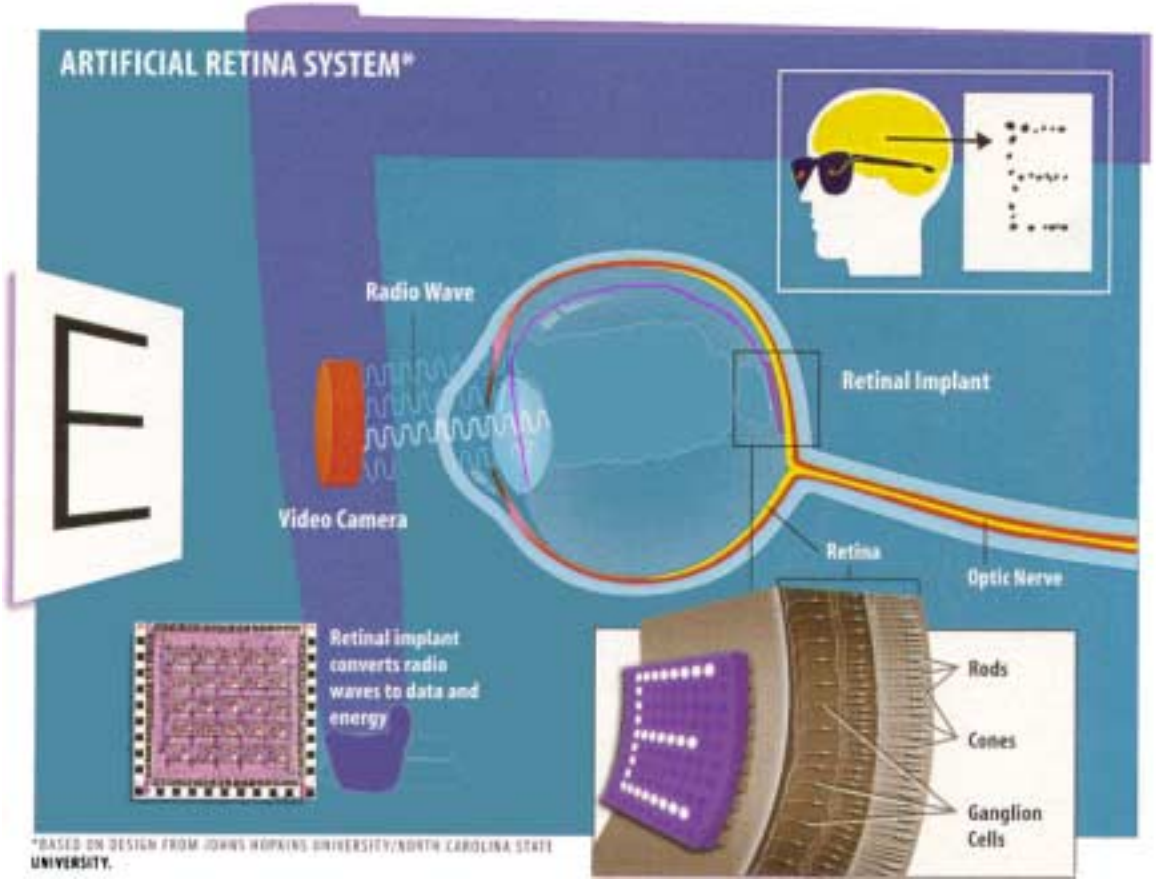


- Sensors/actutors
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)

Prosthesis - Dual Intraocular Units

NC STATE UNIVERSITY

Retinal Prosthesis

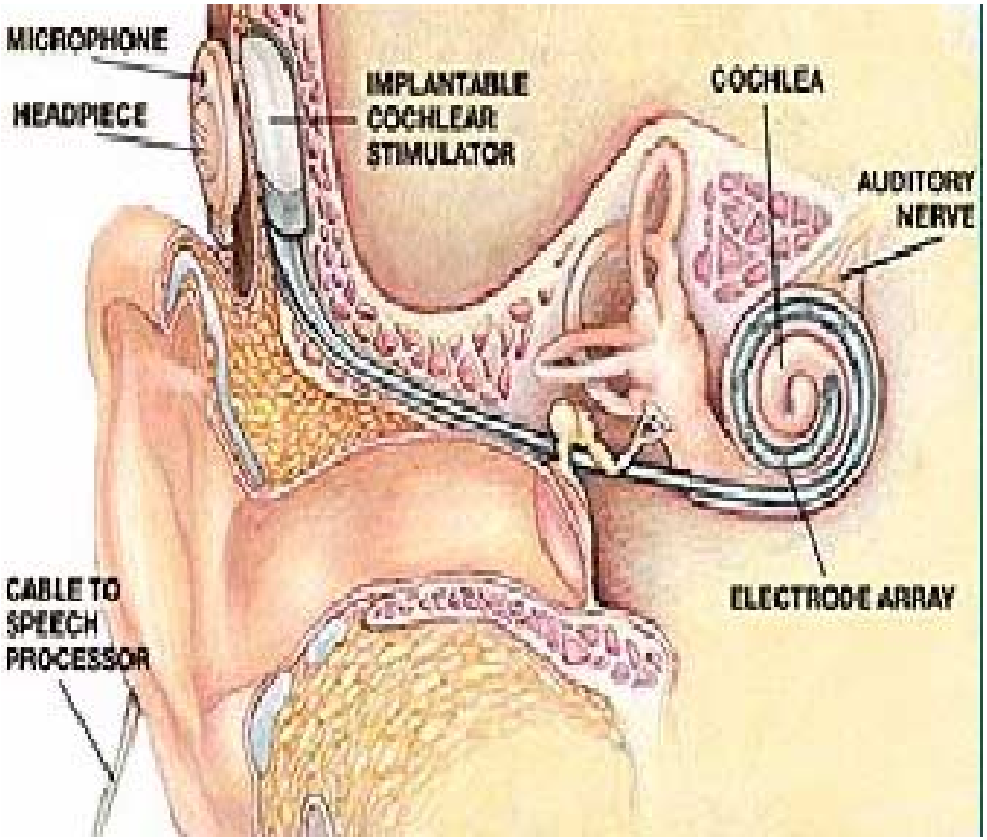


Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Cochlear Implants

NC STATE UNIVERSITY

- 22 Electrodes
- Spatially Attached at Cochlear (low pitch sound at the apex)
- Power and Signals by Carrier Radio Frequency



Retinal Prosthesis

将来の実装が開く世界

さて、将来、LSIの超低電力化が実現され、より安価な無線機能が実現できれば、全く新しいアプリケーションへの道が開けることも考えられる。例えば、メモリや簡単なプロセッサを内蔵し、電源は無線でもらう1ミリ角で0.1ミリ以下の薄さのチップができたとする。これを現在のバーコードの代わりに全商品に付加すれば、インテリジェント・バーコードといった応用が可能になる。スーパーマーケットなどでは、全く人手に頼らず、リアルタイムで在庫管理ができる。どの商品がまだ商品棚にあるかなどを無線でチェックできるからだ。冷蔵庫の中にあるものの賞味期限管理を自動で行うといった応用にも効力を発揮する。衣服に取り付けて、そろそろ洗濯どきだといった警鐘を鳴らすことも可能だ。このようなチップをすべてのお金に埋め込めば、リアルタイムでキャッシュレジスタの中にあるお金の金額がわかるので、金銭授受でのミスや勘定ミスなどもなくなるだろう。書類に埋め込めば、この書類はどこの机を通過してきたかを記憶でき、履歴を読むこともできる。

新しいLSIのアプリケーションとして人体へ埋め込むチップや、医療に使われるチップにも低電力化と無線技術が必須である。無線を使った人工網膜チップを眼に埋め込むことによって、眼の不自由な人がアルファベットを認識したという報告がなされている。また、血管の中にチップを入れて、各種の検査や治療を行うことも考えられている。

日経産業新聞（桜井貴康）