

未来開拓プロジェクトの概要と 回路・ソフトウェアの協調による低消費電力化

「極低消費電力・新システムLSI技術の開拓」

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期待される成果、独自性

- 0.5V以下で高速動作するLSIを実現する
新システム、回路、デバイス技術
(0.5V、GHzレベルクロック動作)
- 学術的に未着手の低電力LSI新分野の体系化



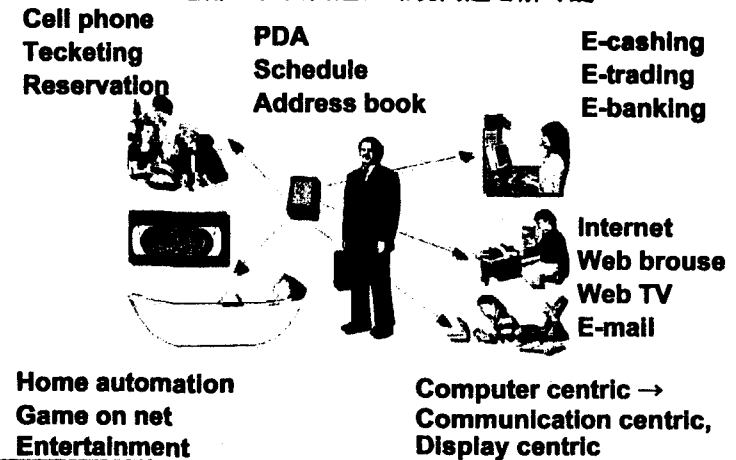
- 独自性
ソフトウェア、システム、
回路、デバイス、CADなど
分野間の連携によるソリューションの提案

日本の産業競争力の増大

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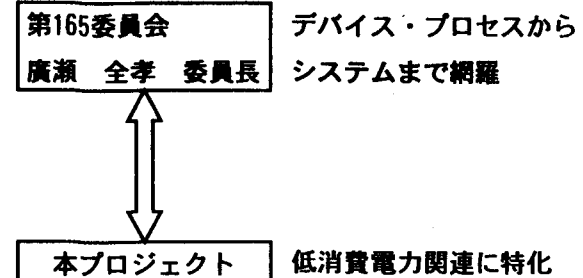
低電力LSI：モバイルIT社会のインフラ

高齢化社会問題、環境問題を解く鍵



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本プロジェクトの位置付け



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研究組織・研究分担

プロジェクトリーダー

桜井貴康 東京大学国際・産学共同研究センター 教授

回路・アーキテクチャ

桜井貴康

東京大学国際産学共同研究センター教授

川口博

東京大学国際産学共同研究センター技術官

稲垣賢一

東京大学生産技術研究所技術官

リー・ソンス

日本学術振興会研究員ポスドク研究員

シン・ヨンス

日本学術振興会研究員ポスドク研究員

黒田忠広

慶応義塾大学理工学部電子工学科助教授

デバイス・プロセス

平本俊哉

東京大学VDEC助教授

更屋拓哉

東京大学生産技術研究所技術官

イム・ヒュンシク

日本学術振興会研究員ポスドク研究員

ばらつき・CAD

小野等秀俊

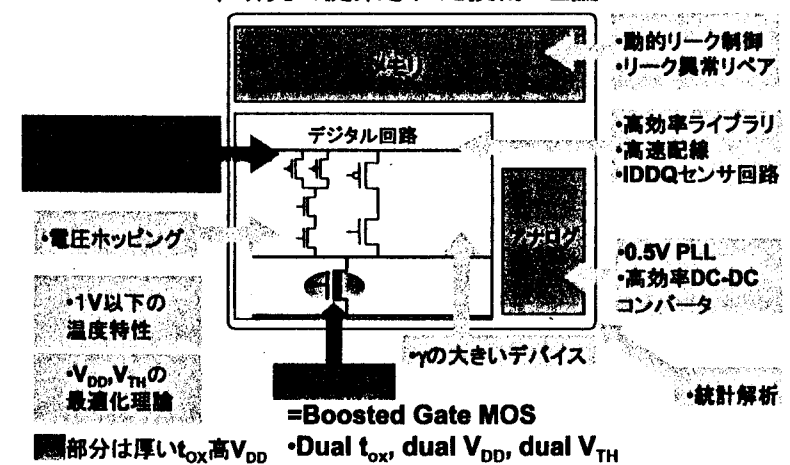
京都大学大学院工学研究科教授

は第165委員会のメンバーを示す

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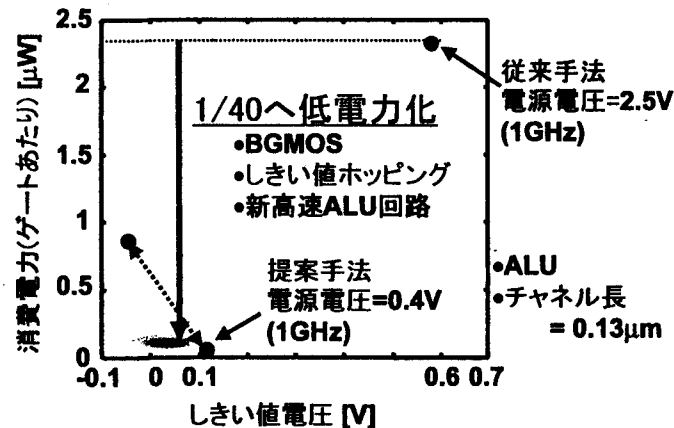
0.5V極低消費電力システムLSI像

—本研究で提案された技術・理論—



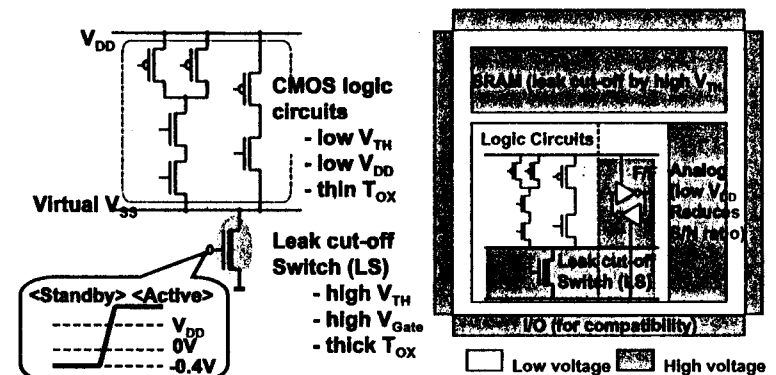
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0.5V高速システムLSIの基本技術



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Dual T_{ox} , dual V_{DD} , dual V_{TH} Device / circuit cooperative approach for low-power

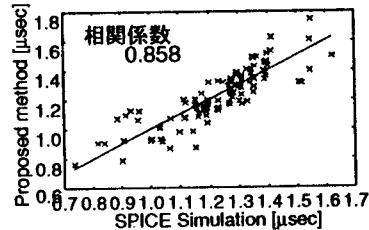
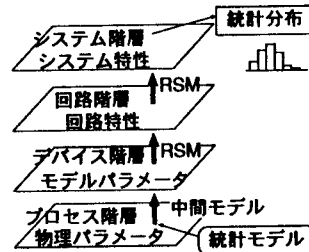


T.Inukai, M.Takamiya, K.Nose, H.Kawaguchi, T.Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC'00, May 2000.

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大規模集積回路の階層的統計解析

- 大規模回路の階層化
- 各階層における統計解析と最適化
- 階層間の統計情報の受渡し
→中間モデル、
応答曲面モデル(RSM)
- プロセス階層の物理パラメータの
ばらつきからシステム特性の変動
を予測



PLLのロックアップ時間の解析例
解析時間
モンテカルロ解析(サンプル数100)
SPICE 34.6時間
提案手法 30分

未来開拓学術研究推進事業研究状況等中間報告

学術への貢献

発表論文

発表済み 50件

投稿中 10件

国際学会、国際シンポジウム等の招待講演

開催済み 15件

開催予定 3件

受賞、新聞報道等特記事項

8件

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発表リスト

	国際学会	論文誌	特許
しきい値ホッピング	CICC	TVLSI(予定)	○
BGMOS	CICC	JSSC(投稿中)	○
電圧ホッピング関連	ASPDAC, DAC, CICC, ISCAS	TVLSI(予定)	○
しきい値ホッピング用デバイス	SSDM, ISLPED	JJAP	
γの大きなデバイス	IEDM	TED(採択決定)	○
低VDD温度特性	CICC	JSSC	
統計解析	ASPDAC	IEICE	
その他	ISLPED, ISSCC, VLSI		○

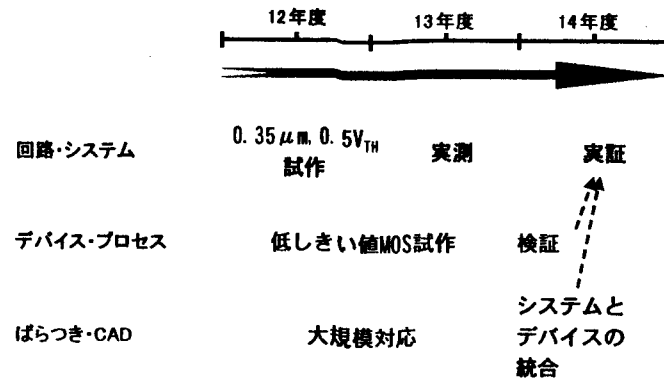
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工業所有権(特許)

- 低電力用システム制御装置(V_{DD} ホッピング)
発明者: 桜井貴康、李誠洙、平林雅之
平成11年10月22日出願、出願国: 日本
- 電力制御装置及び方法並びに電力制御プログラムを記録した記録媒体(V_{TH} ホッピング)
発明者: 桜井貴康、川口博、野瀬浩一
平成12年7月24日出願、出願国: 日本
- しきい値電圧を制御するMOSTランジスタを有する回路及びしきい値電圧制御方法(EIB-DTMOS)
発明者: 平本俊郎、高宮真
平成11年3月5日出願、出願国: 日本、米国
- 半導体集積回路(BGMOS)
発明者: 平本俊郎、桜井貴康、犬飼貴士
平成11年10月27日出願、出願国: 日本、米国

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今後の予定



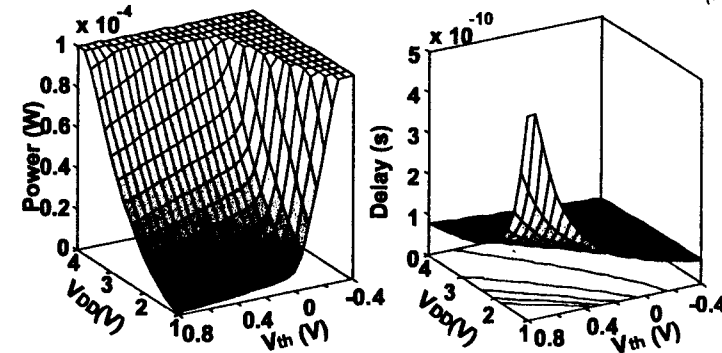
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電力, 遅延の電圧V_{DD}, しきい値V_{TH}依存性

電力 = 充放電電力 + リーク電力

$$= a \cdot f \cdot C_L \cdot V_{DD}^2 + b \cdot 10^{-12} \cdot V_{DD} + \text{ゲートリーク}$$

$$\text{遅延} = \frac{k \cdot Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^\alpha} \quad (\alpha=1.3)$$



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Controlling V_{DD} and V_{TH} for low power

Low power → Low V_{DD} → Low speed → Low V_{TH} → High leakage → V_{DD}-V_{TH} control

	Active	Stand-by
Multiple V _{TH}	Dual-V _{TH}	MTCMOS
Variable V _{TH}	V _{TH} hopping	VTCMOS
Multiple V _{DD}	Dual-V _{DD}	
Variable V _{DD}	V _{DD} hopping	

Software-hardware cooperation

Techno-physical cooperation

- *) MTCMOS: Multi-Threshold CMOS
- *) VTCMOS: Variable Threshold CMOS
- Multiple : spatial assignment
- Variable : temporal assignment

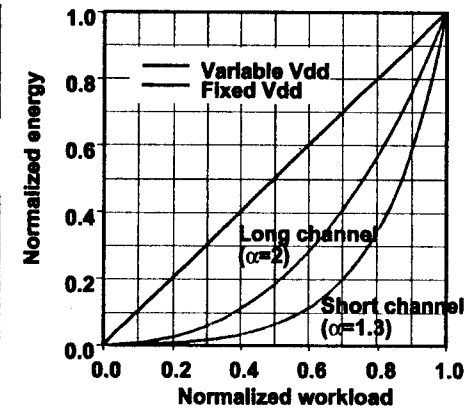
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If you don't need to hussle, V_{DD} should be as low as possible

Energy consumption is proportional to the square of V_{DD}.

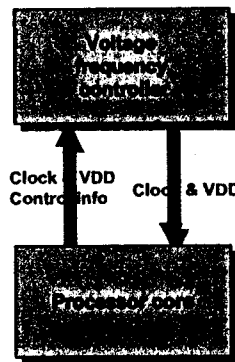


V_{DD} should be lowered to the minimum level which ensures the real-time operation.



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システム・回路の協調によるアプローチ

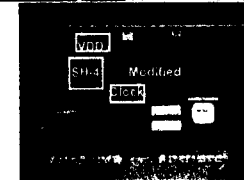
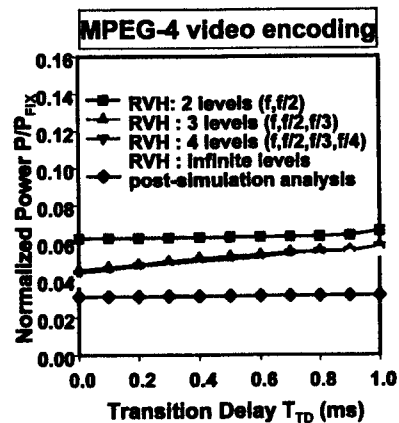


S.Lee and T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications," ASPDAC'00, A5.2, pp.381--pp.386, Jan. 2000.

S.Lee and T.Sakurai, "Run-time Voltage Hopping for Low-power Real-time Systems," DAC'00, June 2000.

T. Sakurai

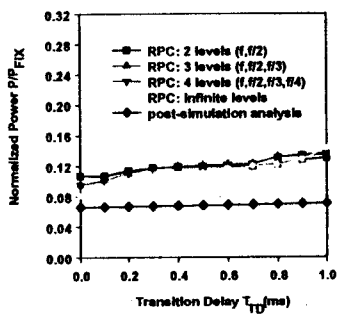
リアルタイム画像エンコードを 電圧ホッピングで電力1/10を達成



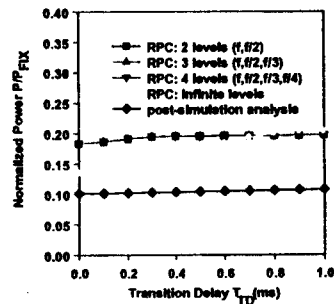
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Simulation results

MPEG-2 video decoding

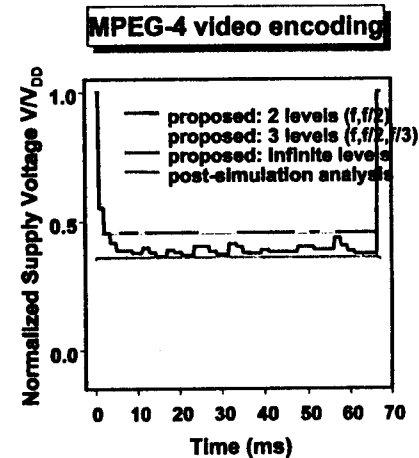


VSELP speech encoding



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Transient voltage waveform



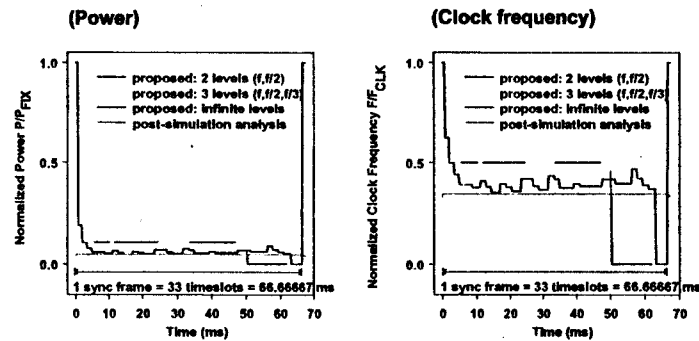
Simulation results

1 sync frame = 33 timeslots = 66.66667 ms

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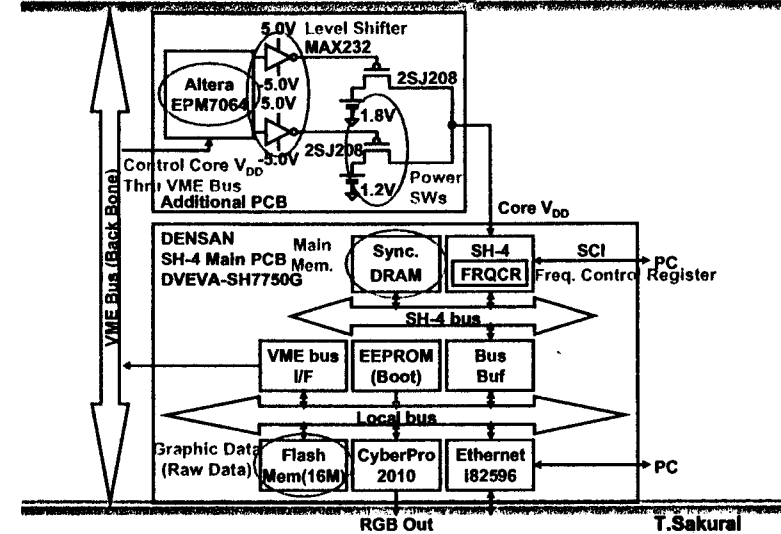
Transient power & frequency

Transient characteristics in a sync frame



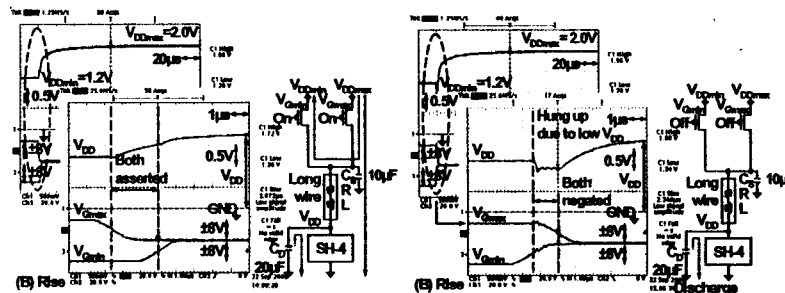
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Block Diagram



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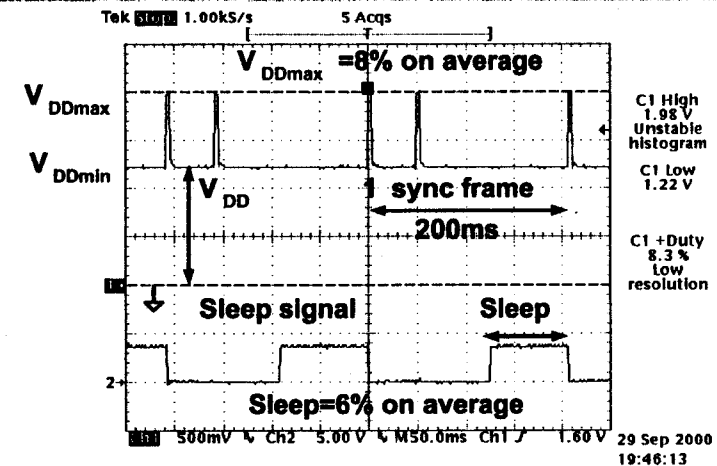
VDD waveforms



Normal

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Measured voltage waveforms

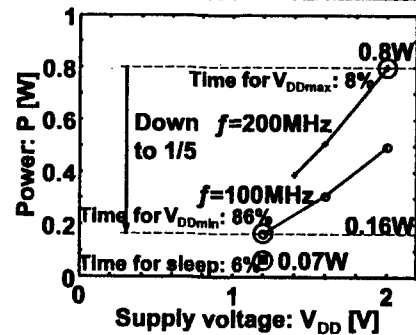


29 Sep 2000
19:46:13

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Measured power characteristics

Total power = $0.8 \times 0.08 + 0.16 \times 0.16 + 0.07 \times 0.06 = 0.2W$

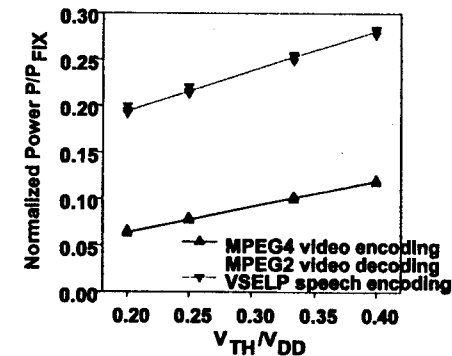


VDD/hopping can cut down power consumption to 1/4

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V_{TH} dependence

- Power saving ratio: approximately linear function of V_{TH}/V_{DD} for various ranges of V_{TH} and V_{DD}



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Power Conscious RT/OS and Application Slicing for Low-Power Embedded Real-Time Systems

Y.Shin & T.Sakurai, "Cooperative Voltage Scaling (CVS) between OS and Applications for Low-Power Real-Time Systems," CICC'01, to be published, May 2001.

T.Sakurai

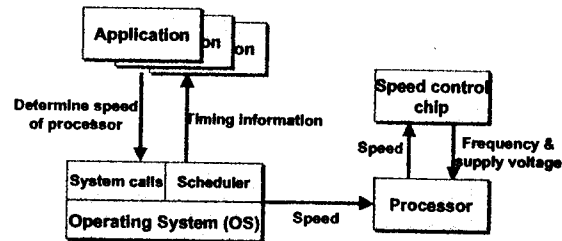
Introduction (cont'd)

- Motivation
 - Reducing power consumption of processor = exploiting idle time
 - OS has better knowledge about idle time due to task interaction
 - Application has better knowledge about idle time due to execution time variation
- Our approach
 - Cooperation of OS and applications
 - Sub-divide each application into a sequence of slices

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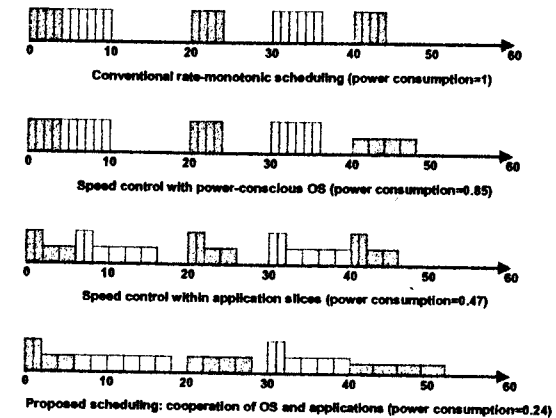
Power Conscious OS & Application Slicing

• Structural view



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Power Conscious OS & Application Slicing (cont'd)



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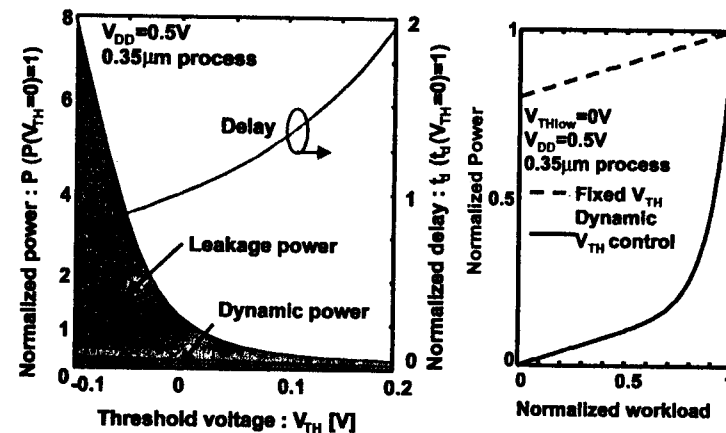
Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
Multiple V_{TH}	Dual- V_{TH}	MTCMOS
Variable V_{TH}		VTCMOS
Multiple V_{DD}	Dual- V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

K. Nose, M.Hirabayashi, H.Kawaguchi, S.Lee and T.Sakurai, "VTH-hopping Scheme for 82% Power Saving in Low-voltage Processors," to be published, CICC 2001.

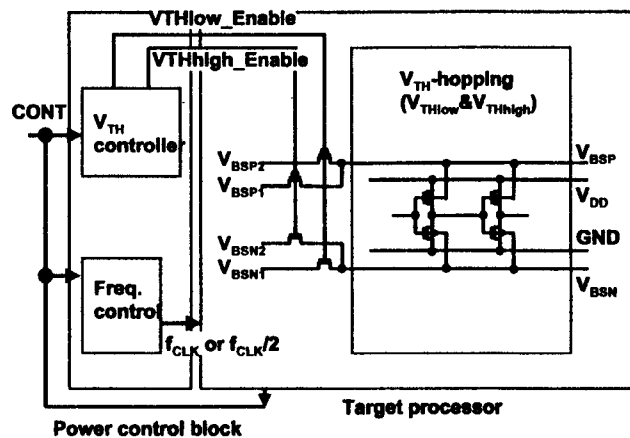
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V_{TH} -hopping



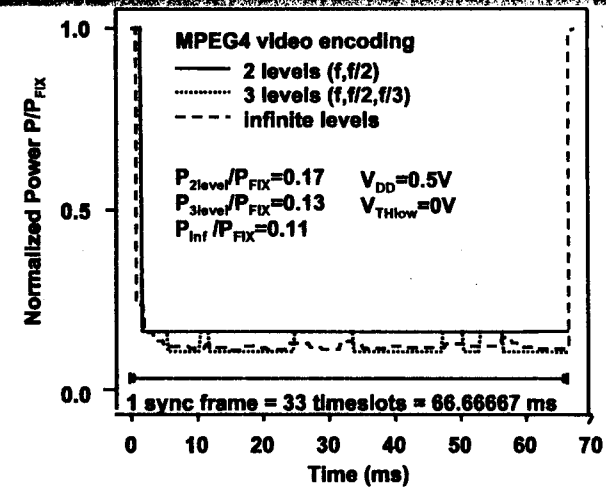
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Schematic of V_{TH} -hopping



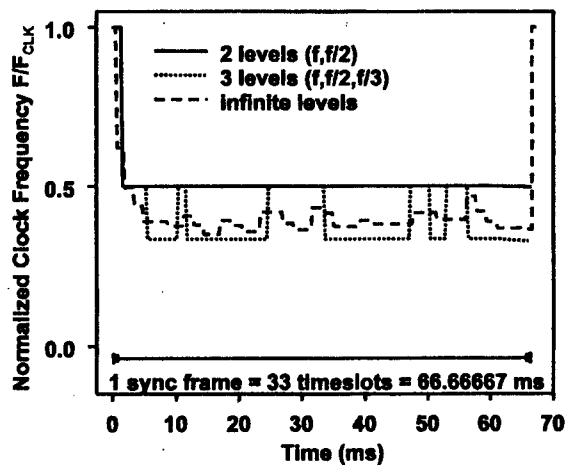
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Power transition of V_{TH} -hopping



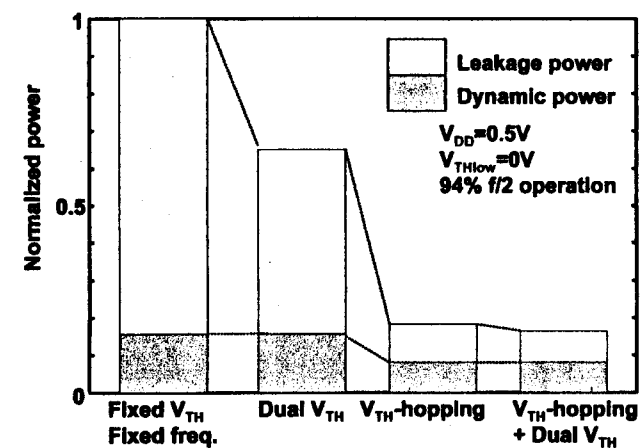
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Frequency transition of V_{TH} -hopping



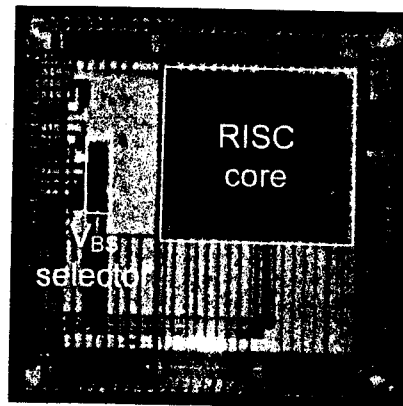
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Power comparison



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Microphotograph of RISC processor



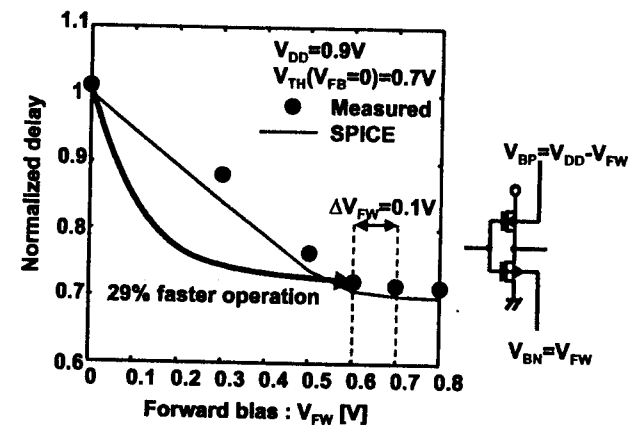
0.6 μ m process

Overhead of V_{TH} -hopping
= 14%

RISC core
= 2.1mm x 2.0mm
 V_{BS} selector
= 0.2mm x 0.6mm

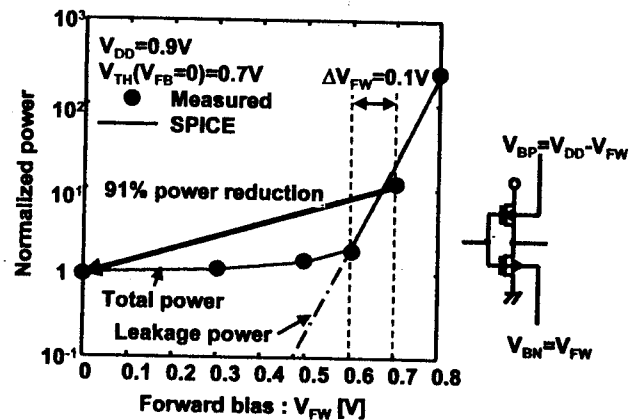
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Measurement results (Delay)



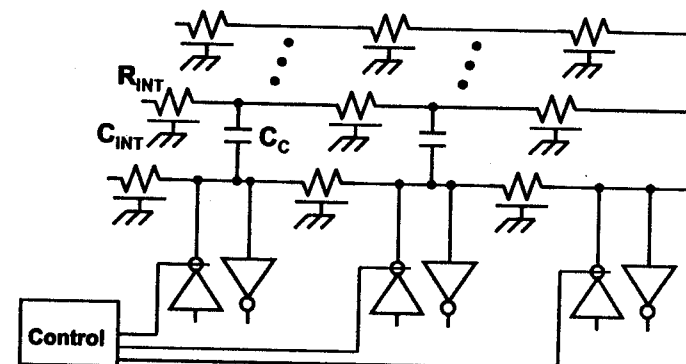
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Measurement results (Power)



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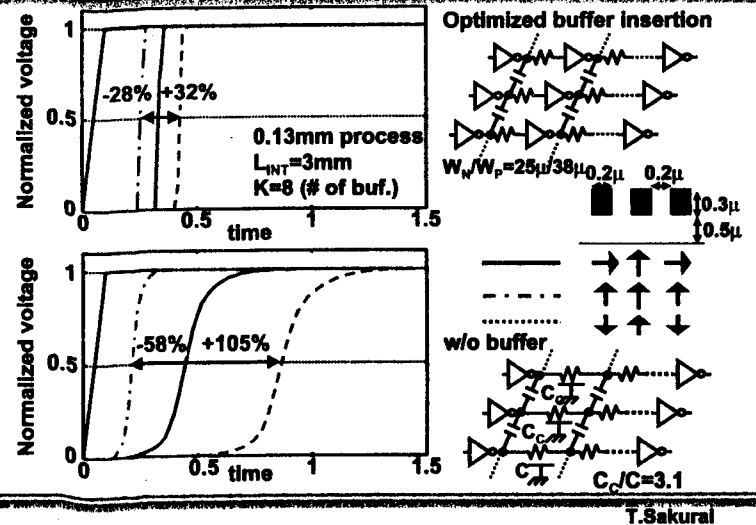
Conventional bus circuit



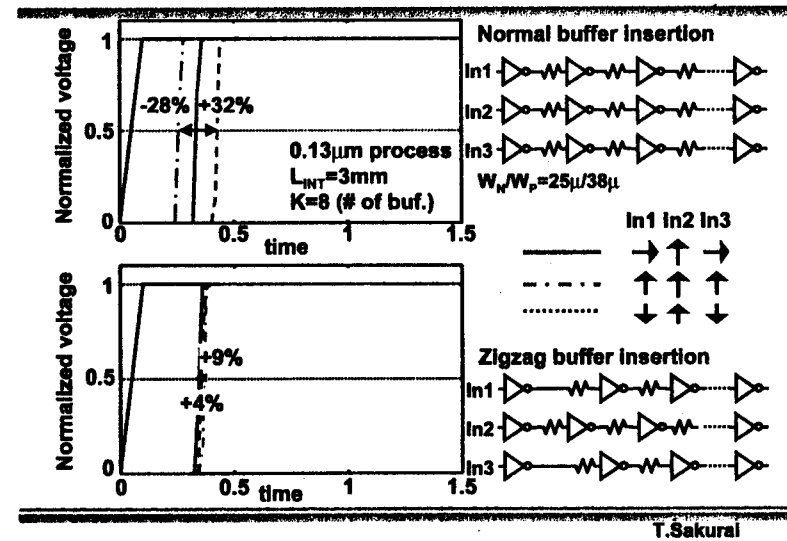
- Bi-direction $\rightarrow$ buffer insertion is difficult.
- $\text{delay} \propto (\text{interconnection length})^2$

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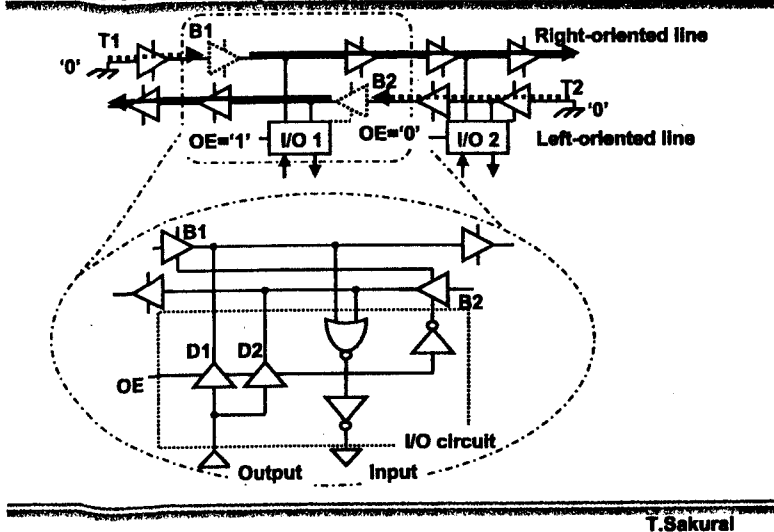
Delay fluctuation by coupling capacitance



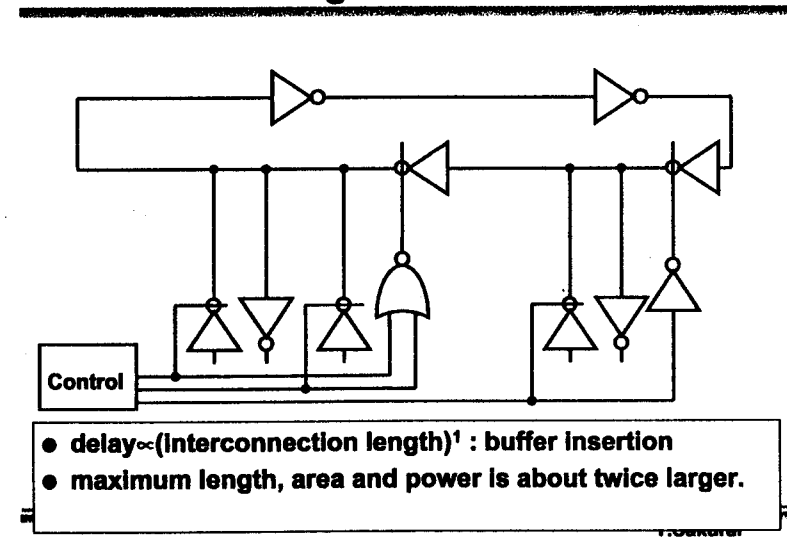
Zigzag buffer insertion



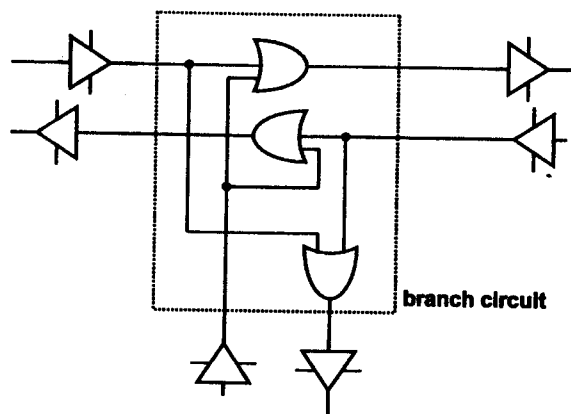
Dual-rail bus (DRB) for bi-directional buses



Ring bus circuit

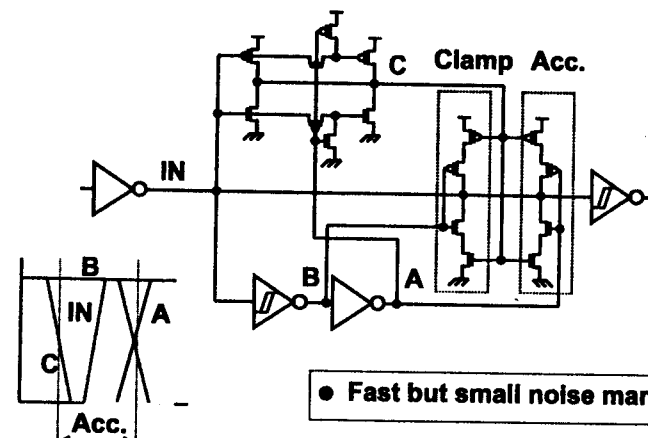


Branch circuit for dual-rail bus



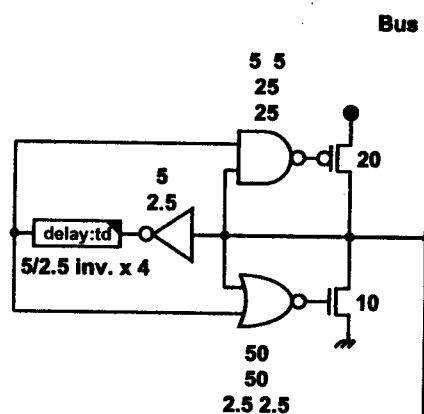
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Transient sensitive accelerator (TSA)



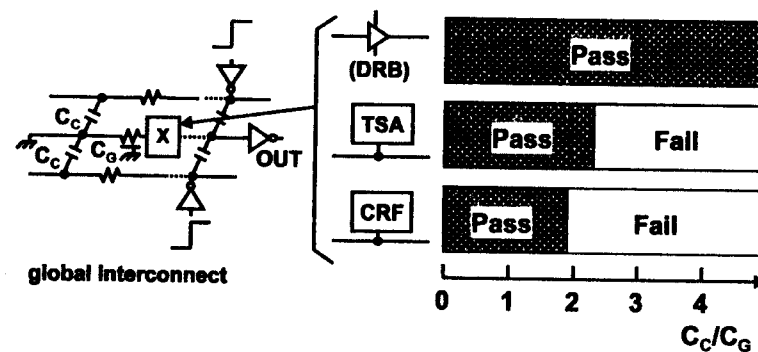
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Self-timed complementary regenerative feedback repeater (CRF)



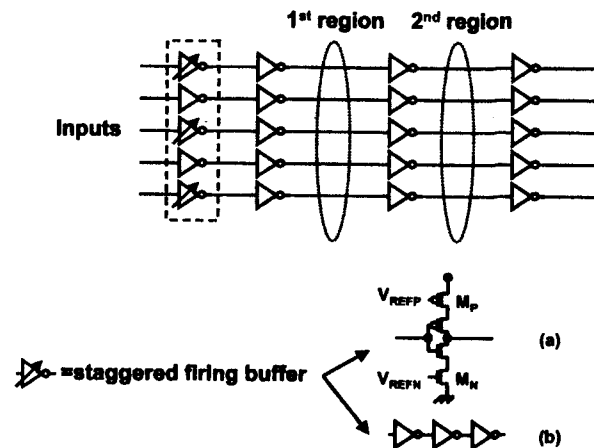
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Noise resiliency comparison



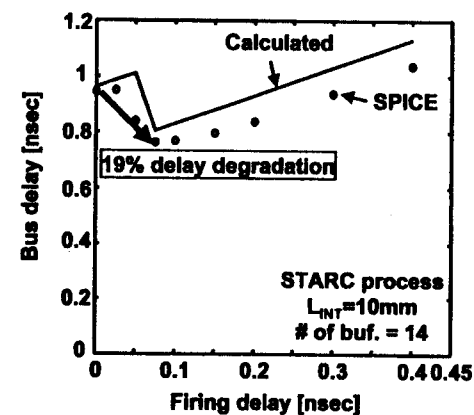
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Staggered firing bus (SFB) scheme



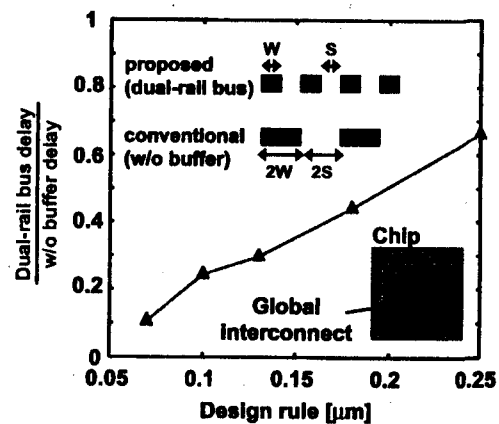
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Simulation result of staggered firing bus



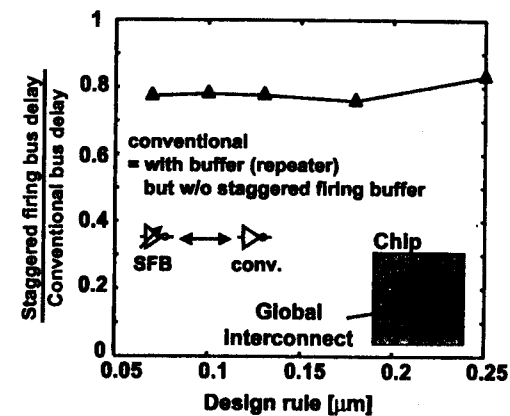
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SPICE simulation of benefit of DRB



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SPICE simulation of benefit of SFB



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Coupling-Driven Bus Design for Low-Power Application-Specific Systems

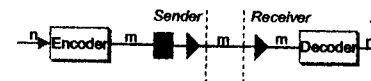
Youngsoo Shin and Takayasu Sakurai
Center for Collaborative Research and Institute of
Industrial Science
University of Tokyo

Y. Shin and T. Sakurai, "Coupling-driven bus design for low-power application-specific systems,"
to appear in Proc. Design Automation Conf. (DAC), June 2001.

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Introduction

- Low-power bus coding
 - Mostly for off-chip buses
 - Reducing number of transitions
 - Low transition encoding at the sender & decoding at the receiver
 - Tradeoff between coding logic and power



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Introduction

- VLSI scaling
 - Increasing wire-to-wire capacitance
 - Power consumption of global buses are determined by effects from wire-to-wire cap. and area and load cap.
- On-chip bus coding
 - Reducing number of transitions and effects from wire-to-wire capacitance
 - Extension of bus-Invert code [cicc2000, lccad2000, aspdac2001]: applicability is questionable due to overhead (delay and power)

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Bus Shuffling

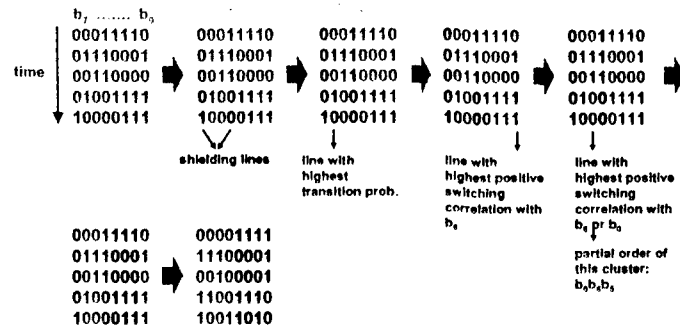
- Bus shuffling
 - Virtually no overhead
 - Pattern information is necessary: applicable to special-purpose systems
 - Layout modification or compiler backend support
- Problem definition
 - Given a set of patterns or statistics of patterns
 - Find order of bus lines so that power consumption due to area and coupling capacitances is minimized

Y. Shin and T. Sakurai, "Coupling-driven bus design for low-power application-specific systems,"
to appear in Proc. Design Automation Conf. (DAC), June 2001.

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Bus Shuffling

• Example

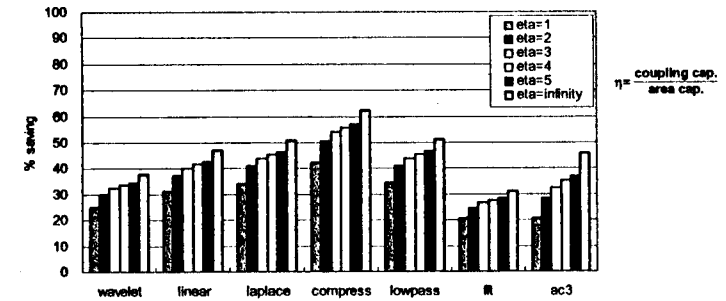


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Experiments

• Result of heuristic

- 7 data address sets
- % power saving compared to un-shuffled buses



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