DA show ‘01

VLSI design challenges and EDA in the forthcoming decade

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Institute of Industrial Science,
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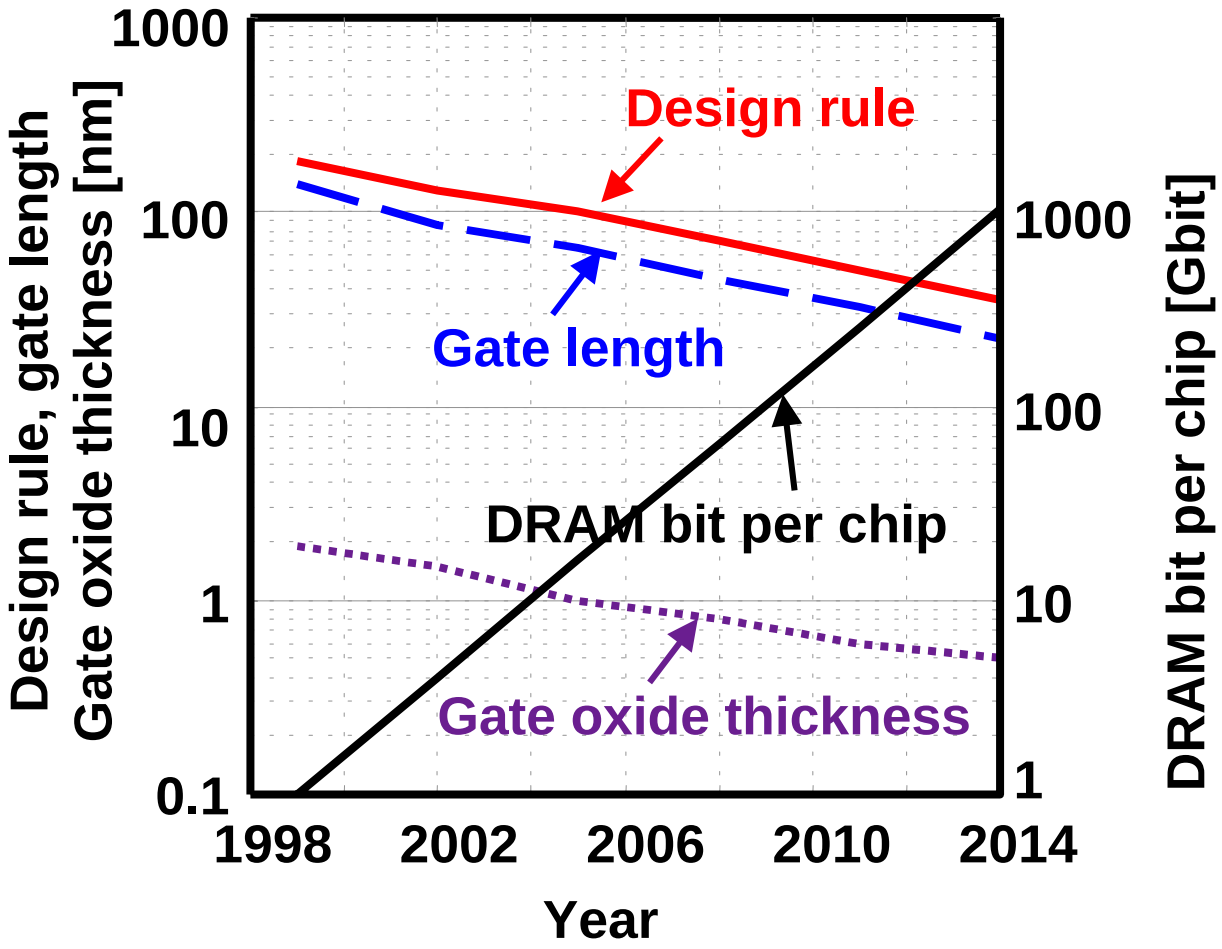
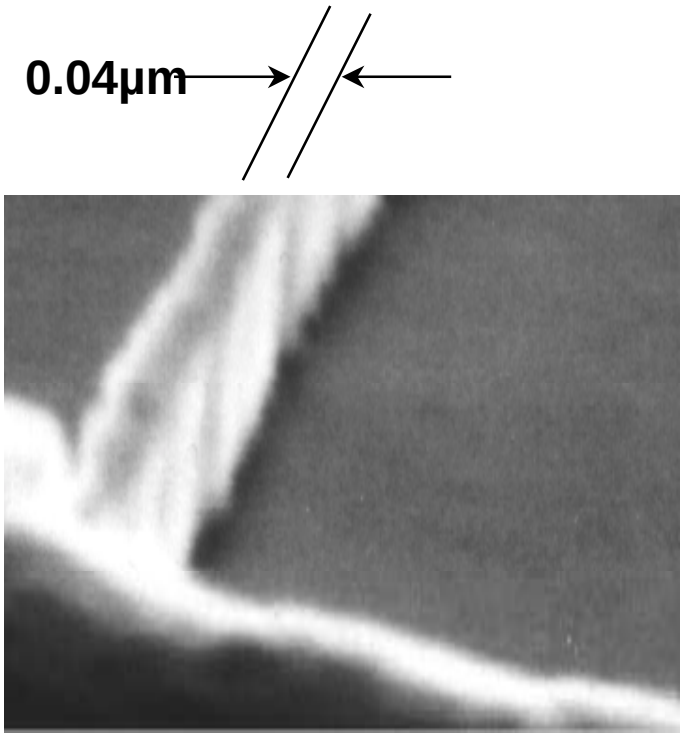
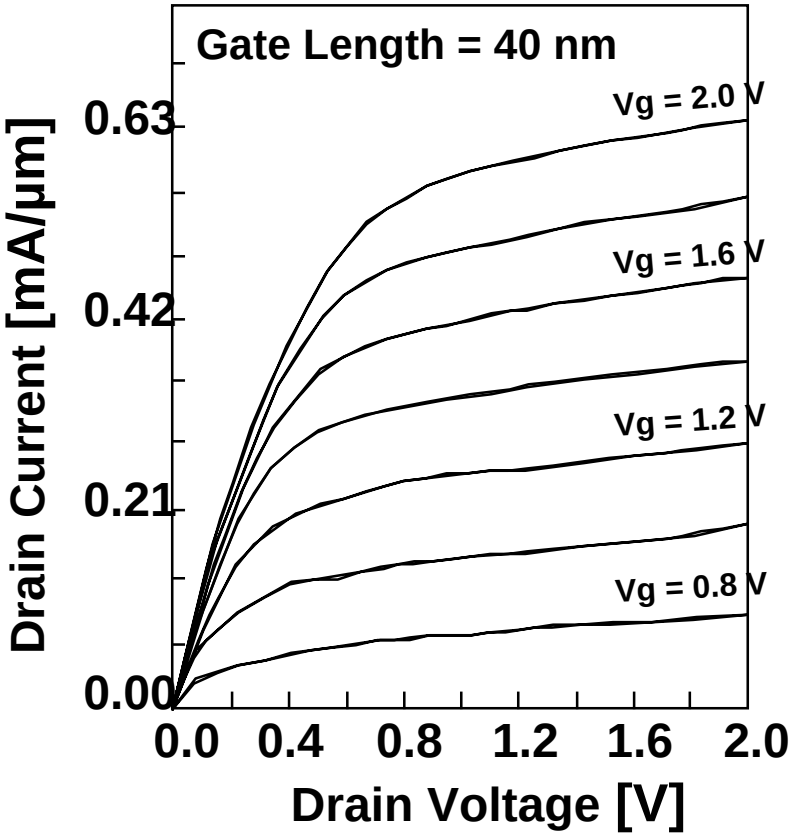
Technology trend



Limit of Miniturization

0.04μm MOSFET



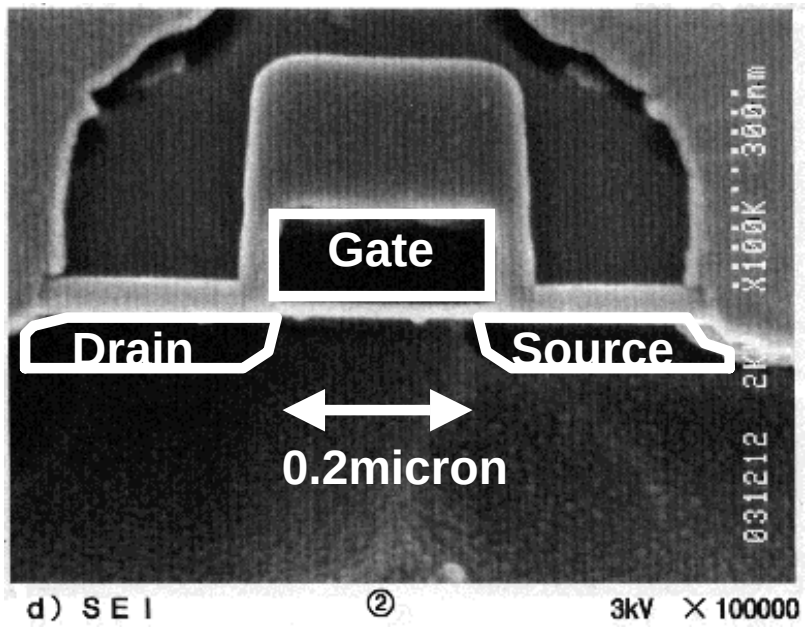


Conventional I-V curve at 0.04μm (Even down to 0.014μm)

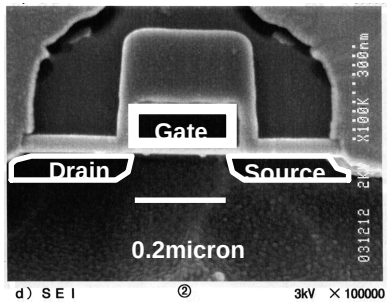
M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50nm gate Length N-MOSFETs with 10 nm Phosphorus Source and Drain Junctions", IEDM Technical Digest, pp. 119 - 122, 1993.

H. Kawaura, T. Sakamoto, Y. Ochiai, J. Fujita, and T. Baba, "Fabrication and Characterization of 14-nm-Gate-Length EJ-MOSFETs", Extended Abstracts of SSDM, pp.572-573, 1997.

Scaling Law



Size 1/2



Favorable effects

Size	x1/2
Voltage	x1/2
Electric Field	x1
Speed	x3
Cost	x1/4

Unfavorable effects

Power density	x1.6
RC delay/Tr. delay	x3.2
Current density	x1.6
Voltage noise	x3.2
Design complexity	x4

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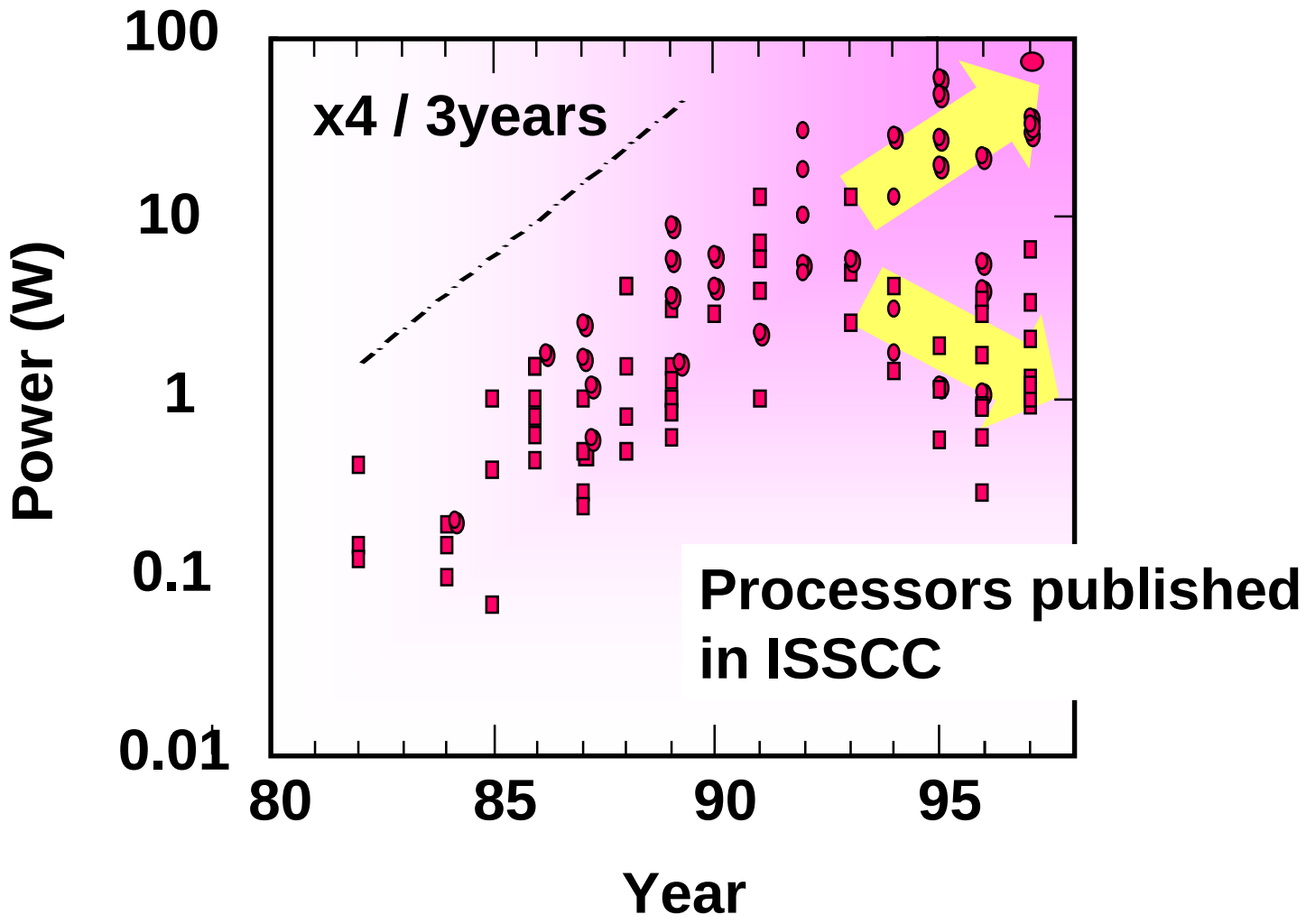
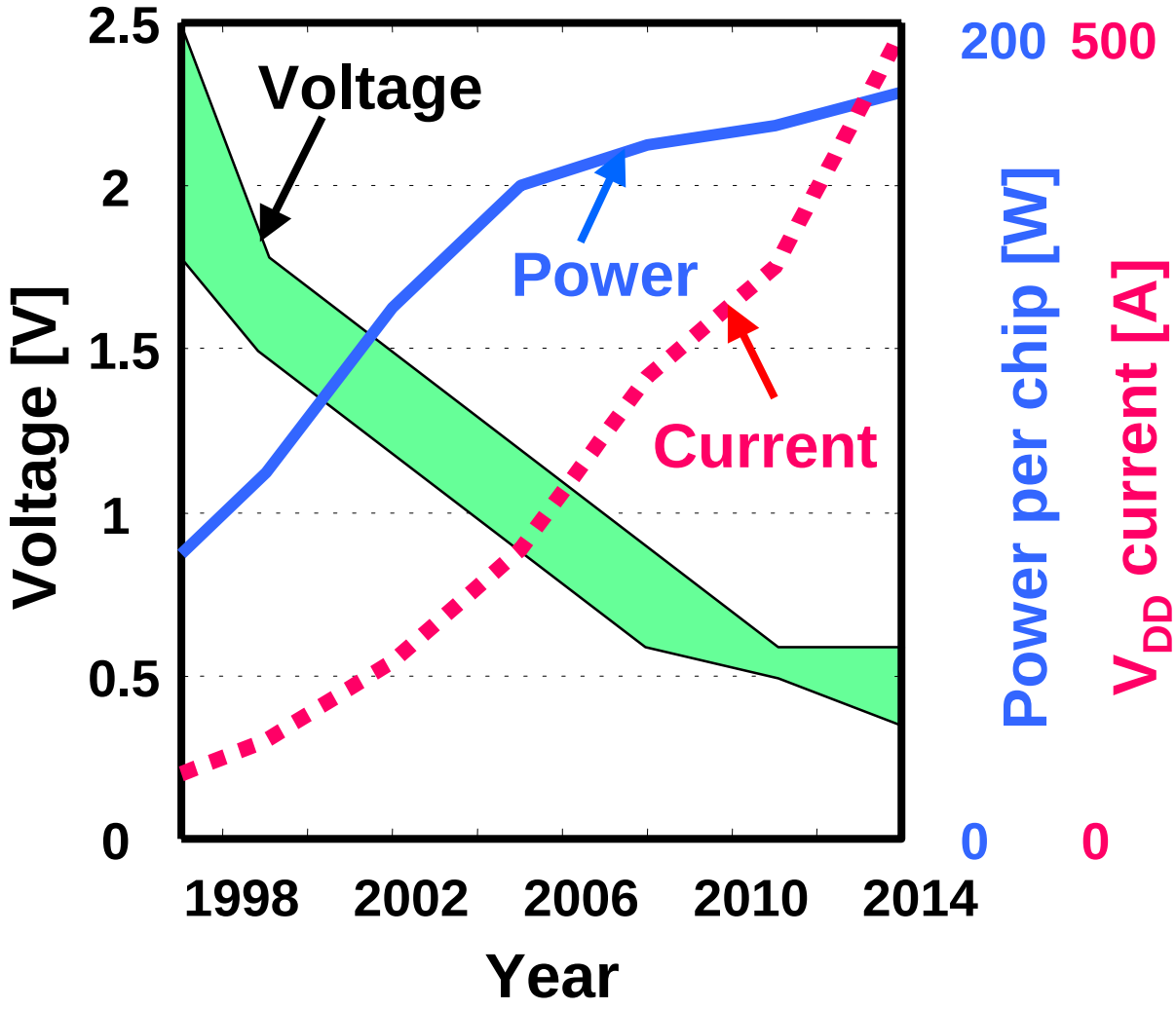
Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

Ever Increasing VLSI Power



V_{DD}, power and current trend



International Technology Roadmap for Semiconductors 1999 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

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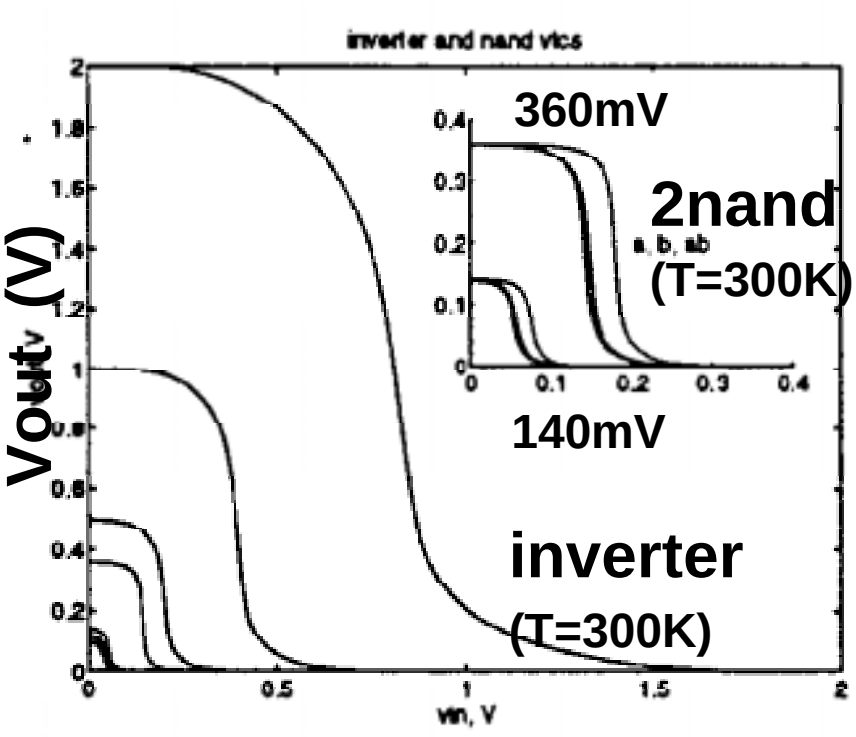
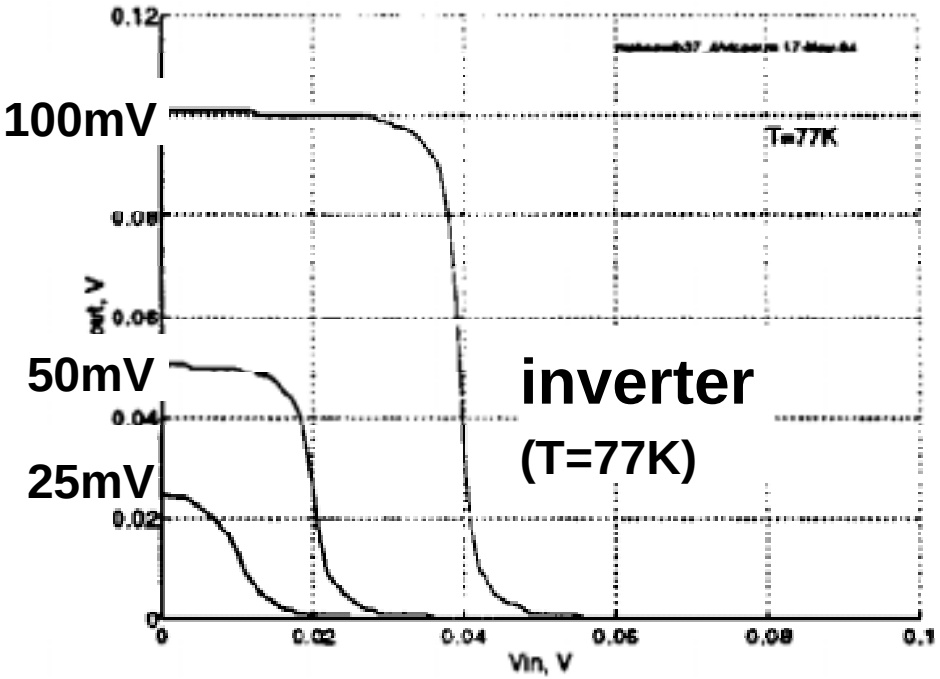
Ultra Low-Voltage Operation

(Stanford Univ.)





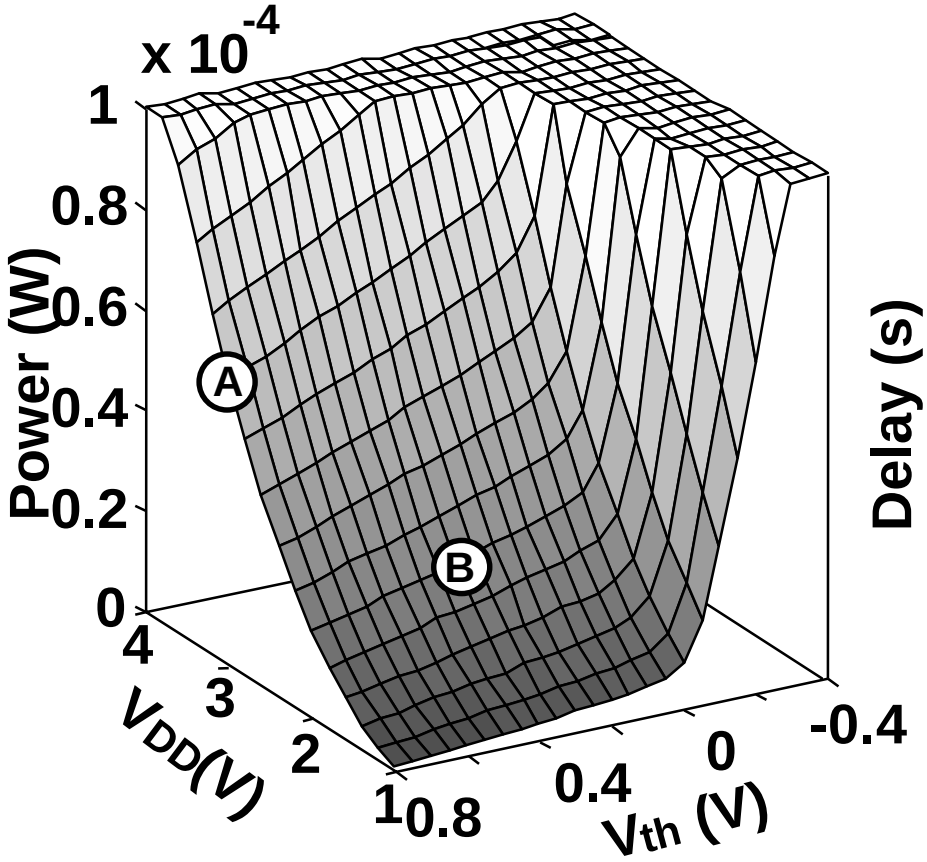
Vin (V)

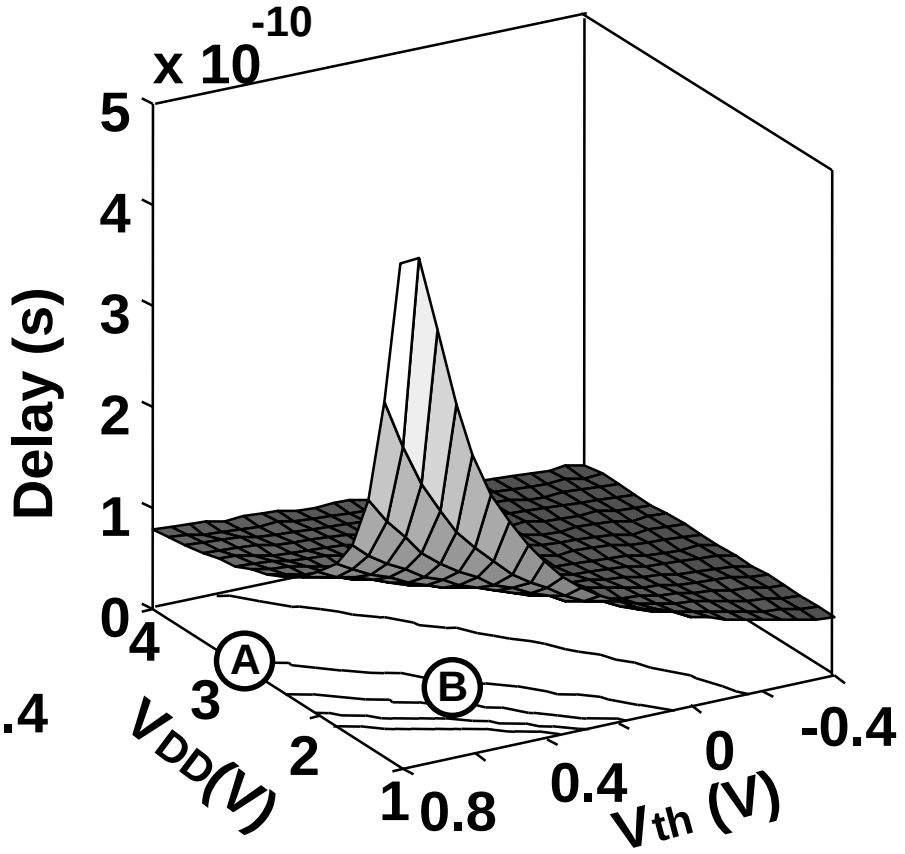
J.Burr&J.Shott,"A 200mV Self-Testing Encoder/Decoder using Stanford Ultra-Low-Power CMOS",ISSCC94, pp.84-85.

Power & Delay Dependence on V_{DD} & V_{TH}

Power : $P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{th}}{S}} \cdot V_{DD}$

Delay $= \frac{k \bullet Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^{\alpha}}$ $(\alpha=1.3)$





Controlling V_{DD} and V_{TH} for low power

Low power → Low V_{DD} → Low speed → Low V_{TH} → High leakage → V_{DD}-V_{TH} control

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Software-hardware cooperation

Technology-circuit cooperation

*) MTCMOS: Multi-Threshold CMOS

*) VTCMOS: Variable Threshold CMOS

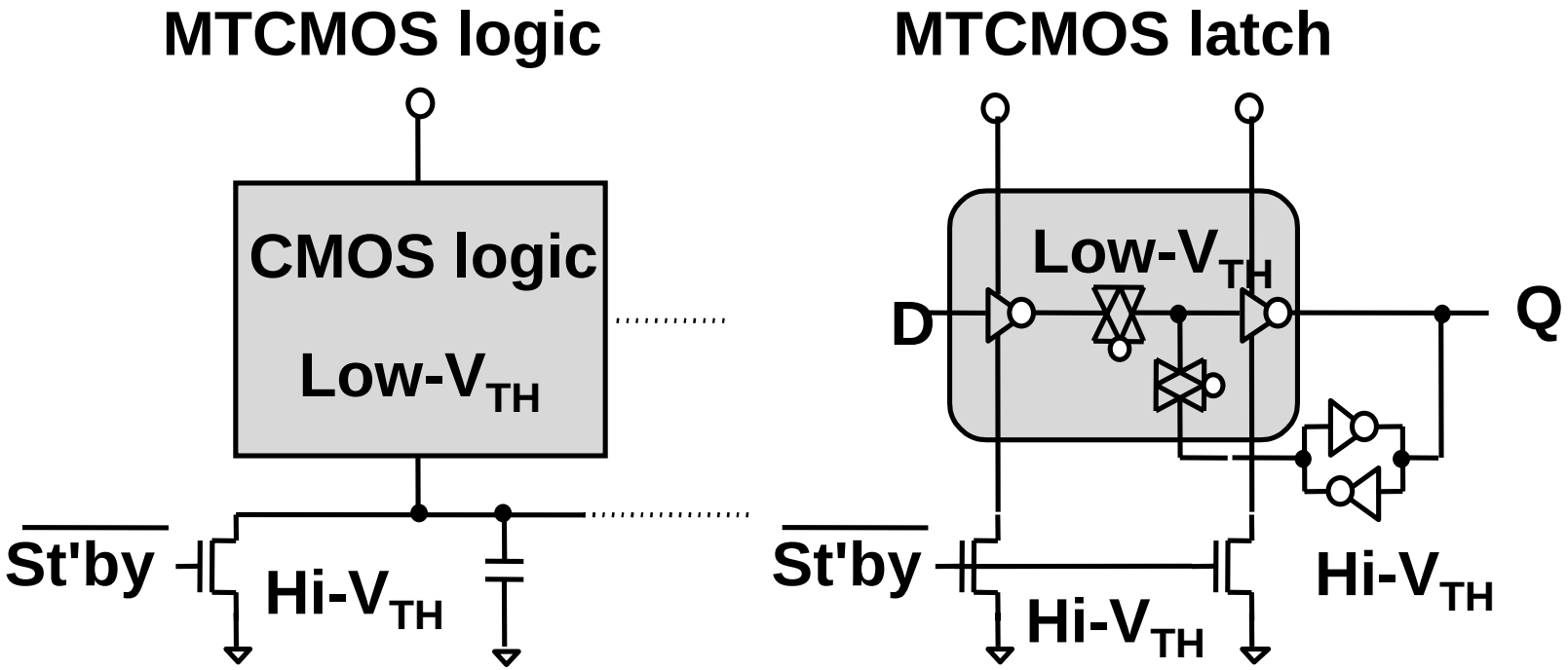
- Multiple : spatial assignment
- Variable : temporal assignment

Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

- MTCMOS: Multi-Threshold CMOS

Multi-Threshold CMOS Circuit

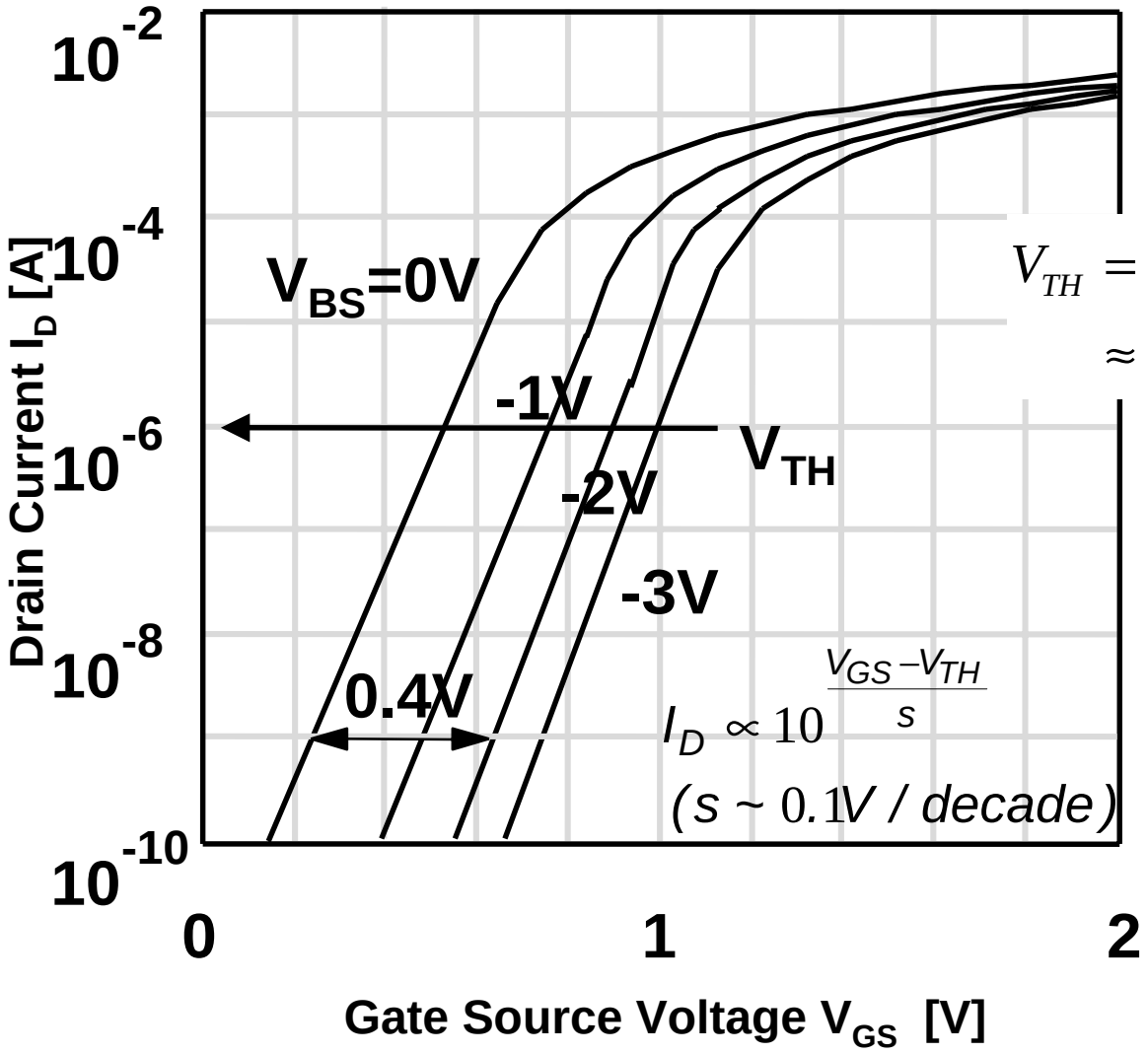


- In active mode, low-V_{TH} (~0.2V) achieve high speed.
- In standby mode when St'by signal is high, high-V_{TH} (~0.6V) MOSFET in series to normal logic circuits cut off leakage current.
- Doesn’t work under 0.8V.

Controlling V_{DD} and V_{TH} for low power

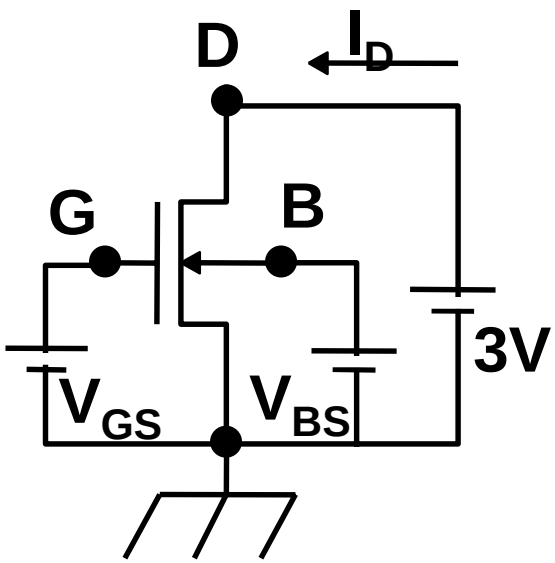
	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Subthreshold current



NMOS **L = 0.3μm**
W = 10μm

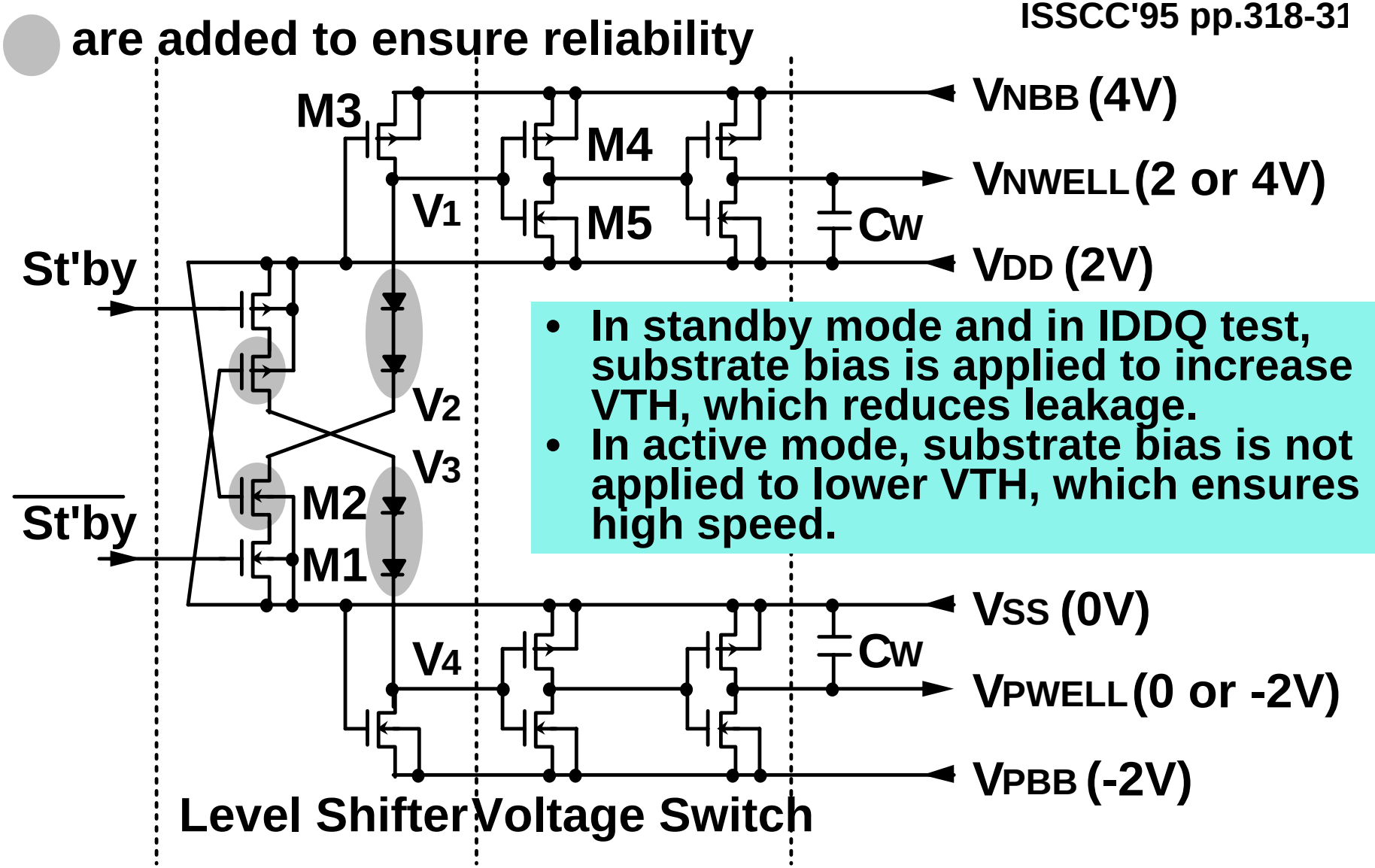
$$V_{TH} = V_{T0} - \gamma\sqrt{2\phi_F - V_{BS}}$$
$$\approx V_{T0} - \gamma_1 V_{BS} \quad (\gamma_1 \approx 0.15 \sim 0.2)$$



Standby Power Reduction (SPR) Circuit

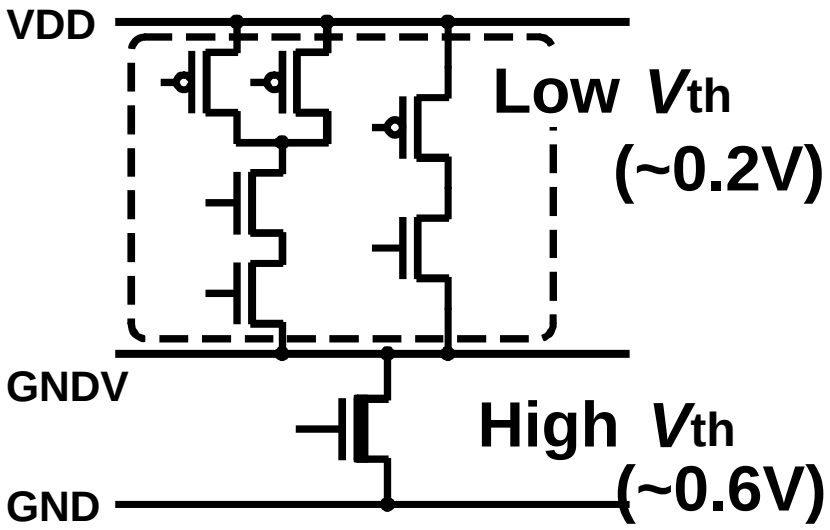
ISSCC'95 pp.318-31

are added to ensure reliability



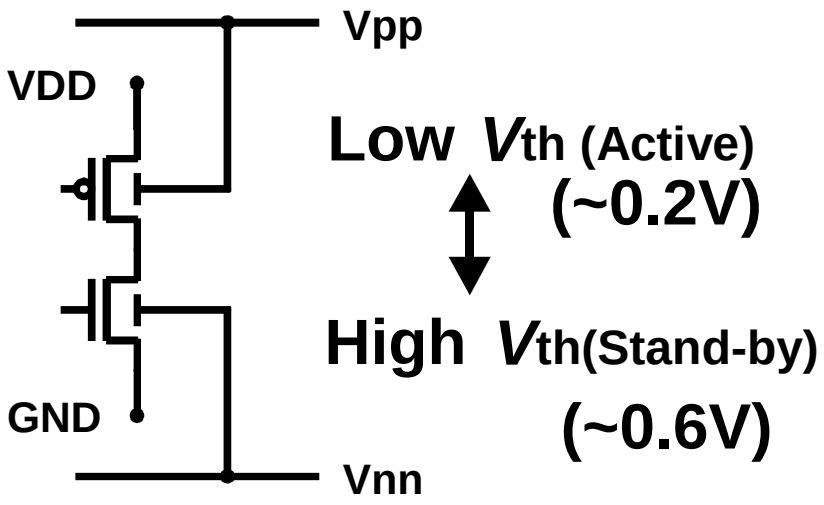
- In standby mode and in IDDQ test, substrate bias is applied to increase VTH, which reduces leakage.
- In active mode, substrate bias is not applied to lower VTH, which ensures high speed.

Previous circuit schemes



MTCMOS [1]

- Tunneling leakage cannot be cut-off.
- Area penalty increases when VDD < 1V.

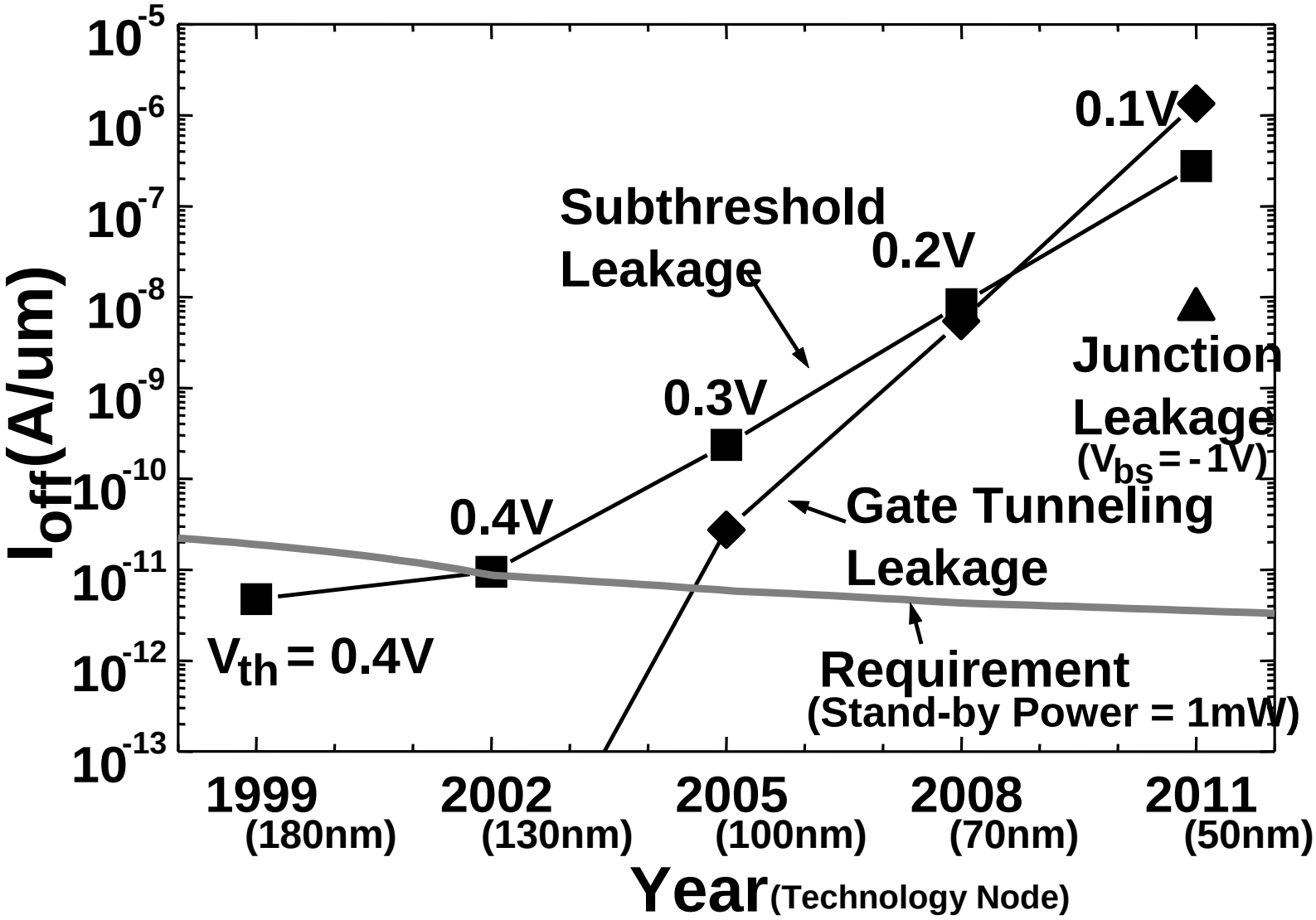


VTCMOS [2]

- Junction leakage increases due to band-to-band tunneling.
- Tunneling leakage is not suppressed.

[1] S.Mutoh *et al*. IEEE, JSSC, 1995. [2] T.Kuroda *et al*. IEEE, JSSC, 1996.

Transistors go leaky



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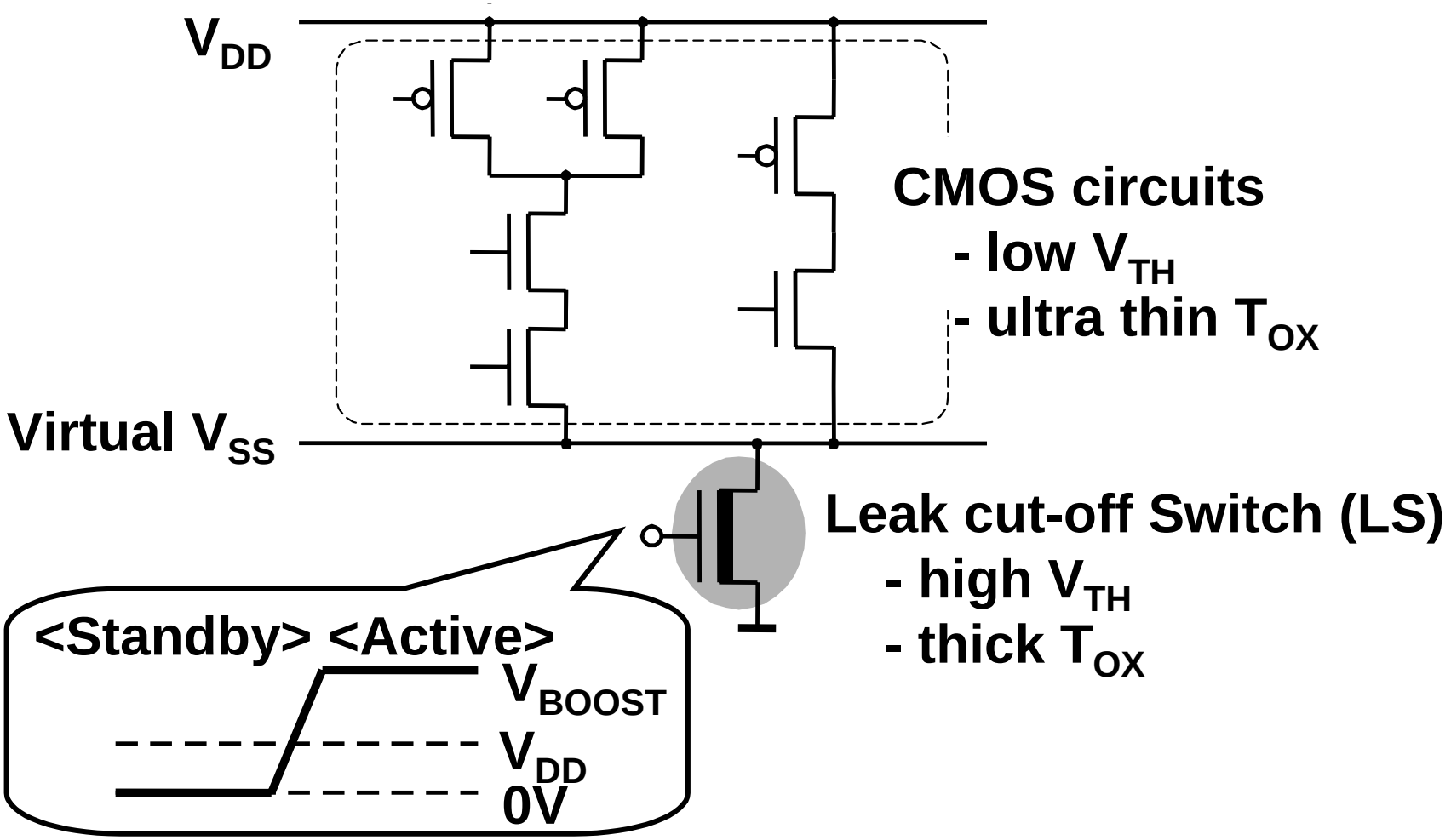
Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	VTCMOS	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

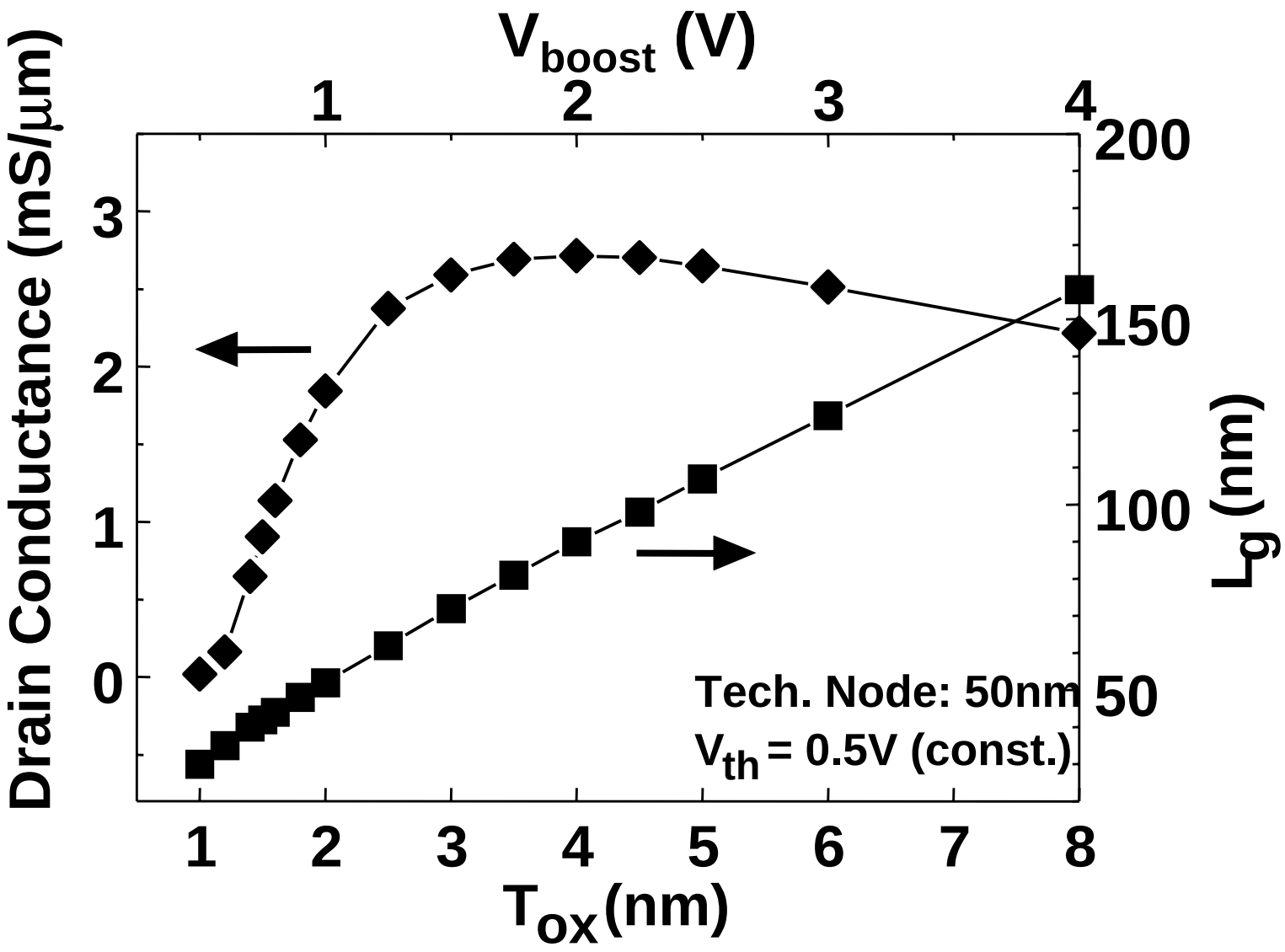
Boosted-Gate MOS (BGMOS)

Device / circuit collaborative approach

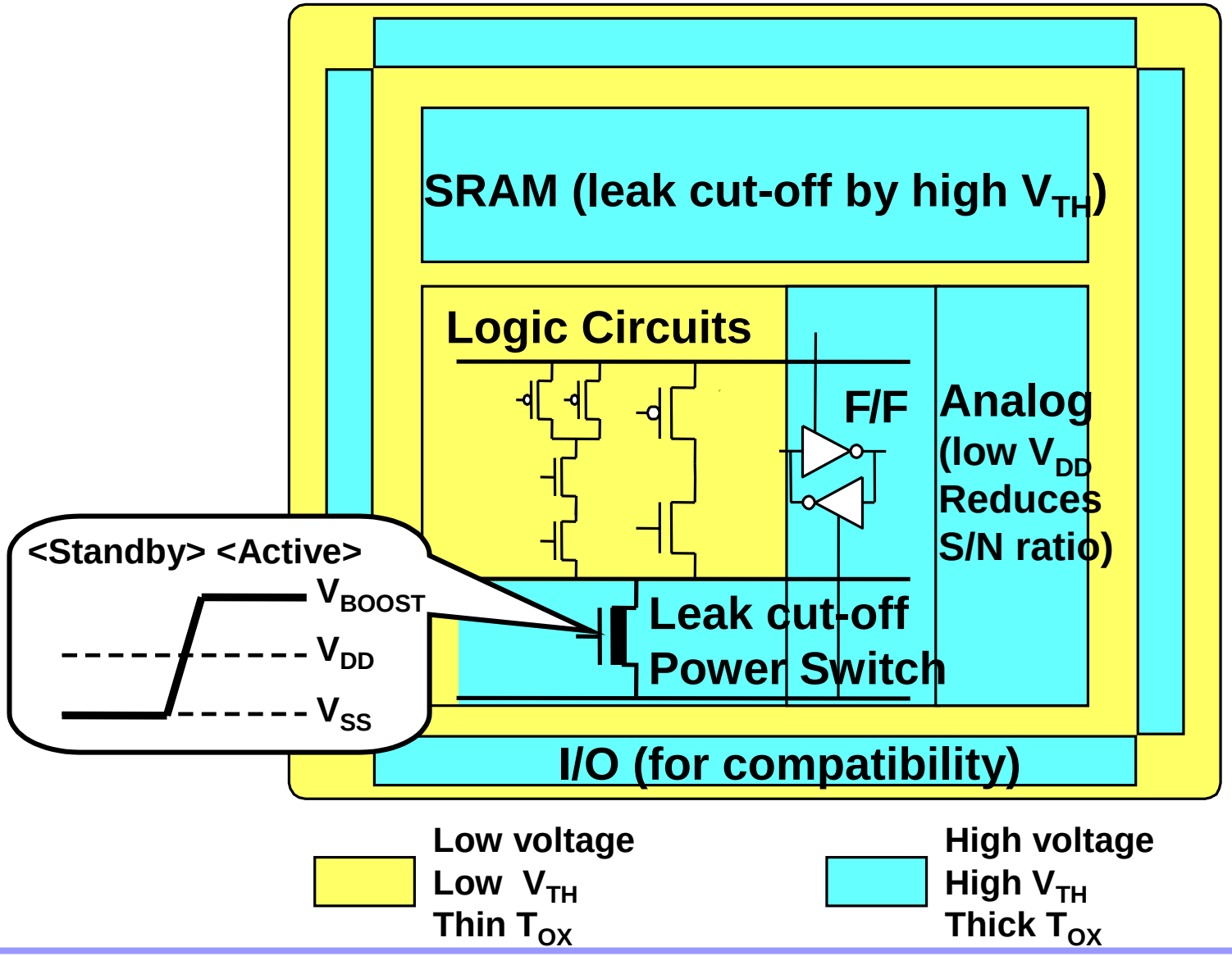


T.Inukai, M.Takamiya, K.Nose, H.Kawaguchi, T.Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC'00, p.409, May 2000.

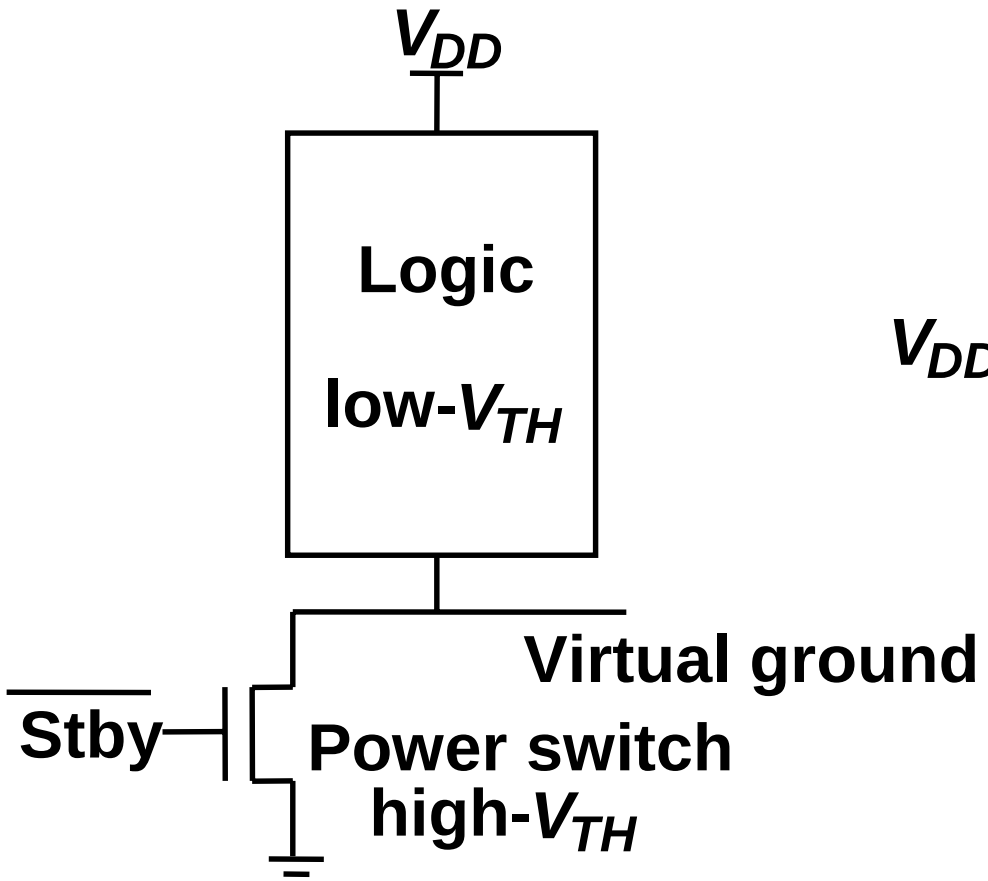
Leak switch optimization

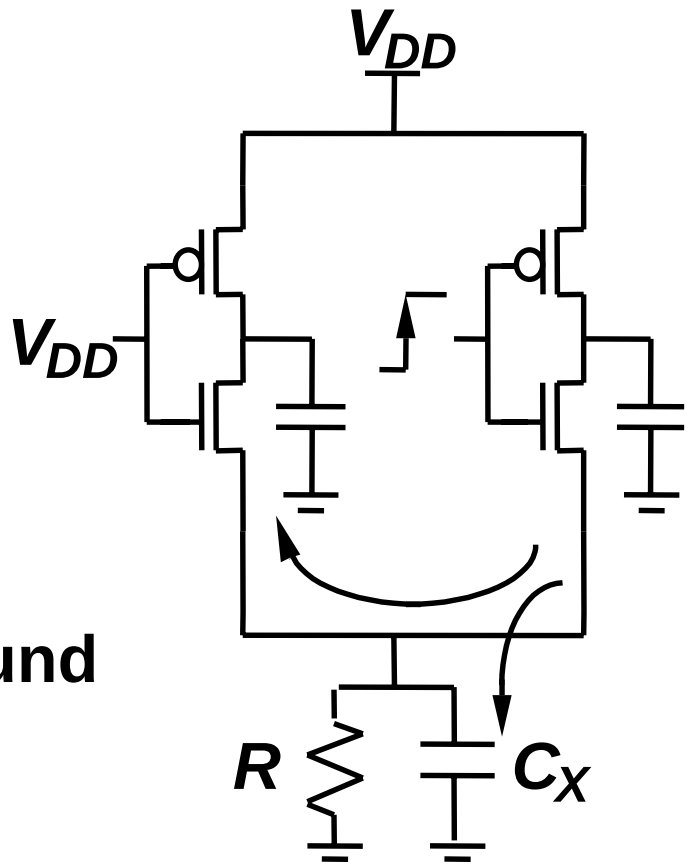


GSI's in deep-submicron era



Power switch gate width in BGMOS





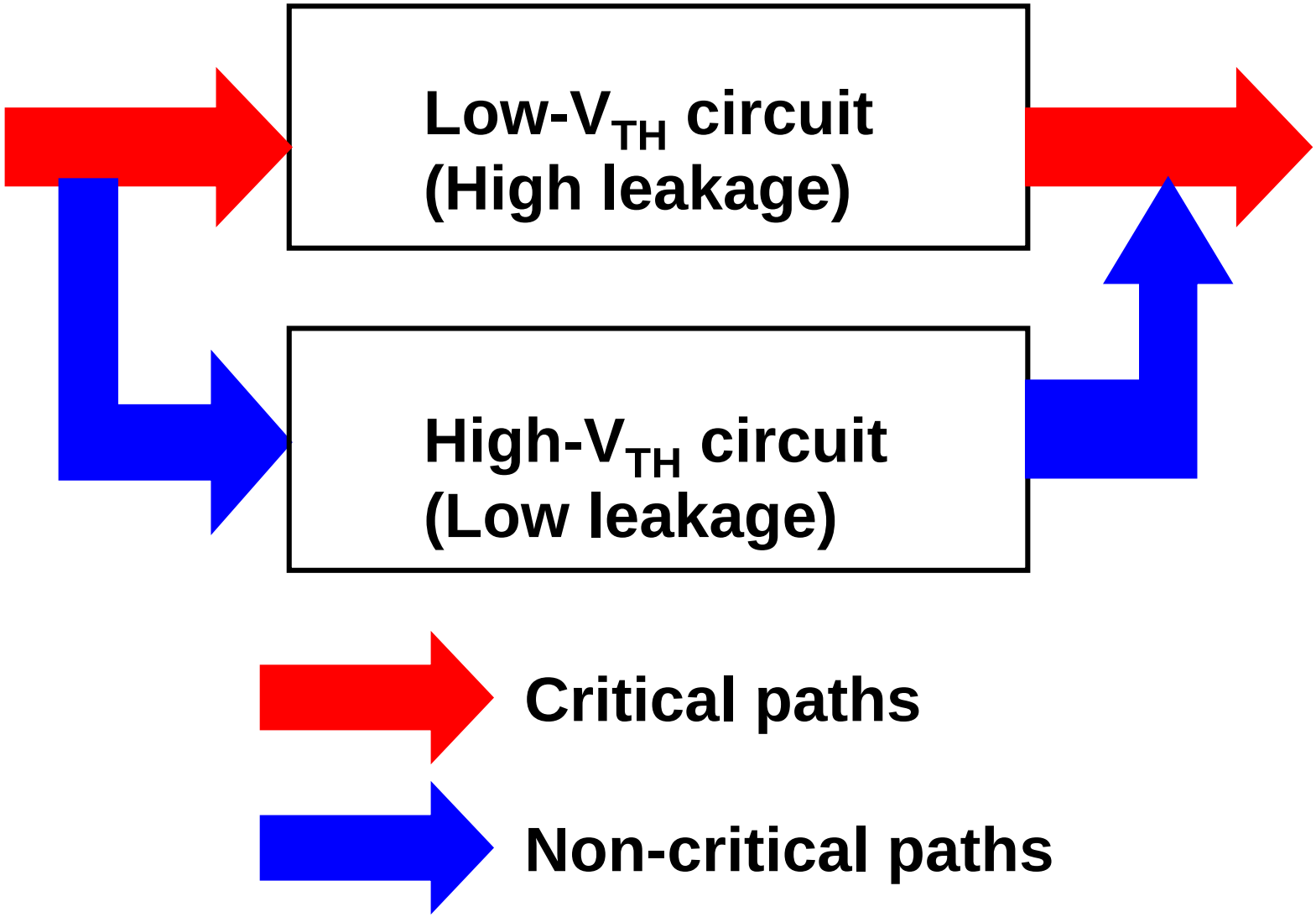
Kao, DAC'97, pp.409-414.

Degrade circuit speed unpredictably

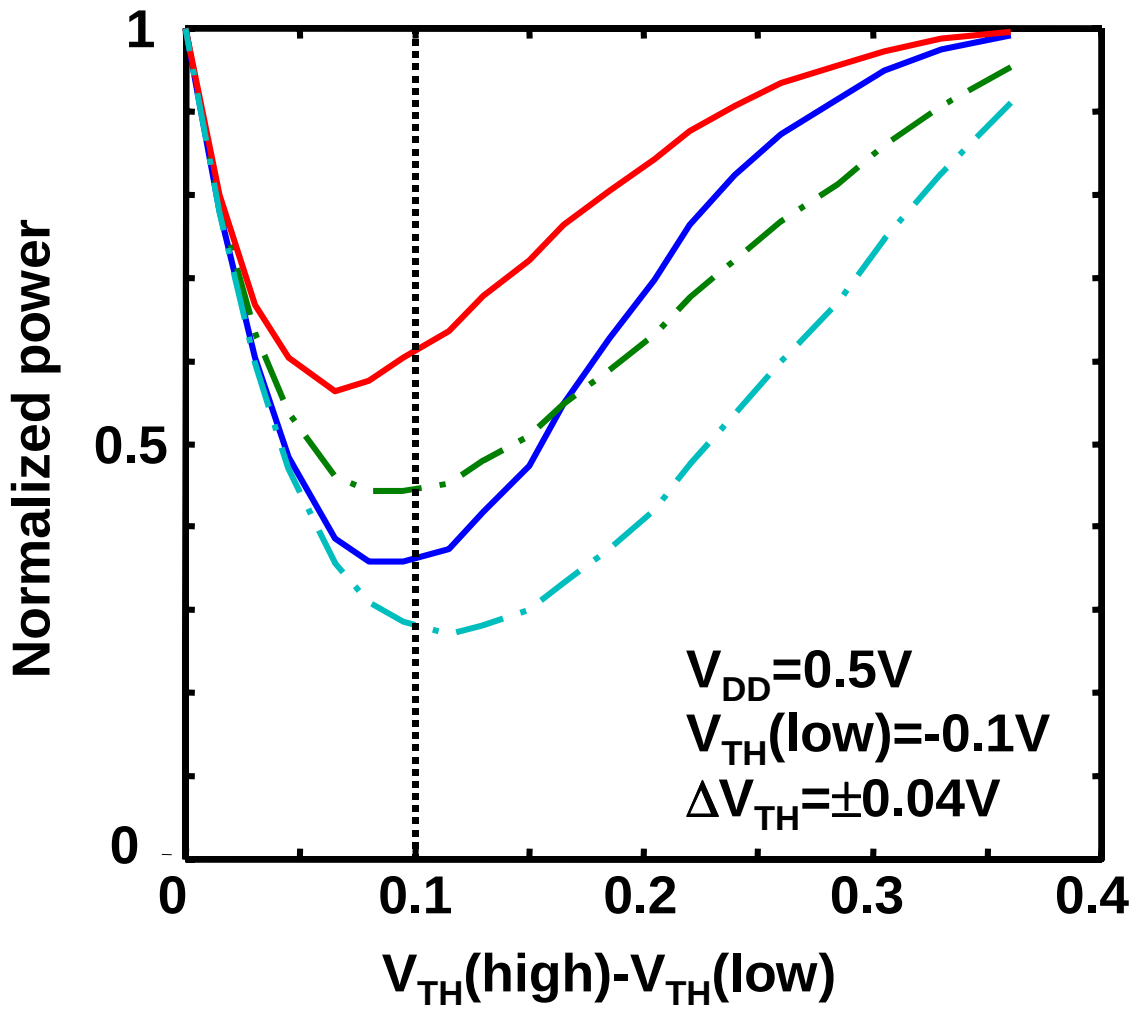
Controlling V_{DD} and V_{TH} for low power

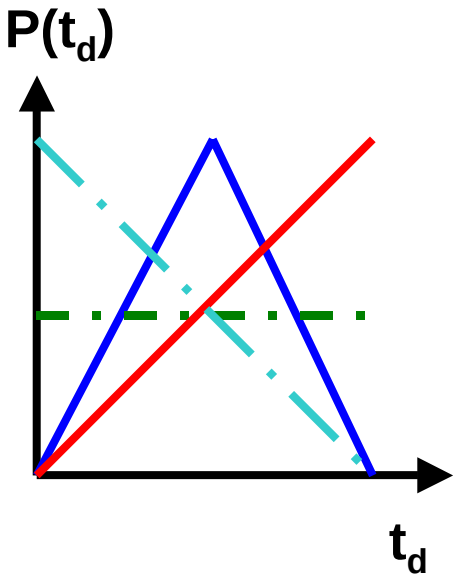
	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Dual-V_{TH} concept

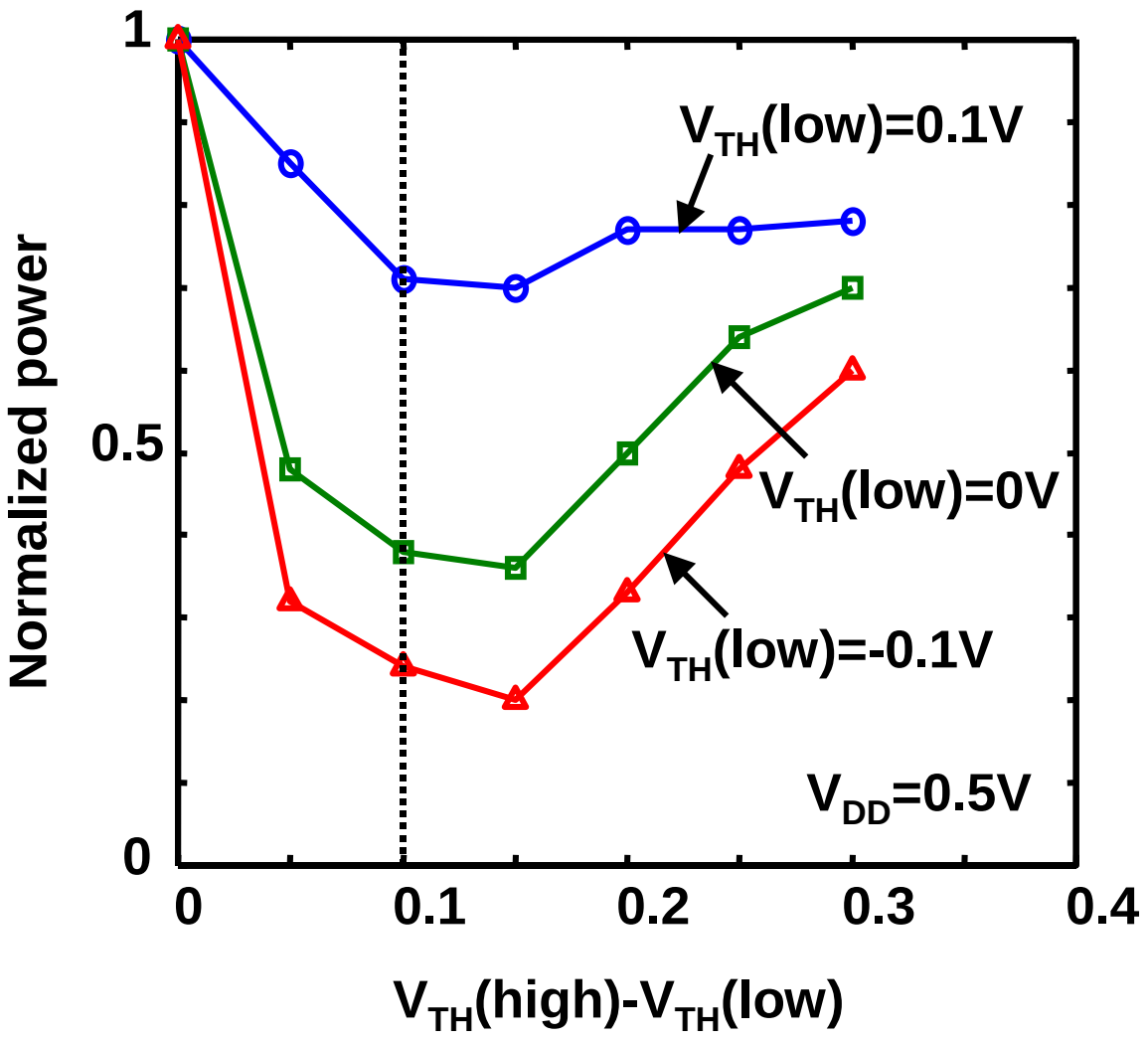


Calculated result of power reduction (Theoretical, V_{DD}=0.5V)





Synopsis simulation result
Simple processor example



Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
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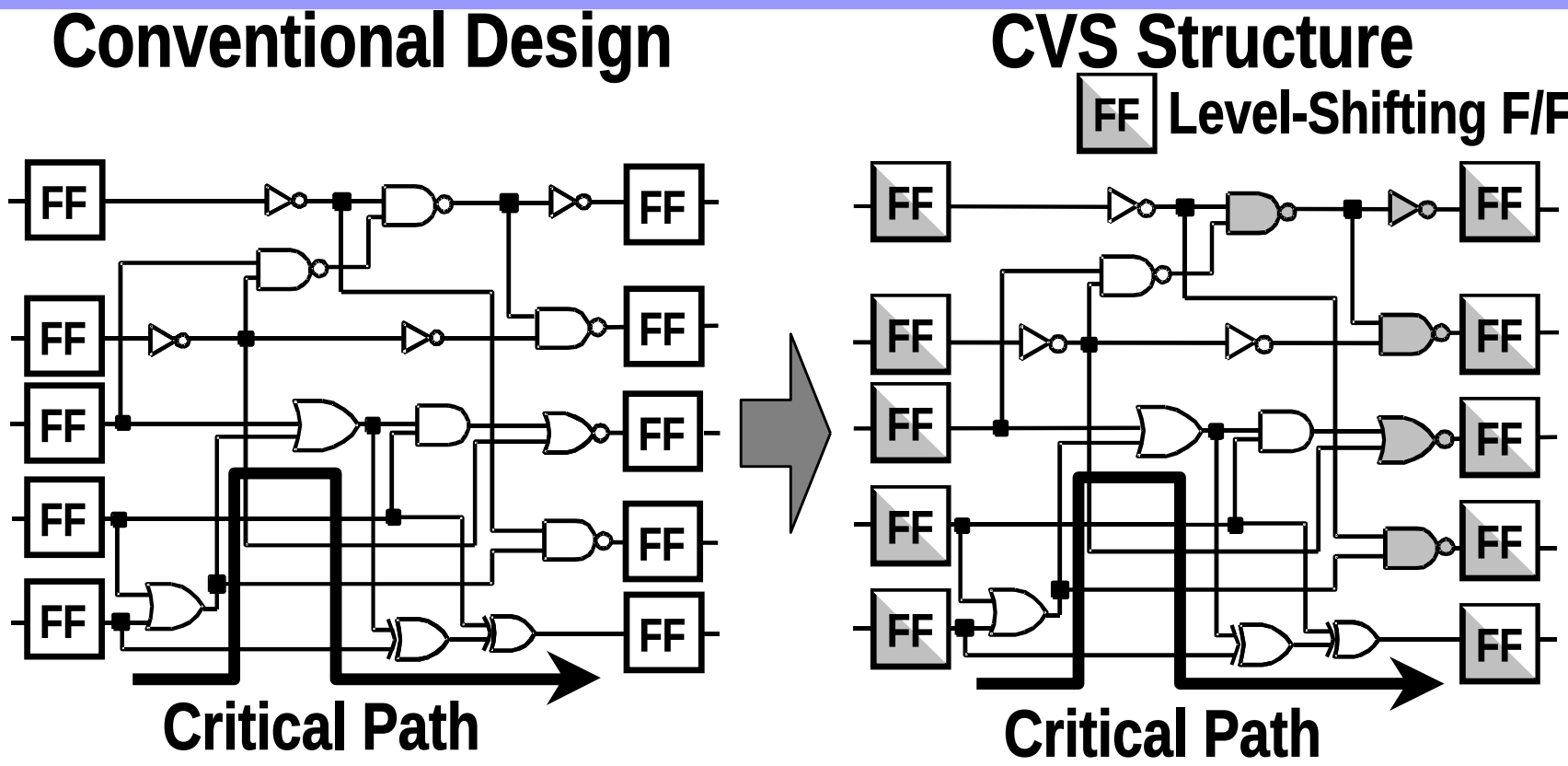
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Clustered Voltage Scaling for Multiple V_{DD}'s

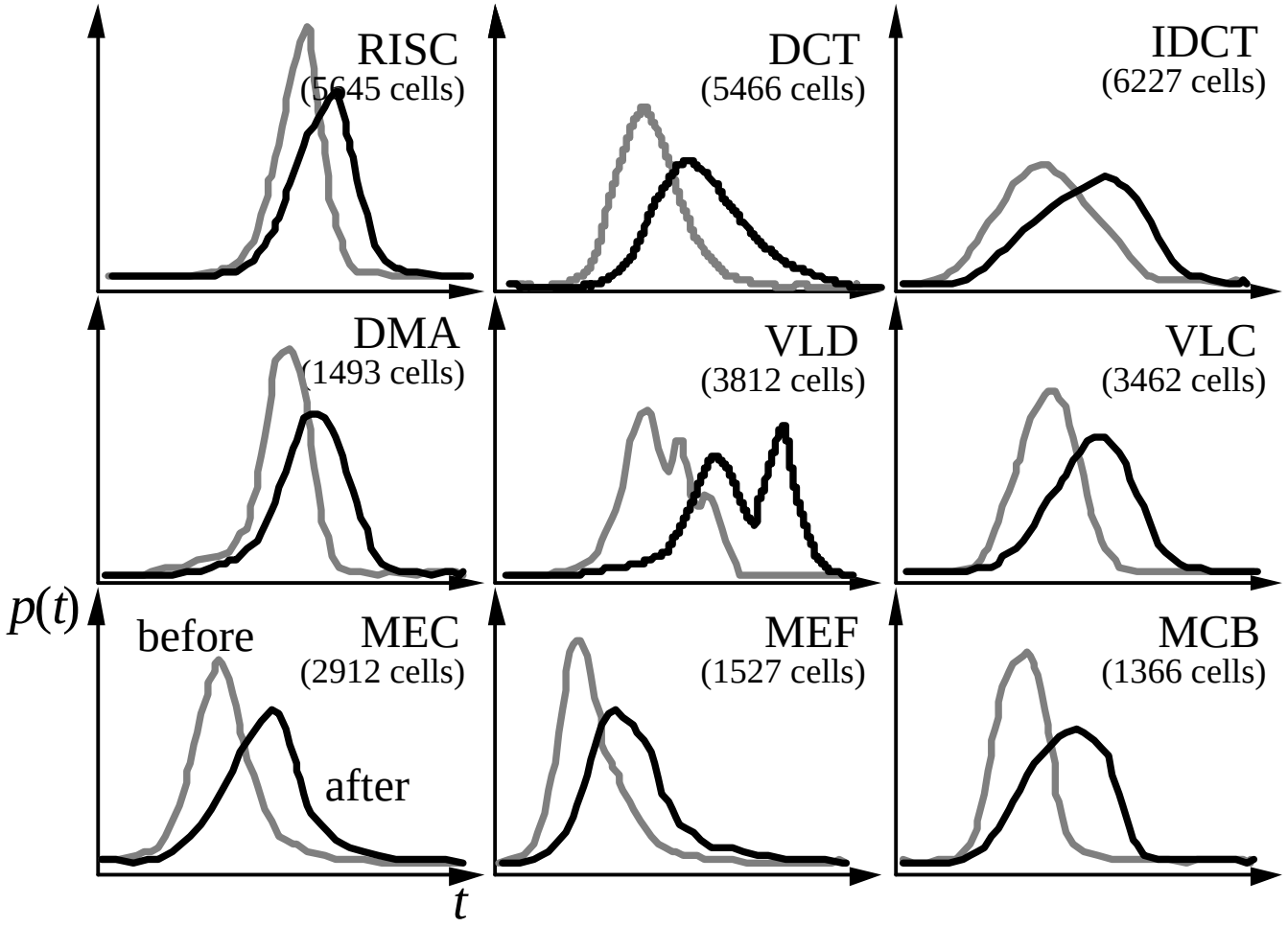


Lower V_{DD} portion is shown as shaded

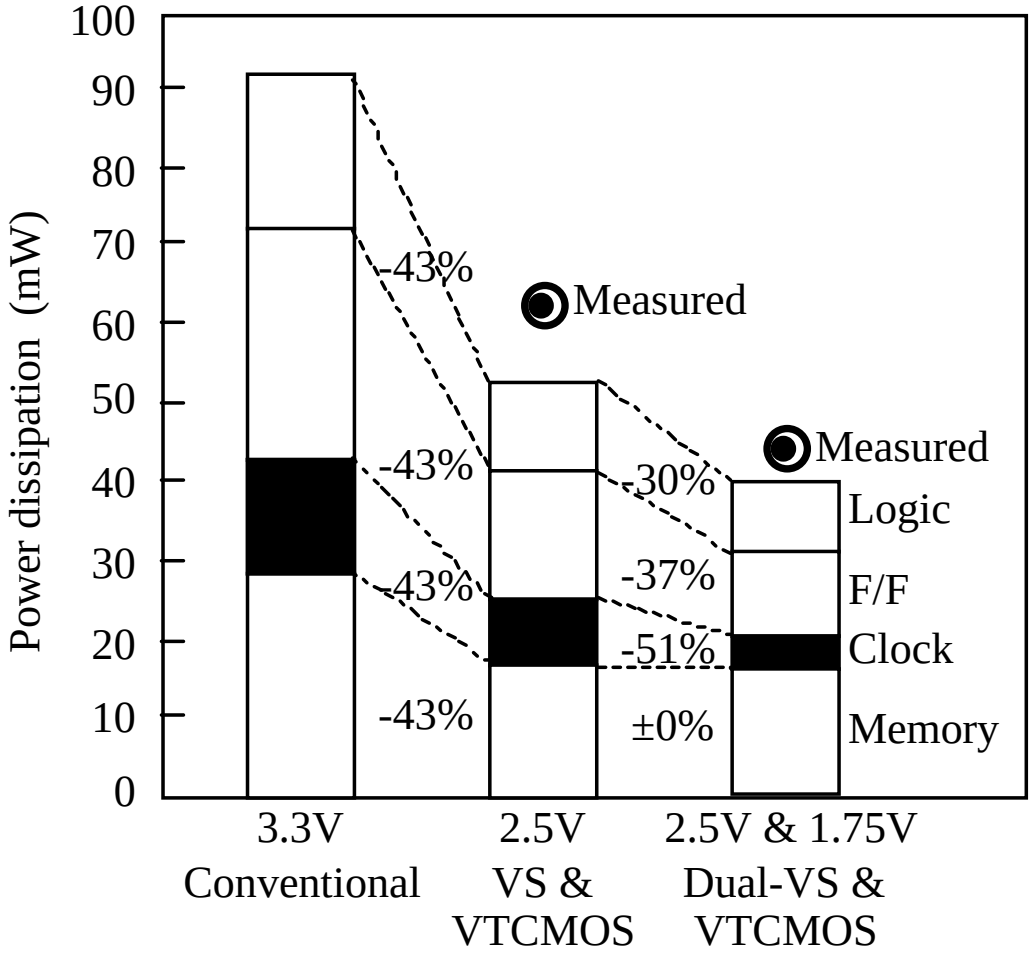
Once V_L is applied to a logic gate, V_L is applied to subsequent logic gates until F/F's to eliminate DC current paths. F/F's restore V_H.

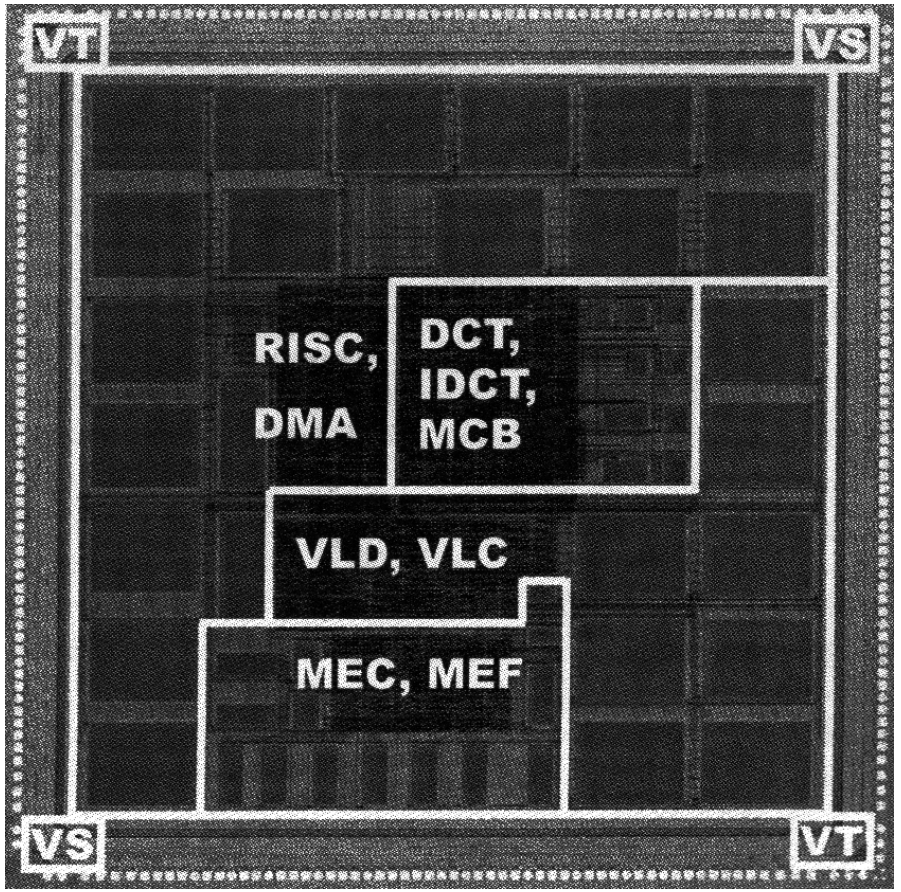
M.Takahashi et al., "A 60mW MPEG4 Video Codec Using Clustered Voltage Scaling with Variable Supply-Voltage Scheme," ISSCC, pp.36-37, Feb.1998.

Path-delay Distribution in Dual-VS



Clustered Voltage Scaling Technique





M.Takahashi et al., "A 60mW MPEG4 Video Codec Using Clustered Voltage Scaling with Variable Supply-Voltage Scheme," ISSCC, pp.36-37, Feb.1998.

Controlling V_{DD} and V_{TH} for low power

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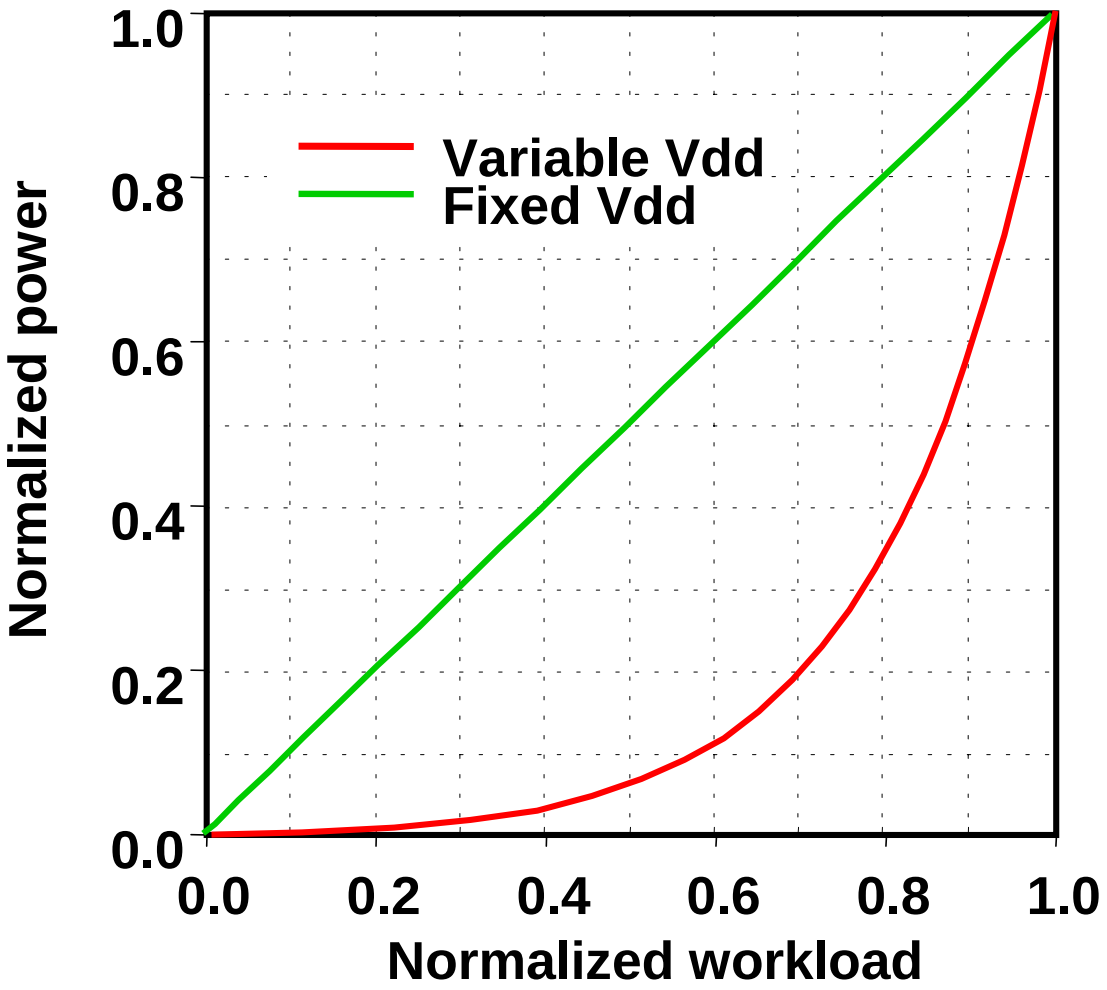
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

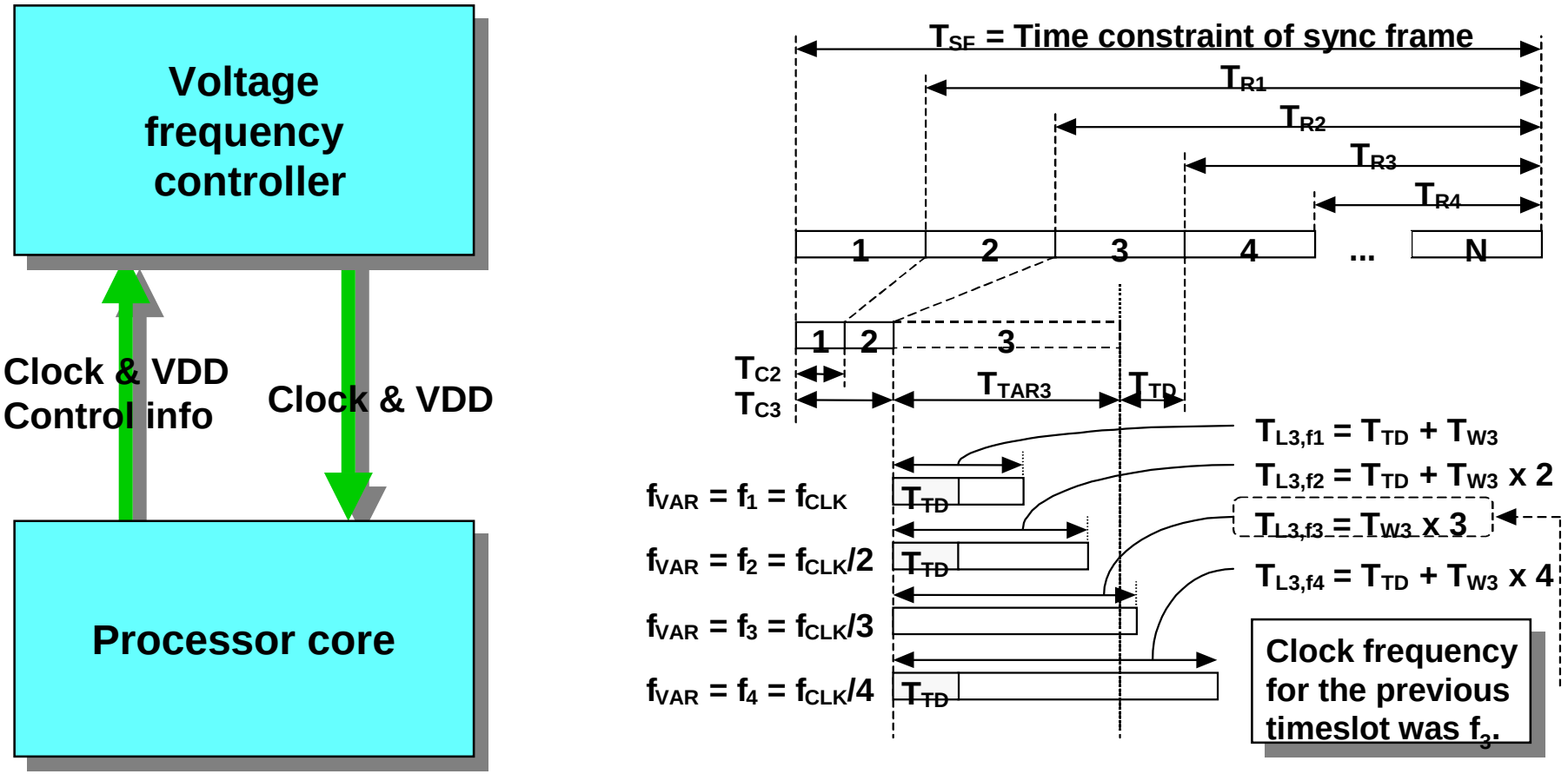
If you don't need to hussle, V_{DD} should be as low as possible

Energy consumption is proportional to the square of V_{DD}.

V_{DD} should be lowered to the minimum level which ensures the real-time operation.



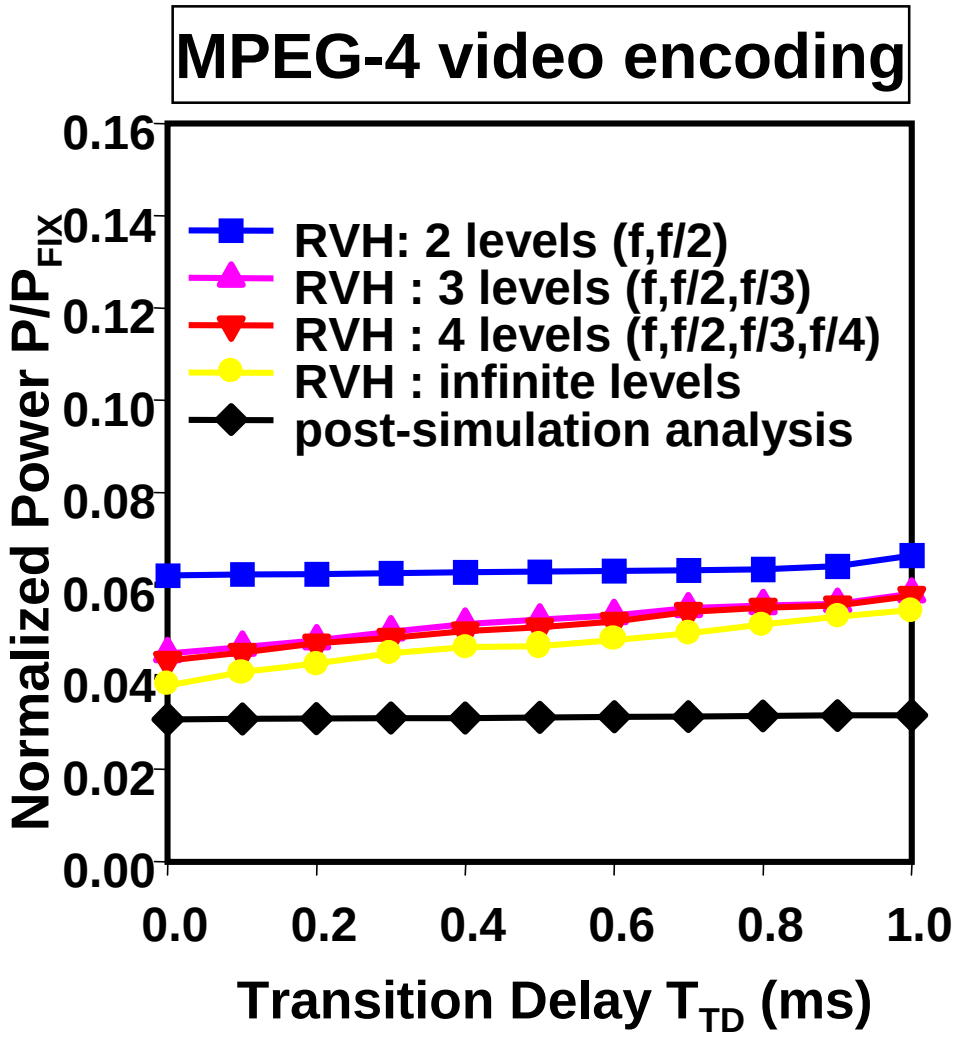
Application slicing and software feedback loop in Voltage Hopping

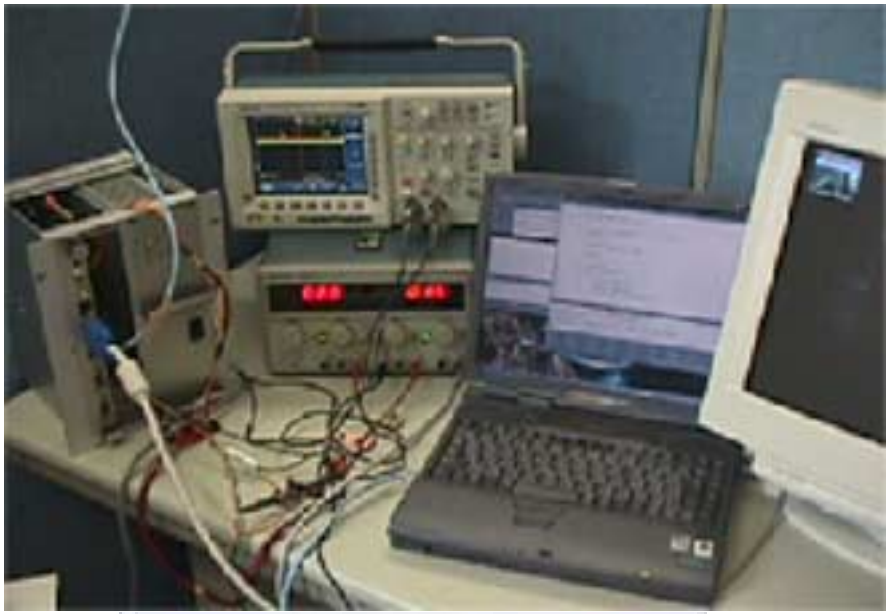


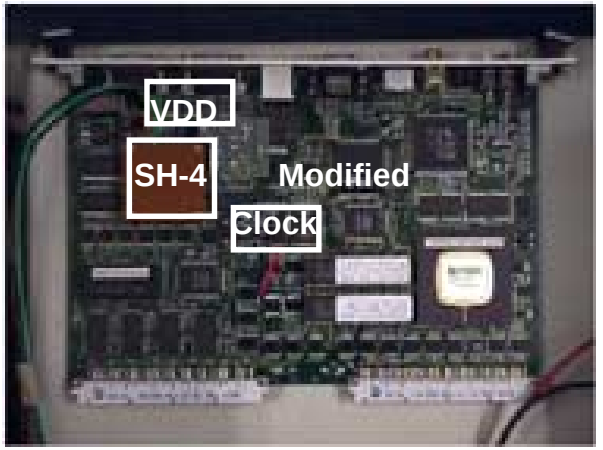
S.Lee and T.Sakurai, “Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications,”ASPDAC'00, A5.2, pp.381~pp.386, Jan. 2000.

S.Lee and T.Sakurai, “Run-time Voltage Hopping for Low-power Real-time Systems,” DAC'00, June 2000.

Run-time Voltage Hopping reduces power to less than 1/10







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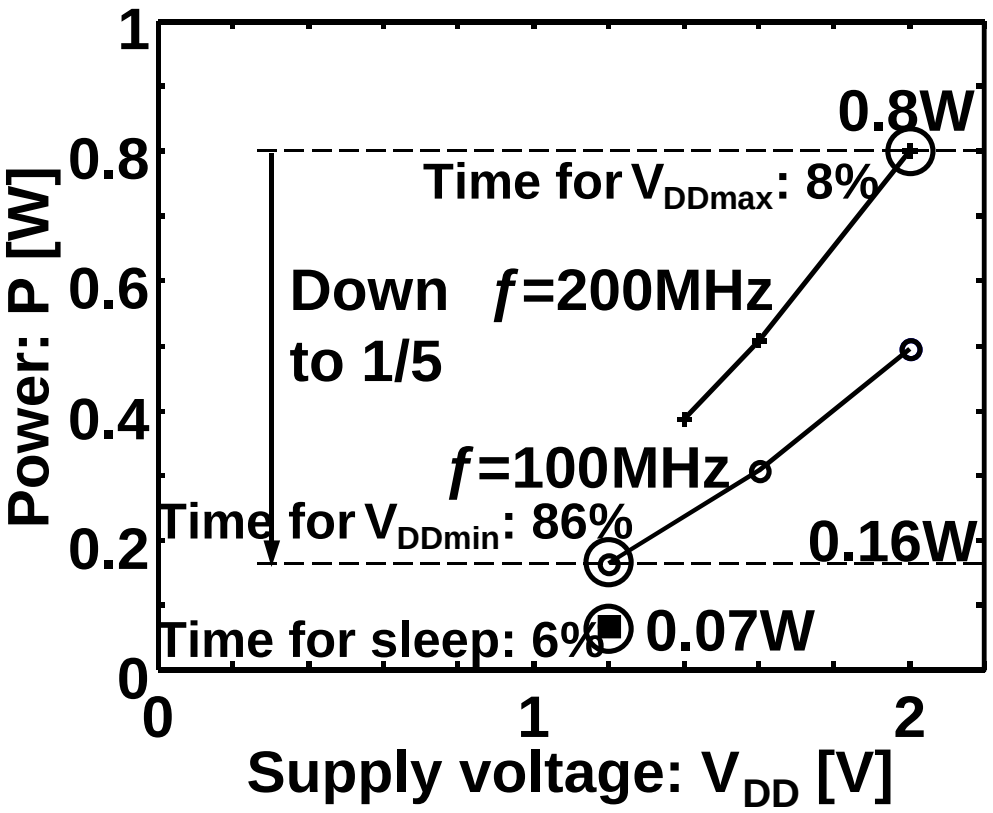
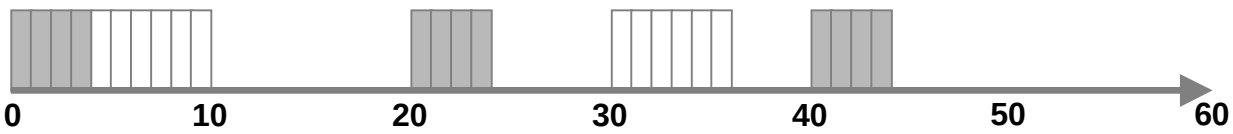
Measured power characteristics

Total power = 0.8 x 0.08 + 0.16 x 0.86 + 0.07 x 0.06 = 0.2W

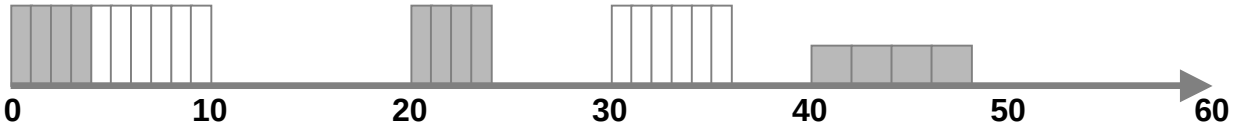


VDD hopping can cut down power consumption to 1/4

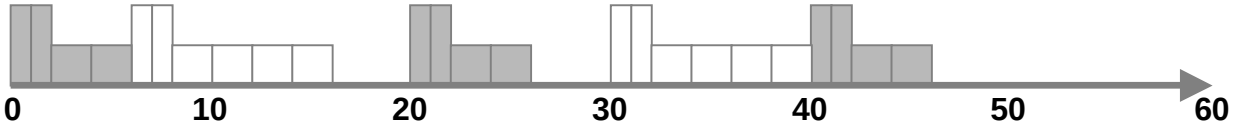
Power Conscious OS & Application Slicing



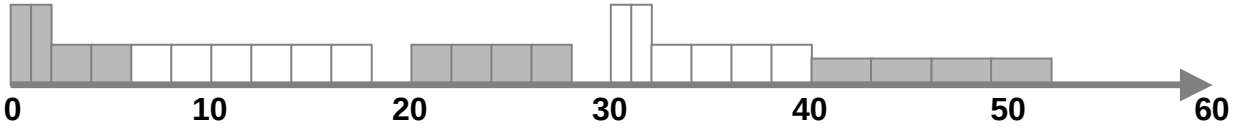
Conventional rate-monotonic scheduling (power consumption=1)



Speed control with power-conscious OS (power consumption=0.85)



Speed control within application slices (power consumption=0.47)

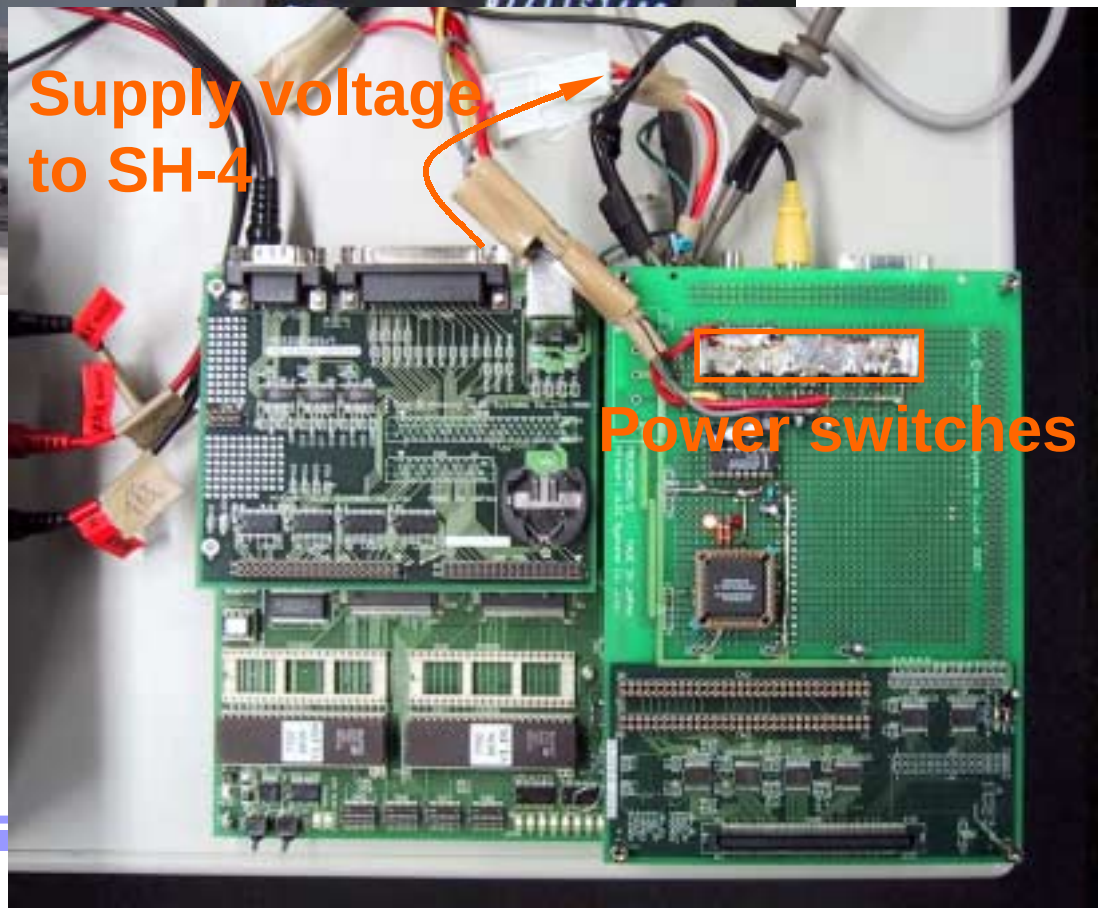


Proposed scheduling: cooperation of OS and applications (power consumption=0.24)

Y.S.Shin, H.Kawaguchi, T.Sakurai, "Cooperative Voltage Scaling (CVS) between OS and Applications for Low-Power Real-Time Systems," CICC'01, pp.553-556, May 2001.

Hardware

(A) System



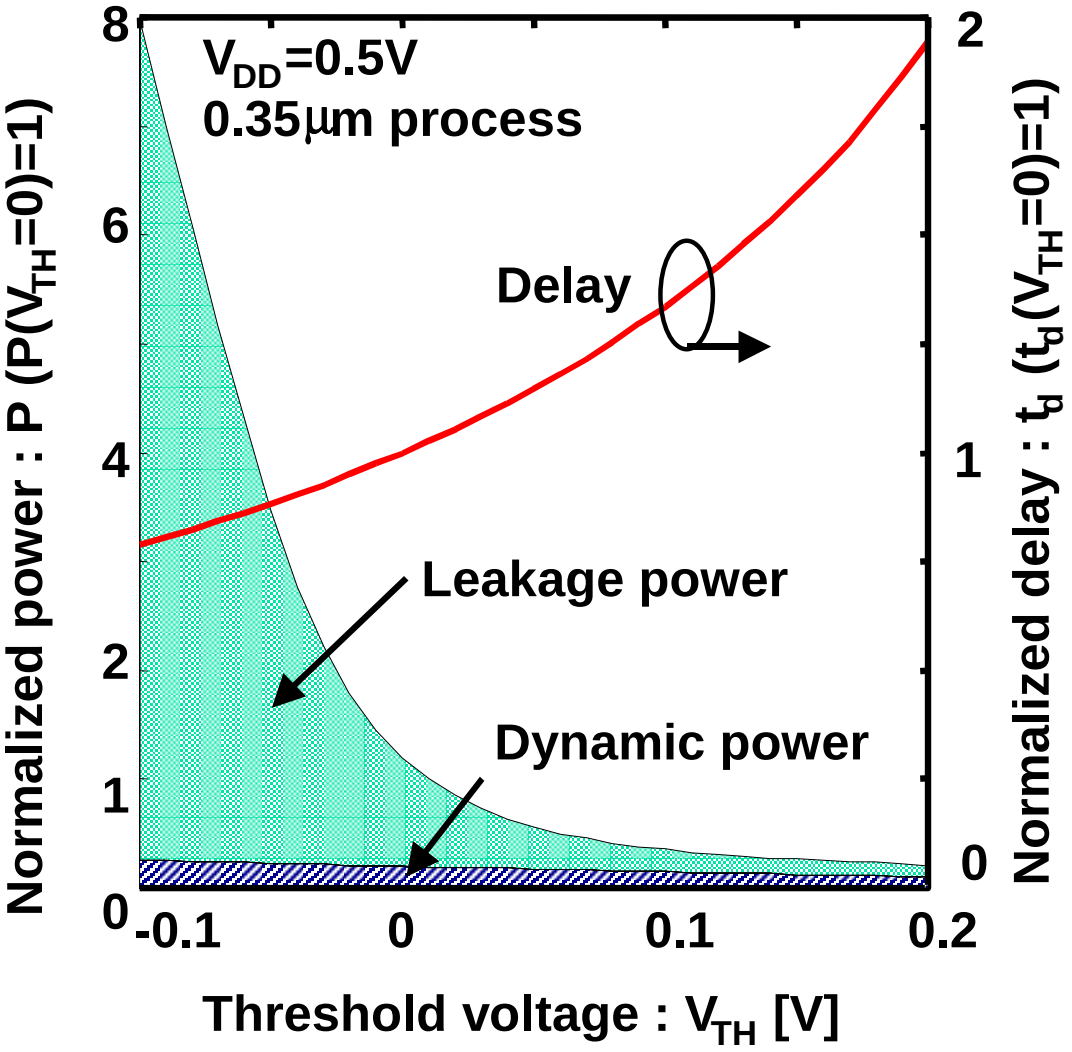
(B) SH-4 embedded board

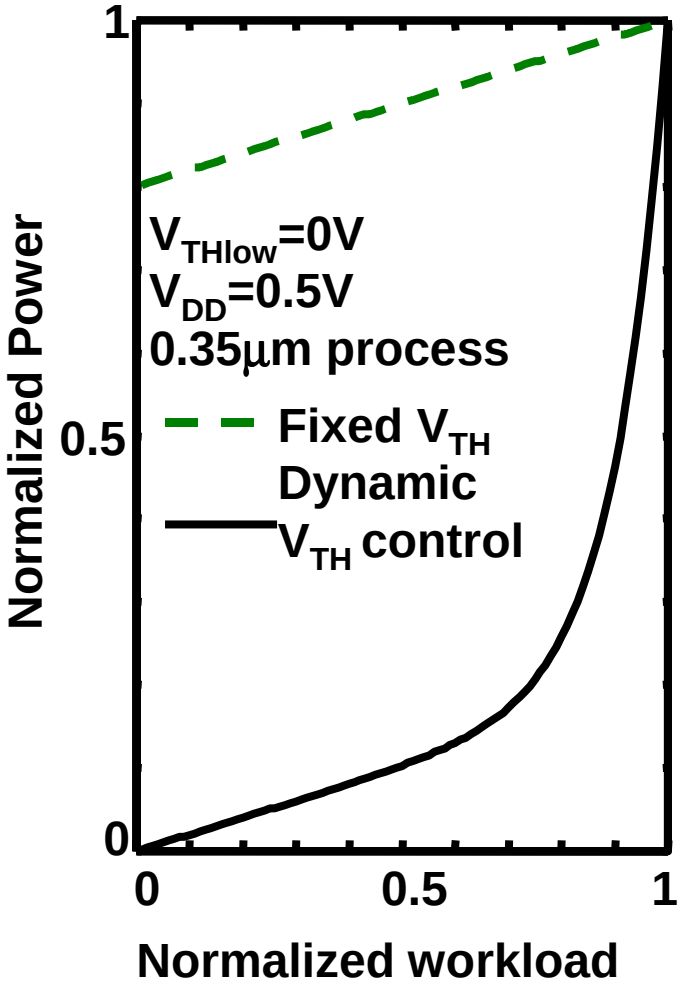
Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

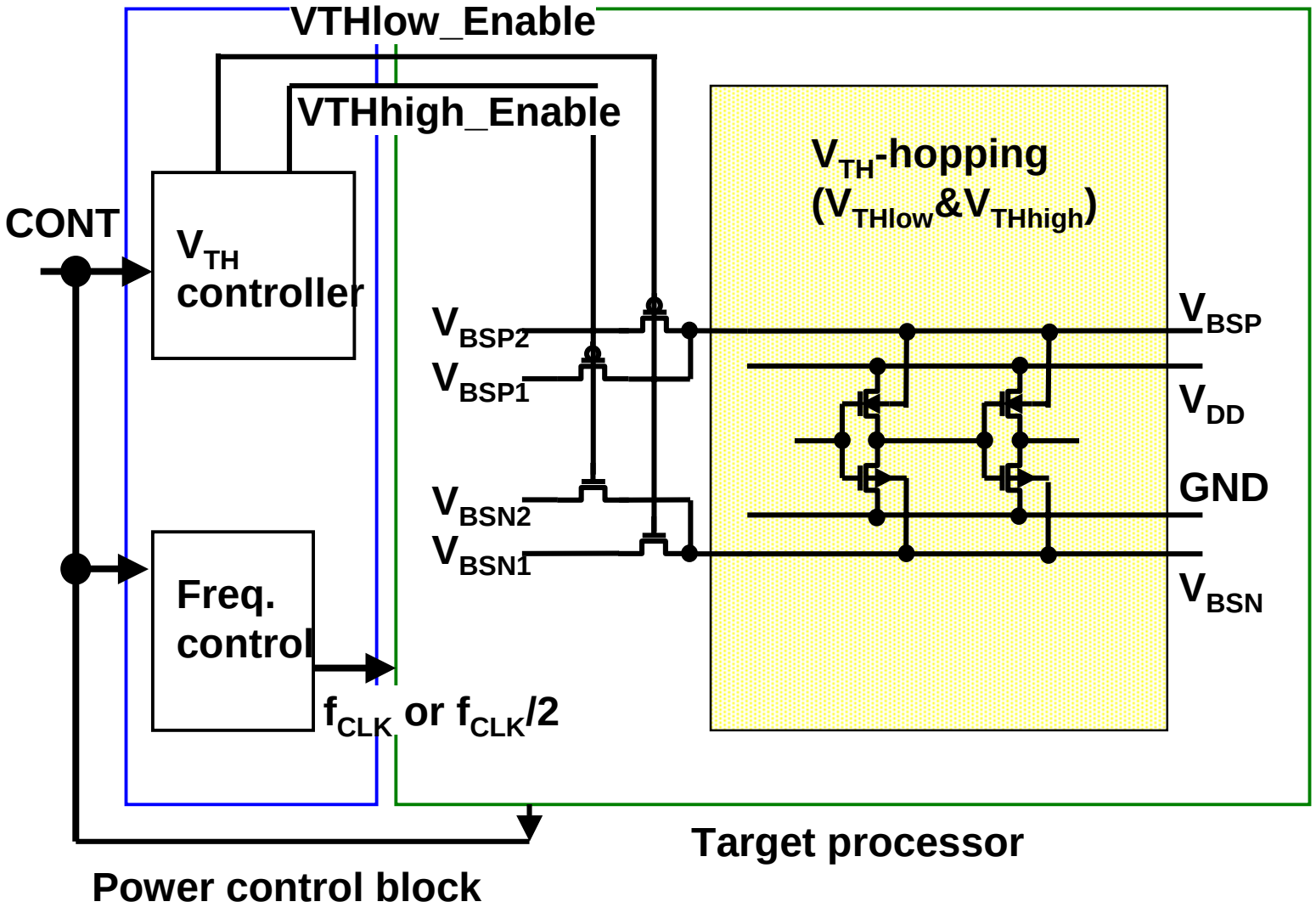
K. Nose, M.Hirabayashi, H.Kawaguchi, S.Lee and T.Sakurai, “VTH-hopping Scheme for 82% Power Saving in Low-voltage Processors,” to be published, CICC 2001.

V_{TH}-hopping

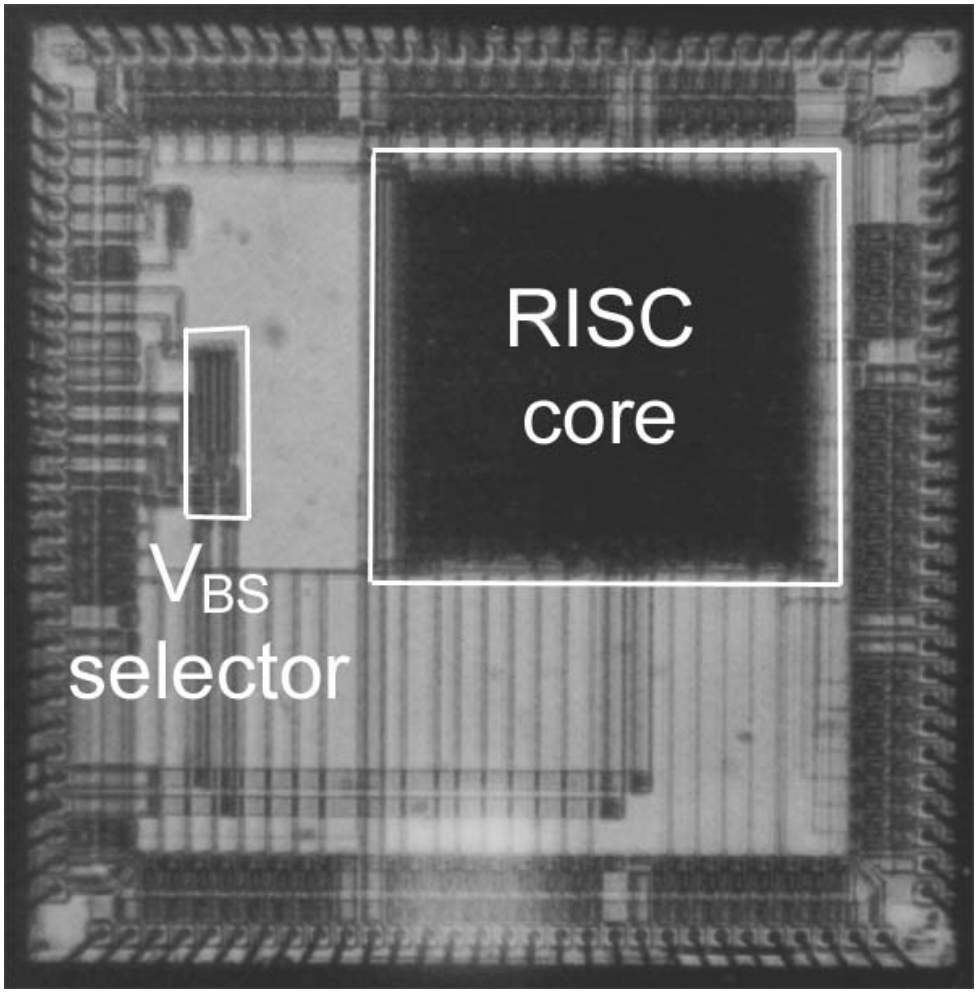

V_{DD}=0.5V
0.35μm process
Delay
Leakage power
Dynamic power
Normalized power : P (P(V_{TH}=0)=1)
Normalized delay : t_d (t_d(V_{TH}=0)=1)
Threshold voltage : V_{TH} [V]
8
6
4
2
1
0
2
1
0
-0.1
0
0.1
0.2


V_{THlow}=0V
V_{DD}=0.5V
0.35μm process
Fixed V_{TH}
Dynamic
V_{TH} control
Normalized Power
Normalized workload
1
0.5
0
0
0.5
1

Schematic of V_{TH}-hopping



Microphotograph of RISC processor

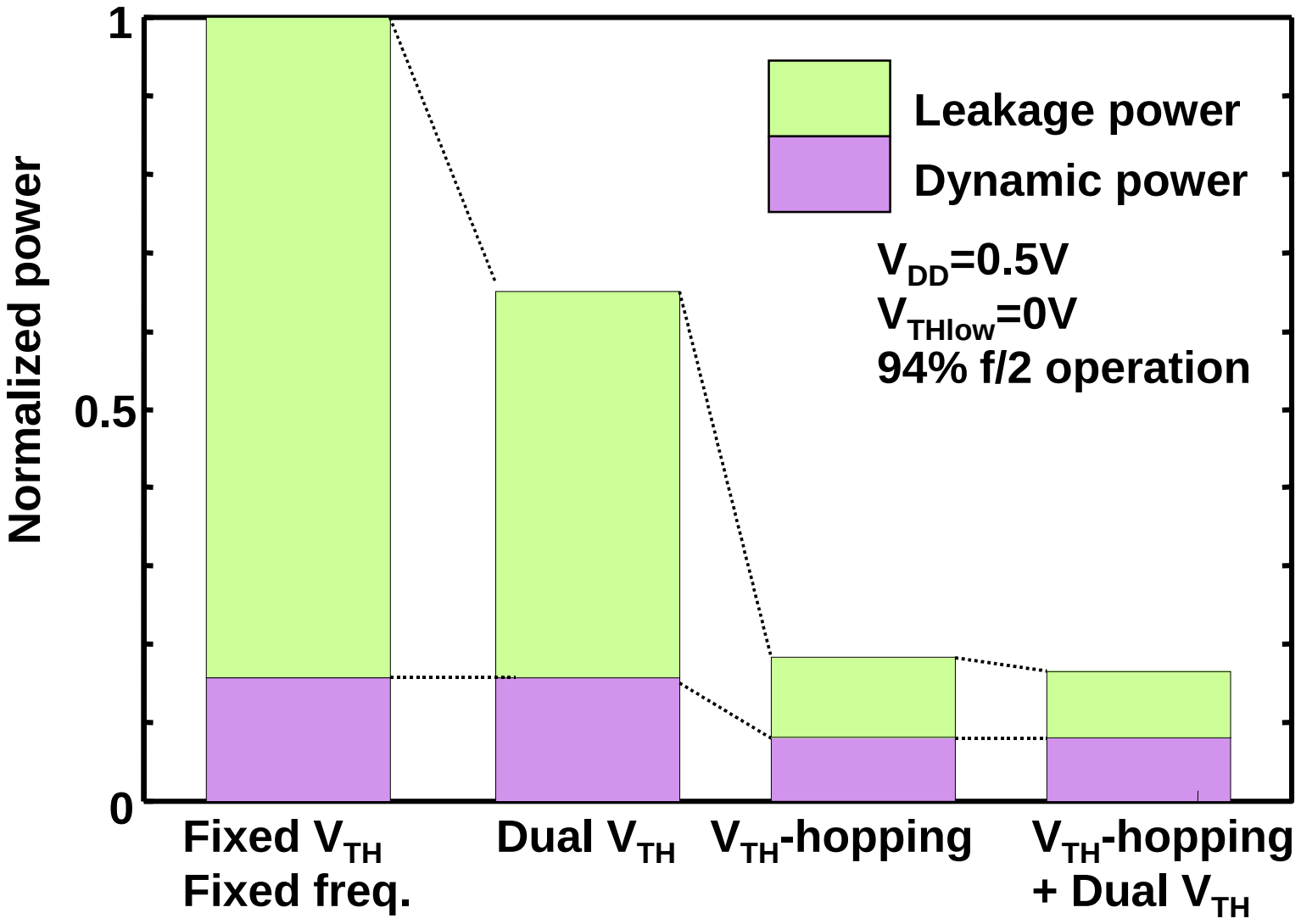


0.6μm process

Overhead of V_{TH}-hopping
= 14%

RISC core
= 2.1mm x 2.0mm
V_{BS} selector
= 0.2mm x 0.6mm

Power comparison



Principle for Power Reduction

$$P \approx \alpha \bullet C_L \bullet V_S \bullet V_{DD} \bullet f_{CLK} + I_0 \bullet 10^{-V_{TH}/S} + \text{gate leak} + \text{junc. leak}$$

- **Lowering switching probability (α)**
  - Low transition coding
  - Gated clock , Conditional F/F
  - Power estimation / optimization CAD
- **Lowering load capacitance (C_L)**
  - Embedded memory
  - Low capacitance circuit
  - Low-power cell library (gate sizing)
- **Lowering supply voltage ($V_S \bullet V_{DD}=V_{DD}^2$)**
  - Variable-V_{DD}, Variable-V_{TH}, Multi-V_{DD}, Multi-V_{TH} , DC/DC
  - Low voltage memory
  - Low swing clock / bus
- **Lowering operating frequency**
  - Better algorithm

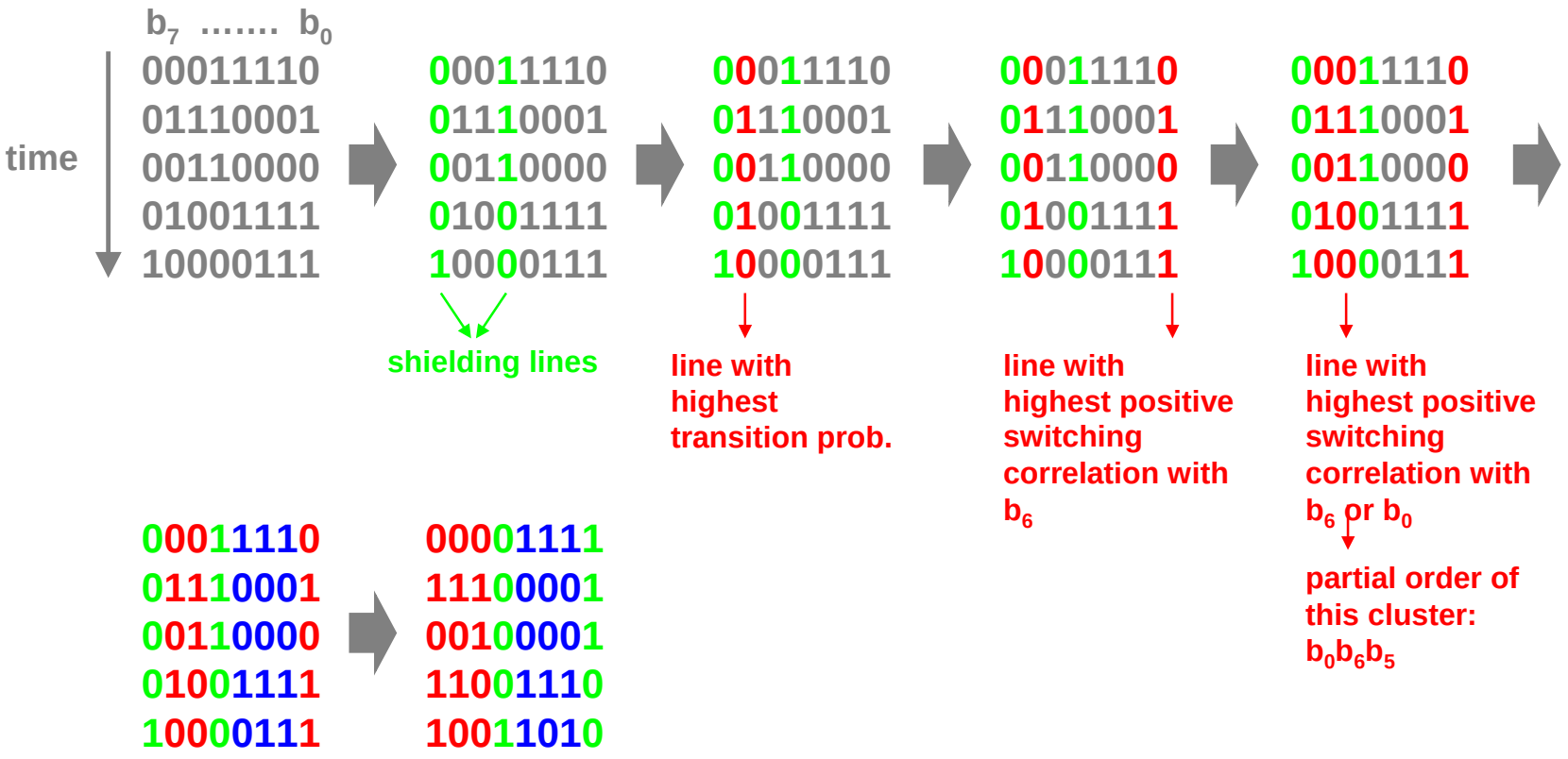
Bus Shuffling

- Bus shuffling
  - Virtually no overhead
  - Pattern information is necessary: applicable to special-purpose systems
  - Layout modification or compiler backend support
- Problem definition
  - Given a set of patterns or statistics of patterns
  - Find order of bus lines so that power consumption due to area and coupling capacitances is minimized

Y. Shin and T. Sakurai, “Coupling-driven bus design for low-power application-specific systems,” Proc. Design Automation Conf. (DAC), pp.750-753, June 2001.

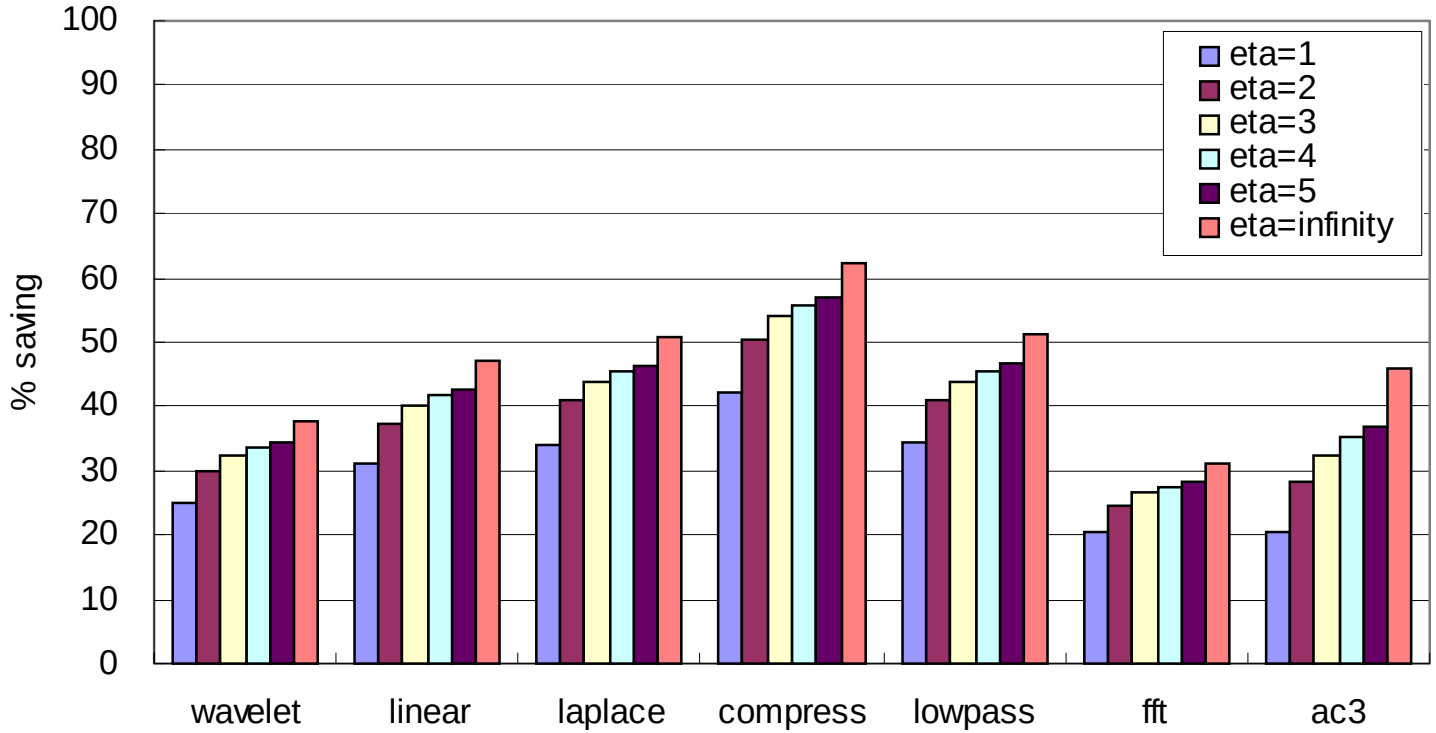
Bus Shuffling

- **Example**



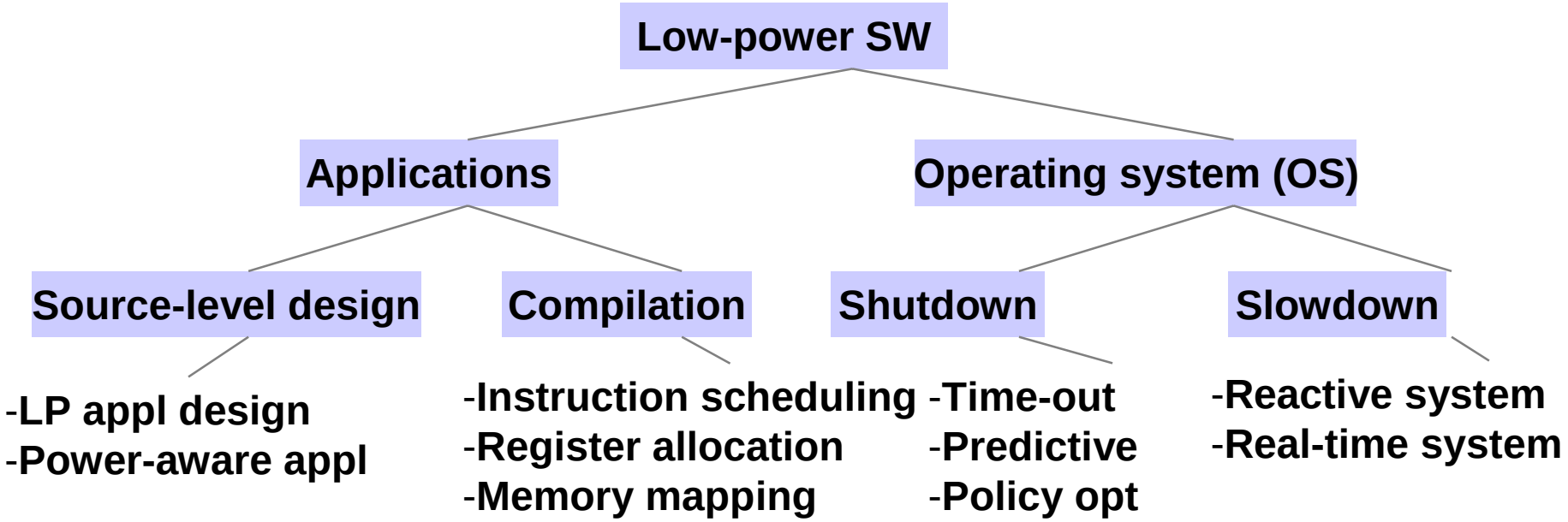
Experiments

- **Result of heuristic**
  - **7 data address sets**
  - **% power saving compared to un-shuffled buses**



$$\eta = \frac{\text{coupling cap.}}{\text{area cap.}}$$

Software Level Low-Power Work

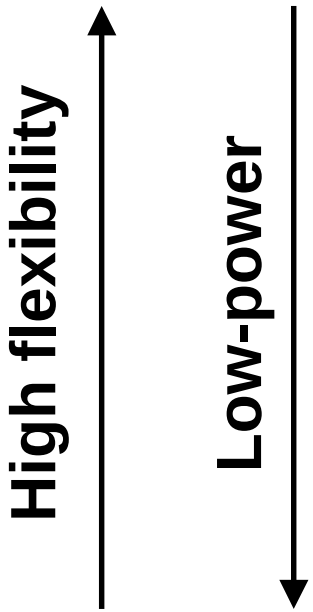


Techniques with architectural changes

- Cache design
- Memory hierarchy design
- Code compression
- Application-specific processor design
- Encoding

Less wasteful design wins low-power race

Example of MPEG2 decoding



- Processor (software)
  ～25W
- DSP
  ～4W
- Dedicated sytem LSI (SW/HW)
  ～0.7W

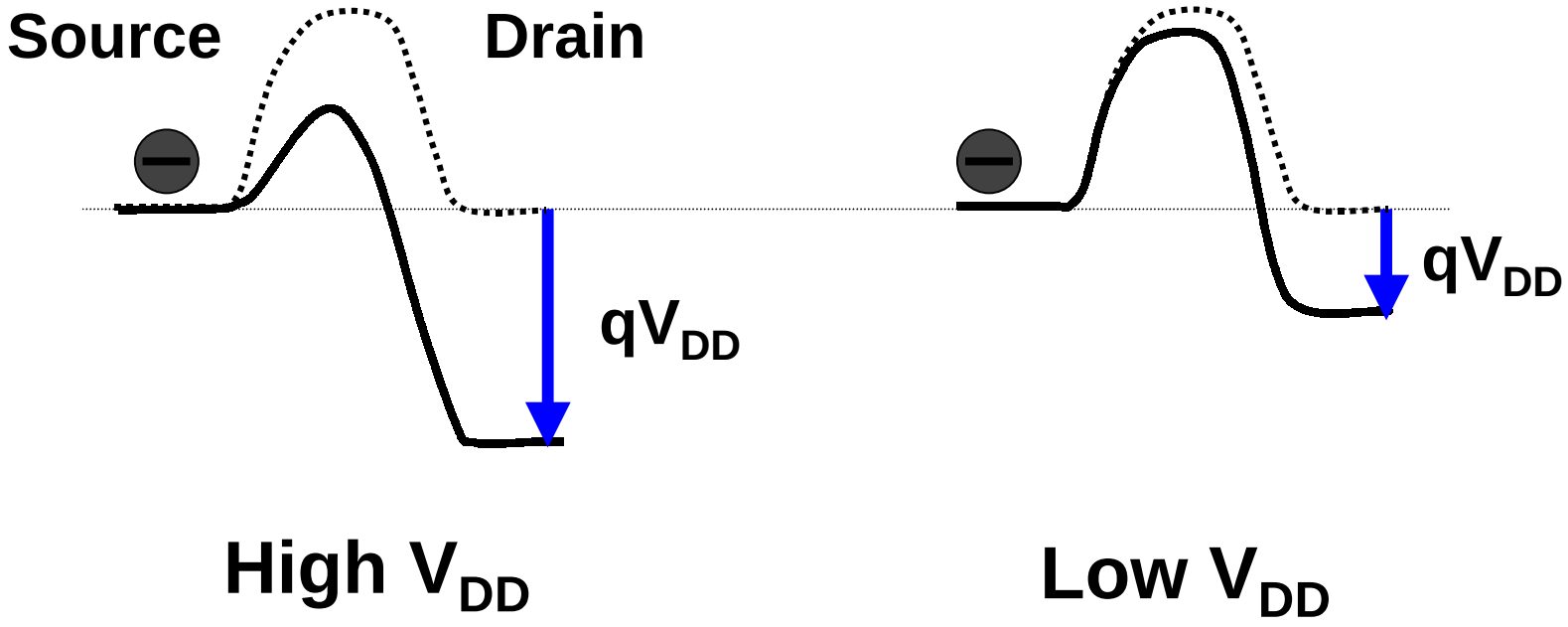
Summary – low-power

- For reducing standby power, insert a power switch in series to logic circuit (BGMOS).
  → Choice of power switch gate width

- For reducing active power, dual-VTH scheme and software control of VDD and VTH are promising.
  → Tools to support system-level low-power design with S/H co-design capability

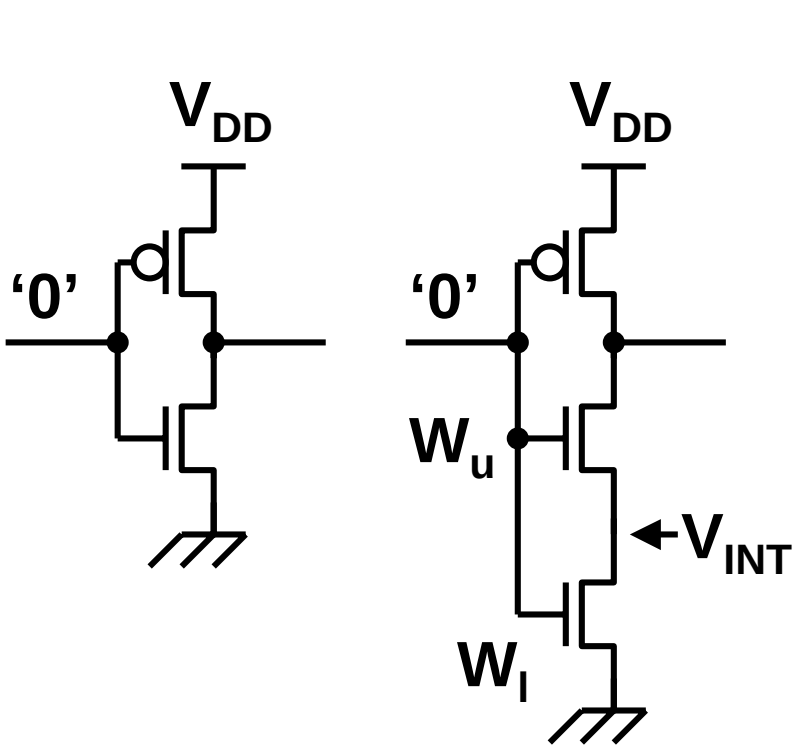
- Future giga-scale integration will use multiple VDD, VTH and Tox.
  → Tools to support new tech.

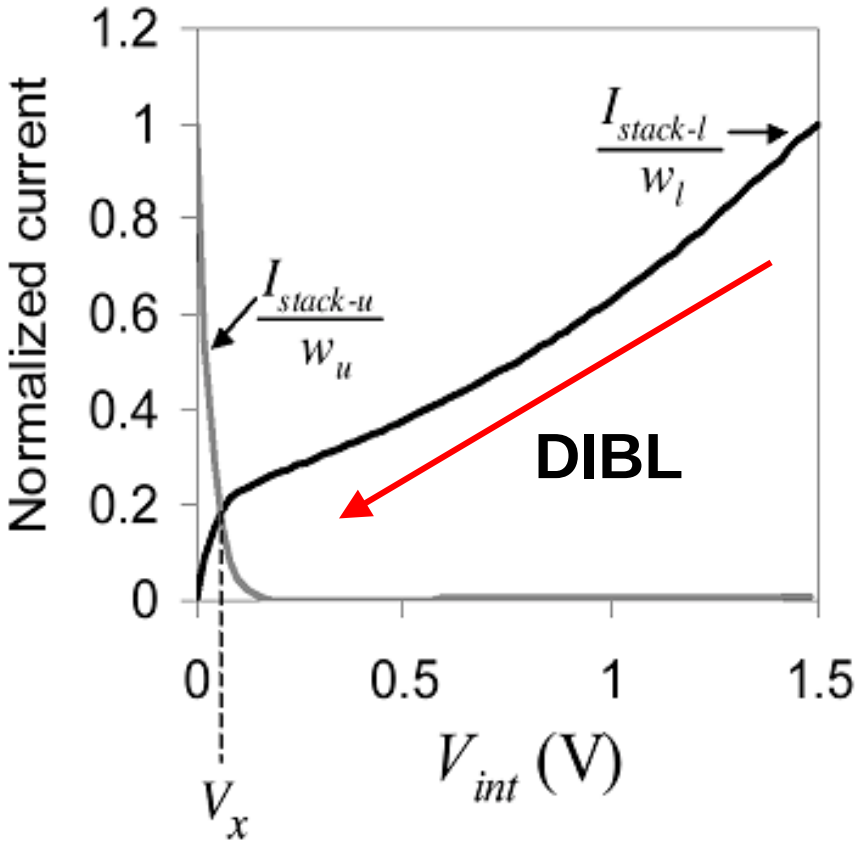
Drain induced barrier lowering (DIBL)



- Drain-Source間電圧が下がるとバンドギャップが増加し，リーク電流が減少する

Stack effect





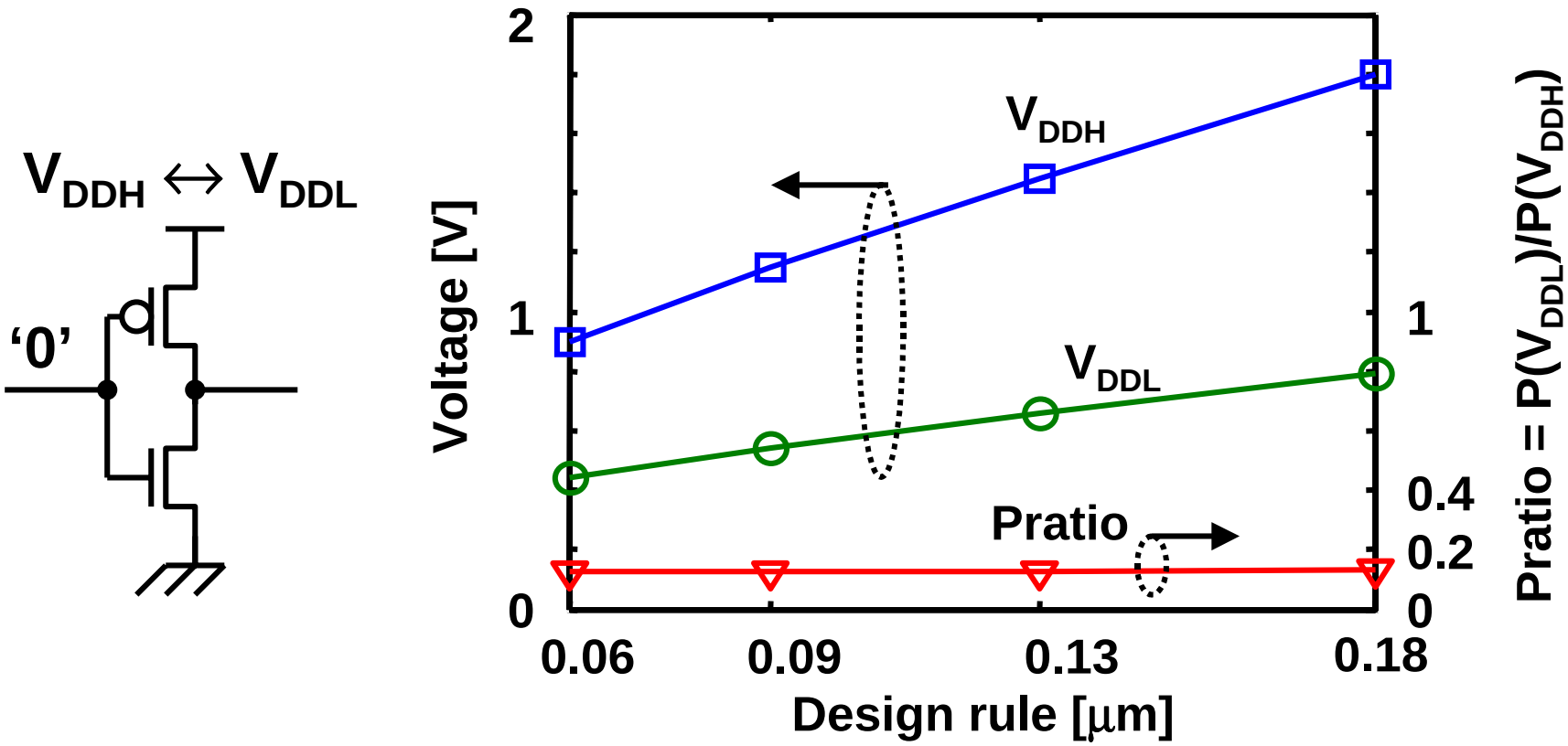
- Stack effect の最大の利点 = V_{INT} << V_{DD} & W_uが負にbias
  - W_L … DIBLは非常によく効く (V_{DS} が V_{DD}→V_{INT}になるため)
  - W_U … V_{INT}=0.1VでもI$_{LEAK}$は1桁減少 (V_{GS}=-0.1Vに等しい)

Scaling of DIBL factor

generation [μm]	0.18	0.13	0.09	0.06
V_{DD}	1.8	1.5	1.2	0.9
stack effect factor	8	9.5	10.5	11.5
DIBL factor : λ	0.042	0.057	0.076	0.103

S=80mV/decade

Analysis of DIBL effect

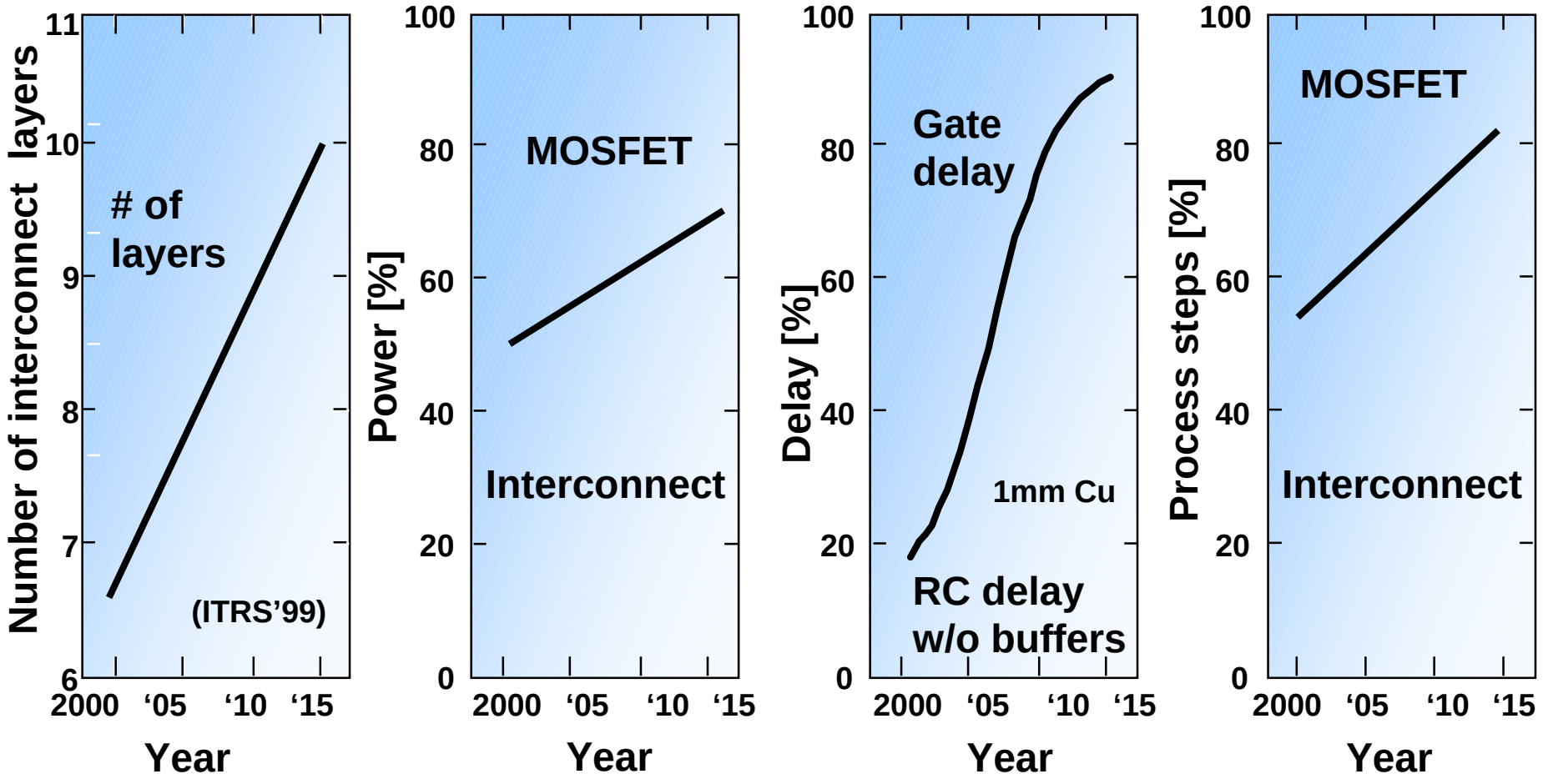


- DIBLは閾値を変えるだけと仮定する (ON時もDIBLを受ける)
- V_{TH}=0.15V_{DDH}, その他のパラメータは前のスライドと同じ
- 効果が世代にほとんどよらず約12%に減少

Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

Interconnect determines cost & perf.



T.Sakurai

DSM interconnect design issues become major design closure obstacles

Larger current

- IR drop (static and dynamic)
- Reliability (electro-migration)

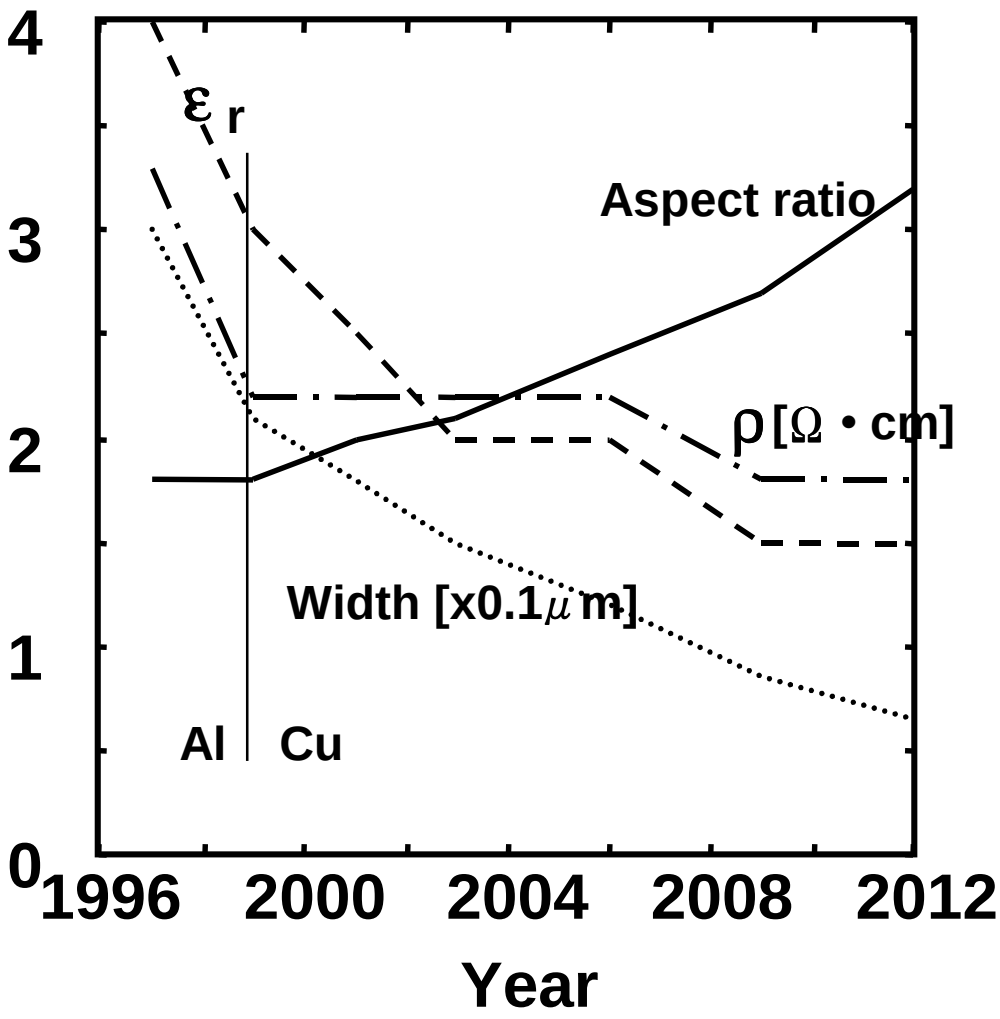
Smaller geometry / Denser pattern

- RC delay
- Crosstalk noise
- Delay fluctuation
- Signal Integrity

Higher speed

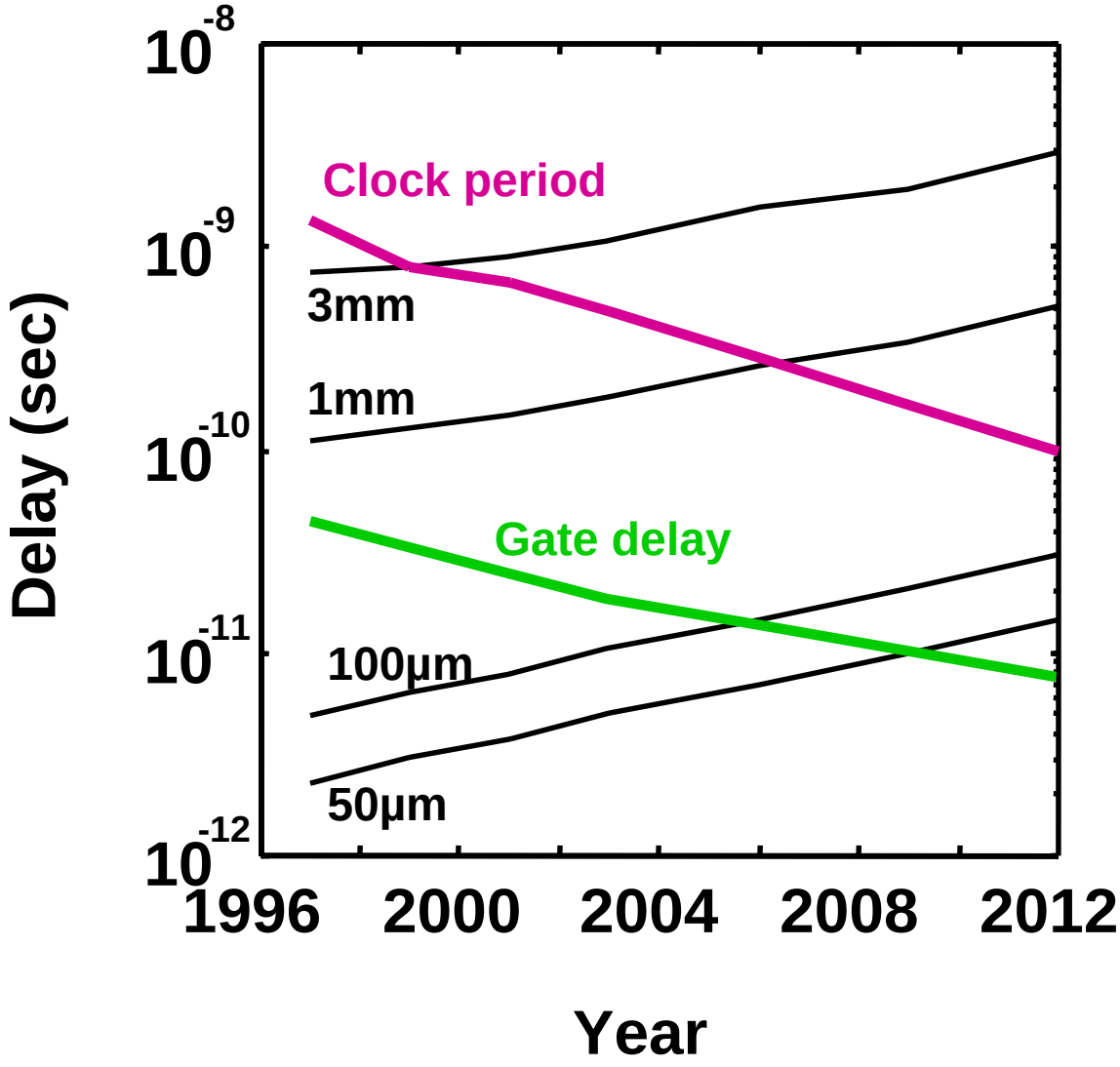
- Inductance
- EMI

Interconnect parameters trend

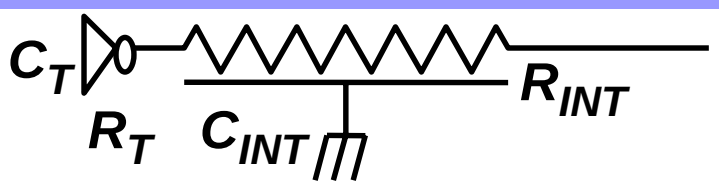


Semiconductor Industry Association roadmap
http://notes.sematech.org/1997pub.htm

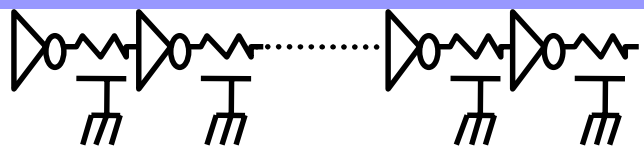
RC delay and gate delay



Buffer insertion



a) Without buffers



b) With buffers

$$t_{05} \approx 0.377 R_{INT} C_{INT} + 0.693(R_T C_T + R_T C_{INT} + R_{INT} C_T)$$

C_0 :*Gate capacitance of minimum MOSFET*

R_0 :*Gate effective resistance of minimum MOSFET*

$$Delay \approx k\left[p_1 \frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h} hC_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k} hC_0 \right)\right]$$: *Buffered*

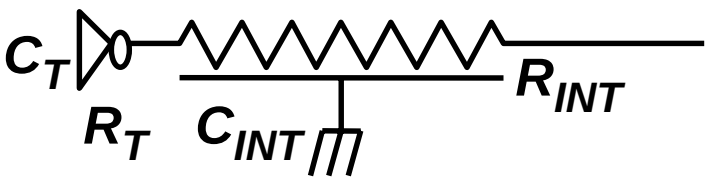
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT} R_0}{R_{INT} C_0}}$$:*Optimized size of buffer inverter*

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}}\sqrt{\frac{R_{INT} C_{INT}}{R_0 C_0}}$$:*Optimized number of stages*

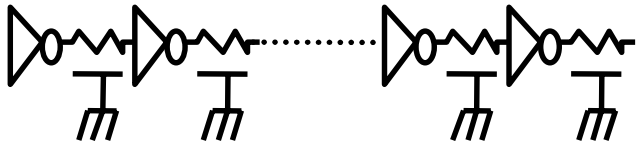
$$Delay_{OPT} = 2\left(\sqrt{p_1 p_2} + p_2\right)\sqrt{R_{INT} C_{INT} R_0 C_0} \approx 2.4\sqrt{\tau_{INT}\tau_{MOS}}$$

$$Cap.\ of\ gates = k_{OPT} h_{OPT} C_0 = \sqrt{p_1 / p_2} C_{INT} = 0.73 C_{INT}$$

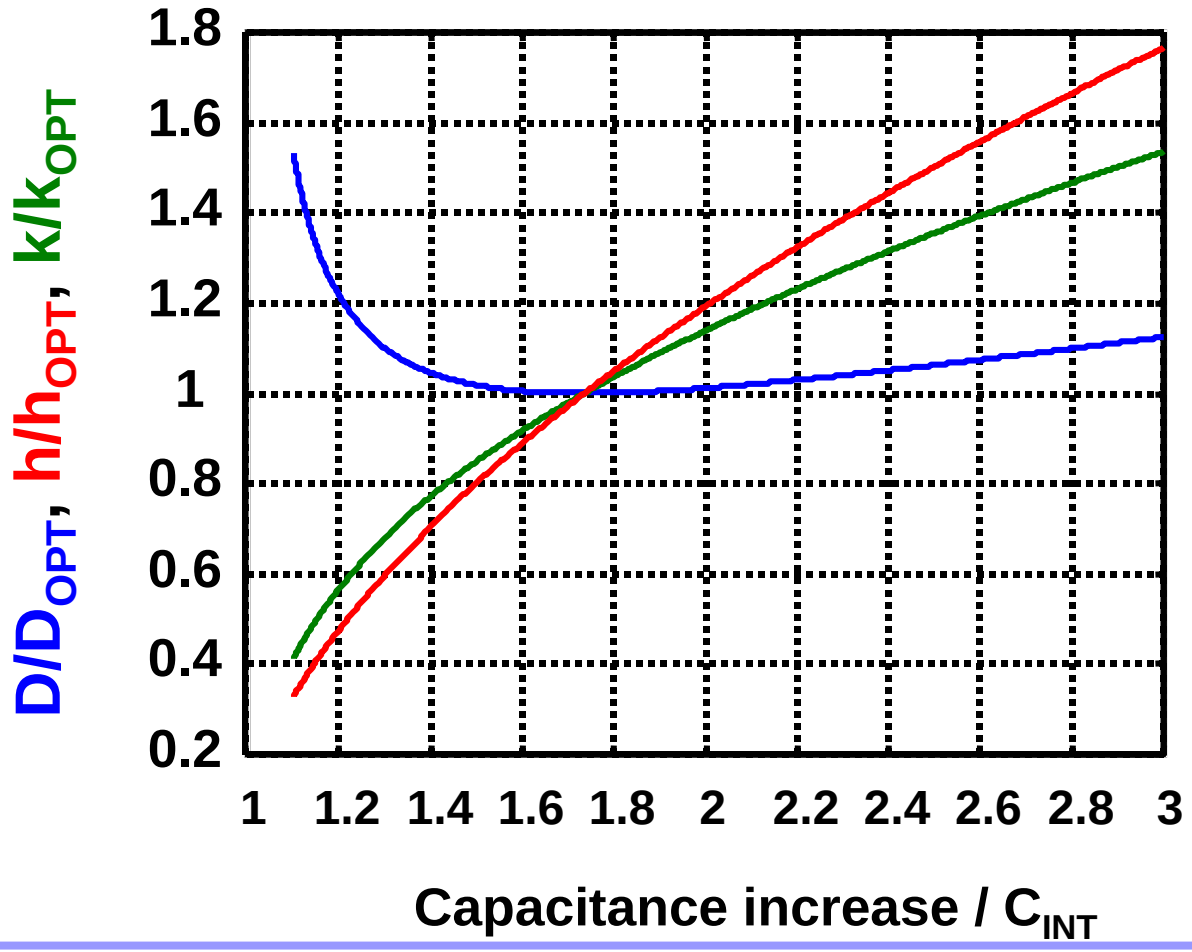
Power and delay optimization



a) Without repeaters



b) With repeaters



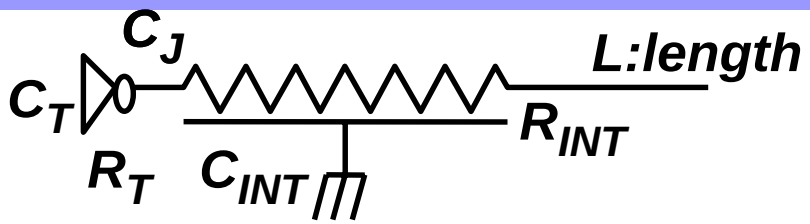
h: size of repeater

k: # of stages

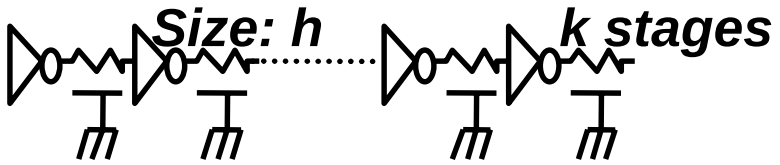
D: total delay

C_{INT}: interconnect capacitance

Buffer insertion with junction cap.



a) Without buffers



b) With buffers

$$\text{Delay}_{OPT} = 2L\left(\sqrt{p_1 p_2} + p_2\sqrt{\frac{C_0}{C_0 + C_{J0}}}\right)\sqrt{R_{INT0}C_{INT0}R_0(C_0 + C_{J0})}$$

$$= 2L\left(\sqrt{p_1 p_2} + p_2\sqrt{1/\eta_J}\right)\sqrt{\tau_{INT0}\tau_{MOS0}}\sqrt{\eta_J},\ \tau_{MOS0} = R_0 C_0$$

$$\approx 2.4L\sqrt{\tau_{INT0}\tau_{MOS0}}\ \text{(when } C_{J0} = 0\text{)}$$

$$\approx 2.8L\sqrt{\tau_{INT0}\tau_{MOS0}}\ \text{(when } C_{J0} = C_0\text{)}$$

$$\eta_J = 1 + \frac{C_{J0}}{C_0}$$

- Delay is 15% smaller when C_J is negligible.
- Delay is a geometric mean of interconnect delay and gate delay and decreases when gate is faster.

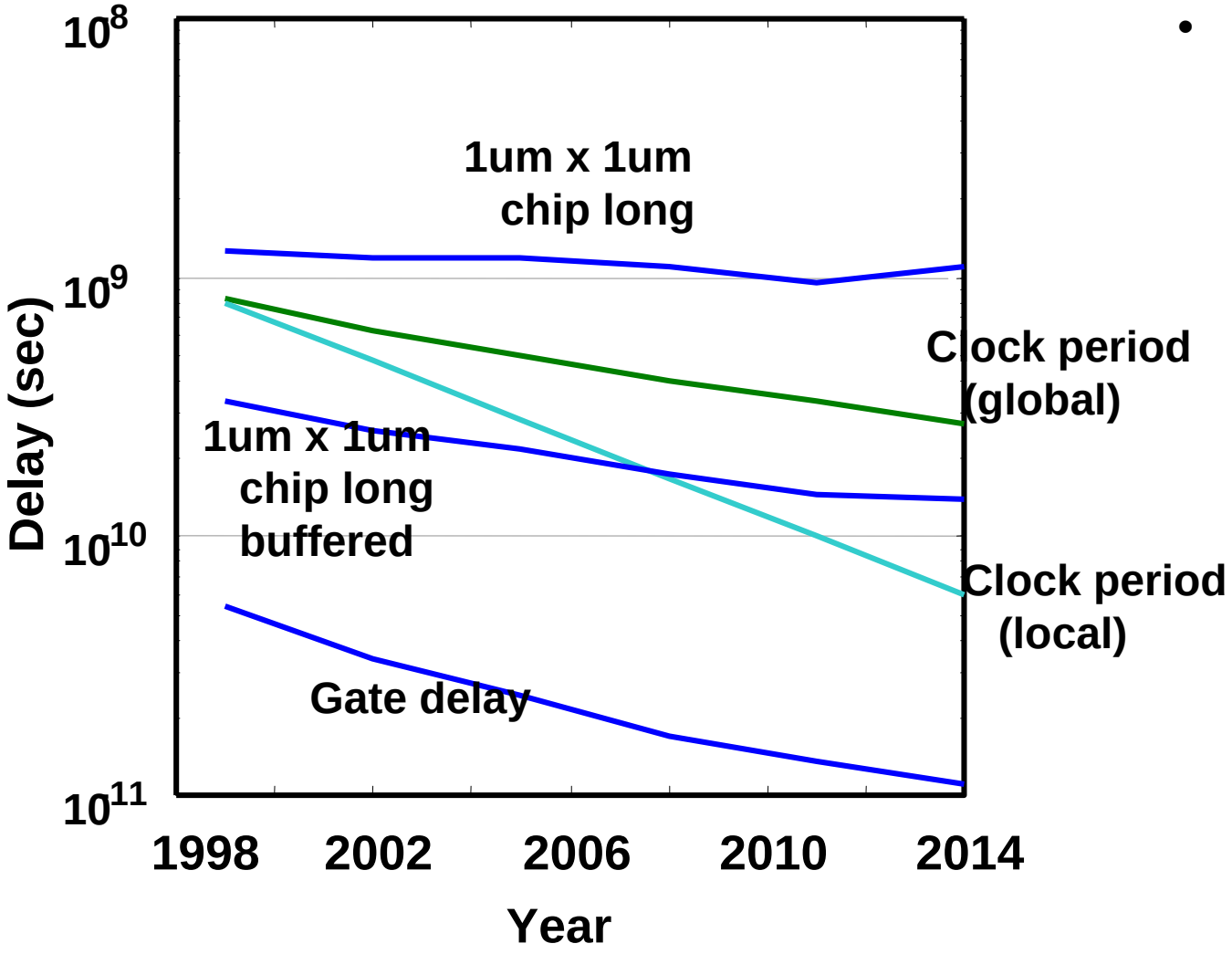
$$\Delta p\,(\text{power increase}) = k_{OPT}h_{OPT}(C_0 + C_{J0}) = \sqrt{\frac{P_1}{P_2}}\sqrt{\frac{C_0 + C_{J0}}{C_0}}C_{INT} = \sqrt{\frac{P_1}{P_2}}\sqrt{\eta_J}C_{INT}$$

$$= 0.73C_{INT}\ \text{(when } C_{J0} = 0\text{)}$$

$$= 1.04C_{INT}\ \text{(when } C_{J0} = C_0\text{)}$$

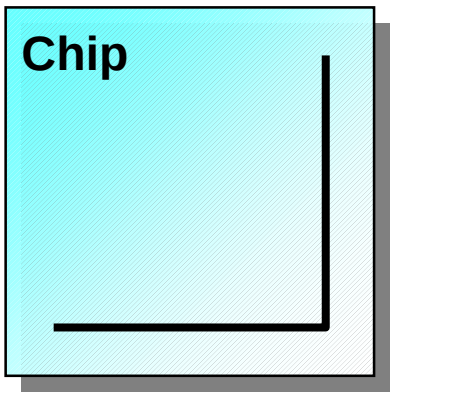
- Total power is 15% smaller when C_J is negligible.

Buffered interconnect delay

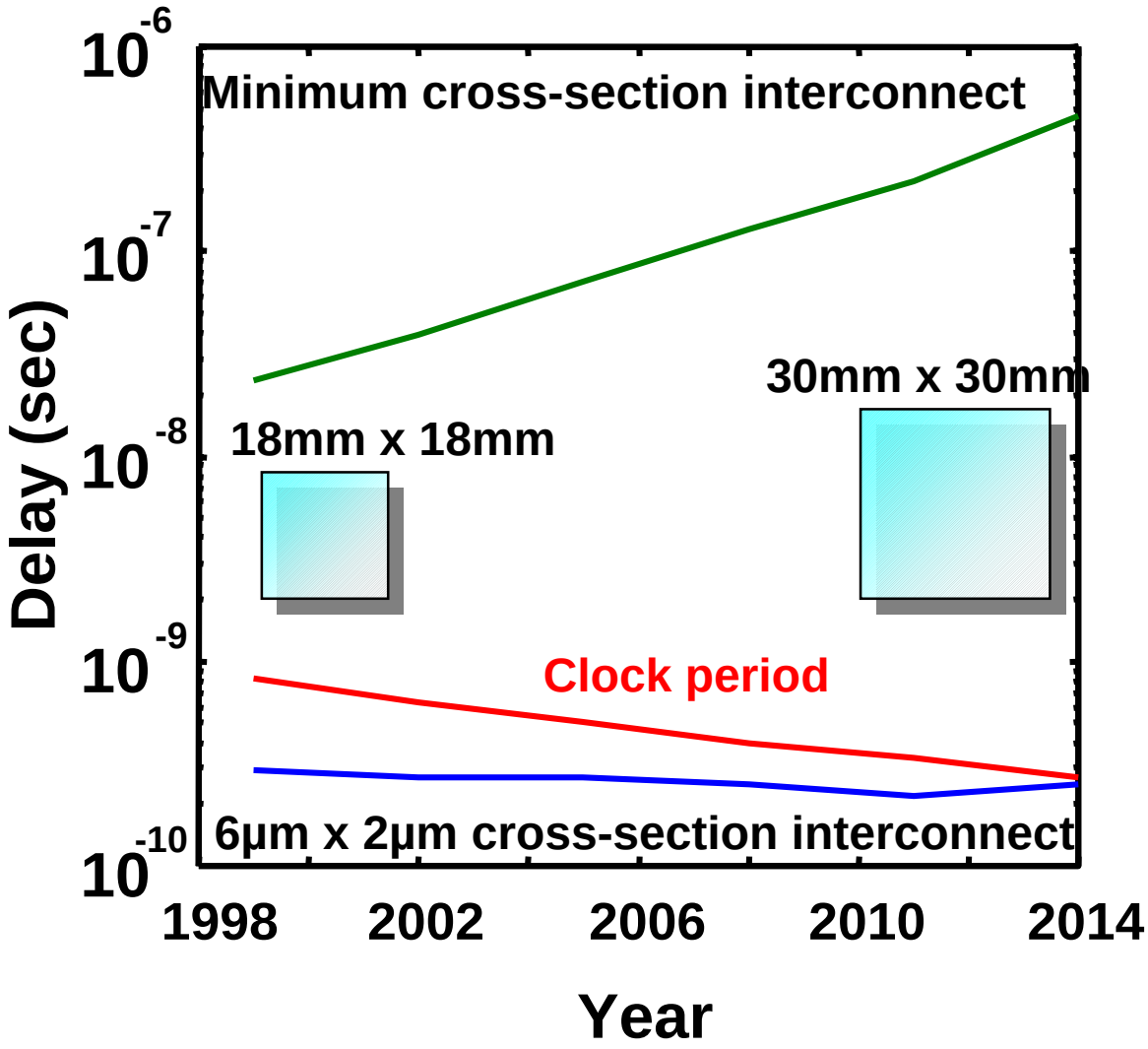


- In Emotion Engine design for PS2, about 10k buffers are inserted, which is increasing.

RC delay of global interconnections



Global interconnect



DSM interconnect design issues

Larger current

- IR drop (static and dynamic)
- Reliability (electro-migration)

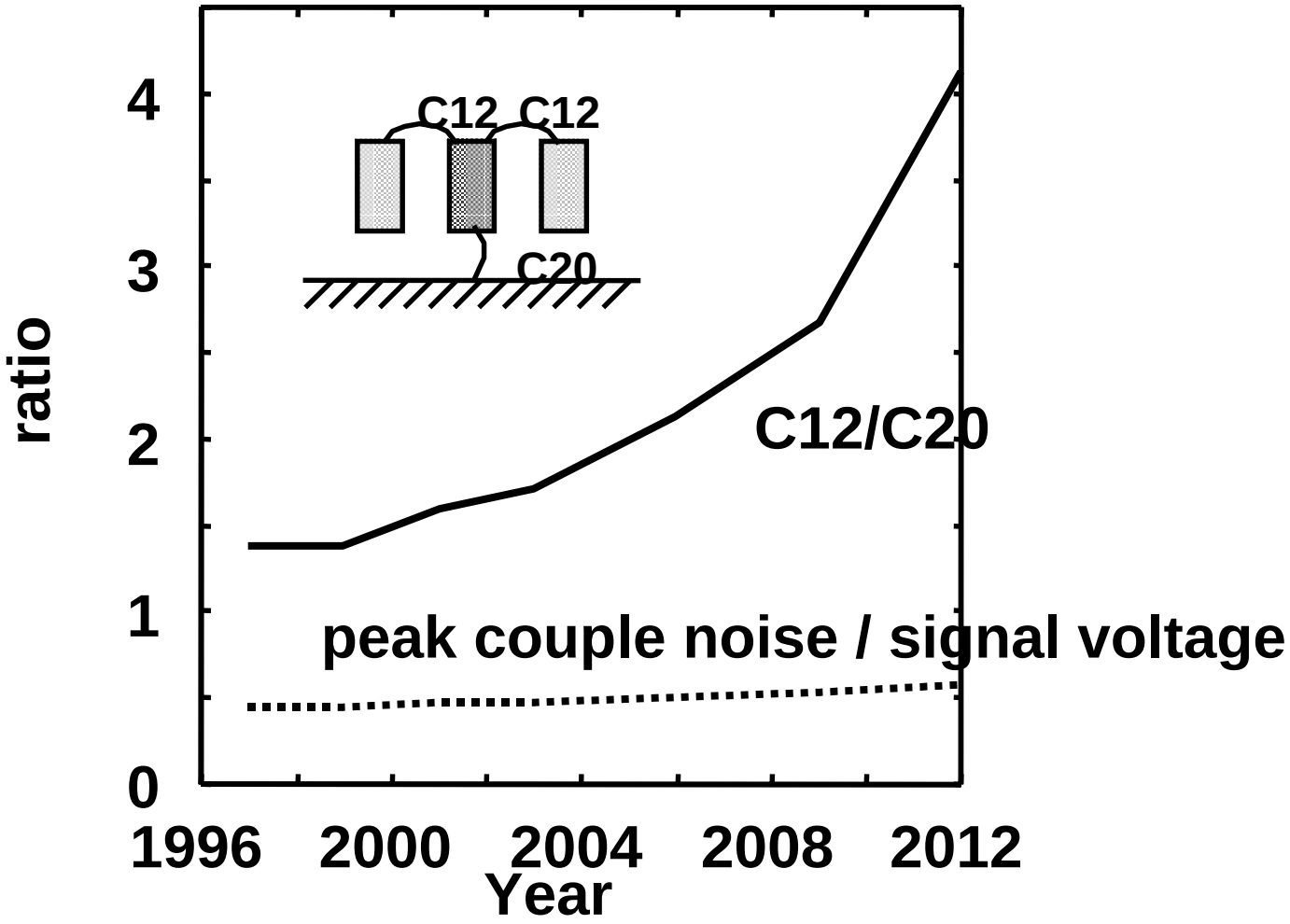
Smaller geometry / Denser pattern

- RC delay
- Crosstalk noise
- Delay fluctuation
- Signal Integrity

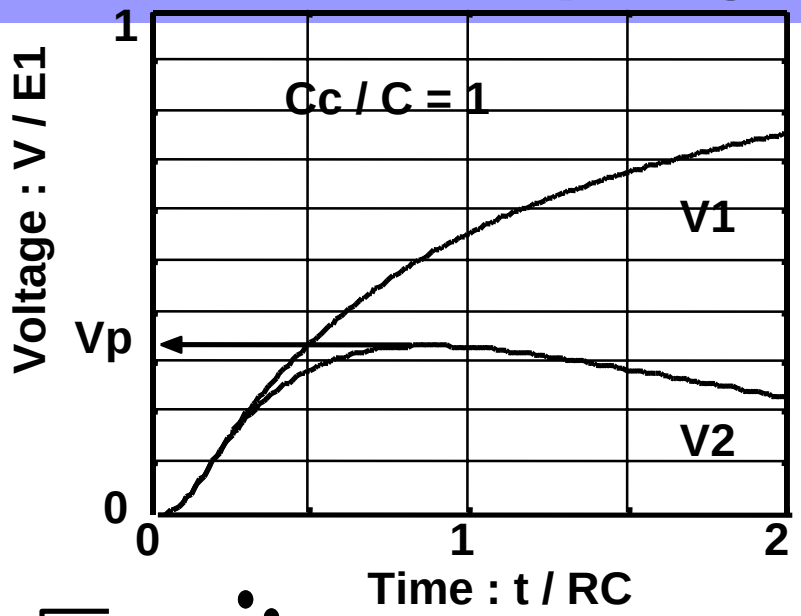
Higher speed

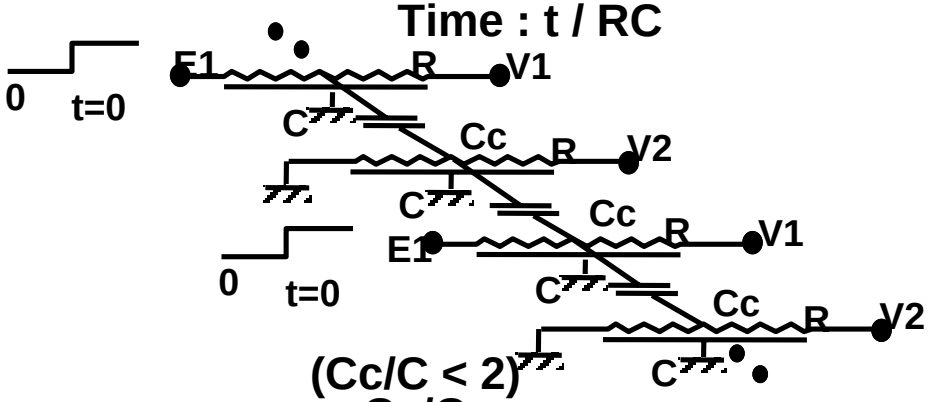
- Inductance
- EMI

Capacitive Coupling Noise



Coupling noise in RC bus

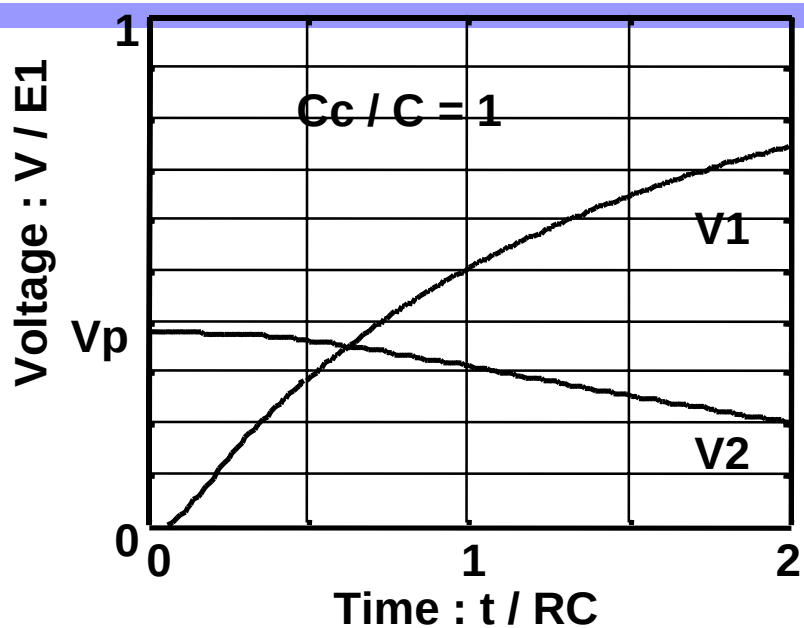


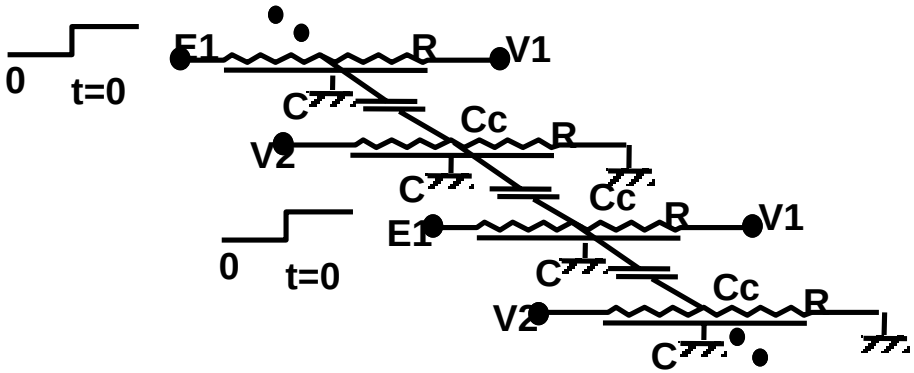


(Cc/C < 2)

$$Vp \approx \frac{Cc/C}{1+2Cc/C} \quad \text{(Bus)}$$

$$Vp \approx \frac{2Cc/C}{2+3Cc/C} \quad \text{(Three lines)}$$

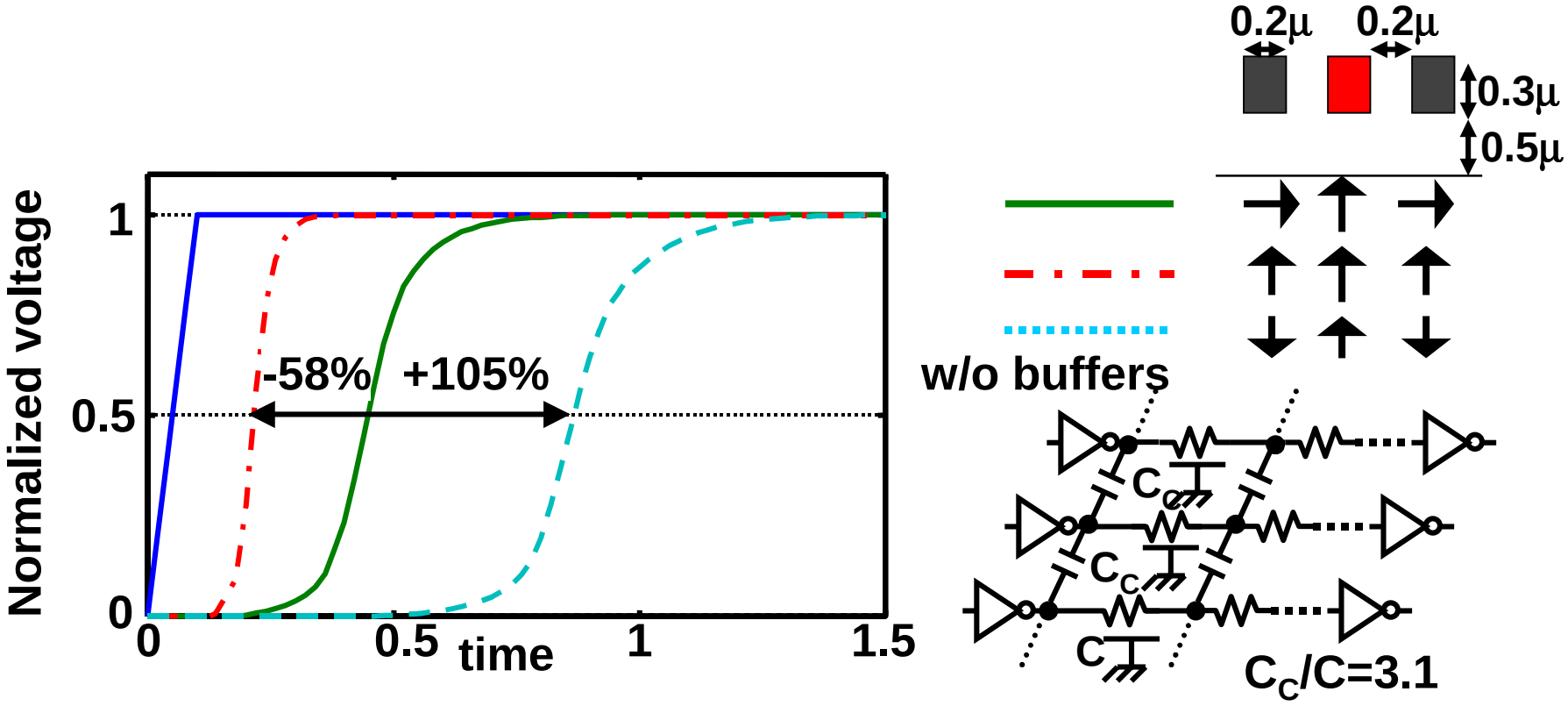




$$Vp = \frac{\sqrt{1+4Cc/C}-1}{\sqrt{1+4Cc/C}+1}$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

Coupling among Interconnections

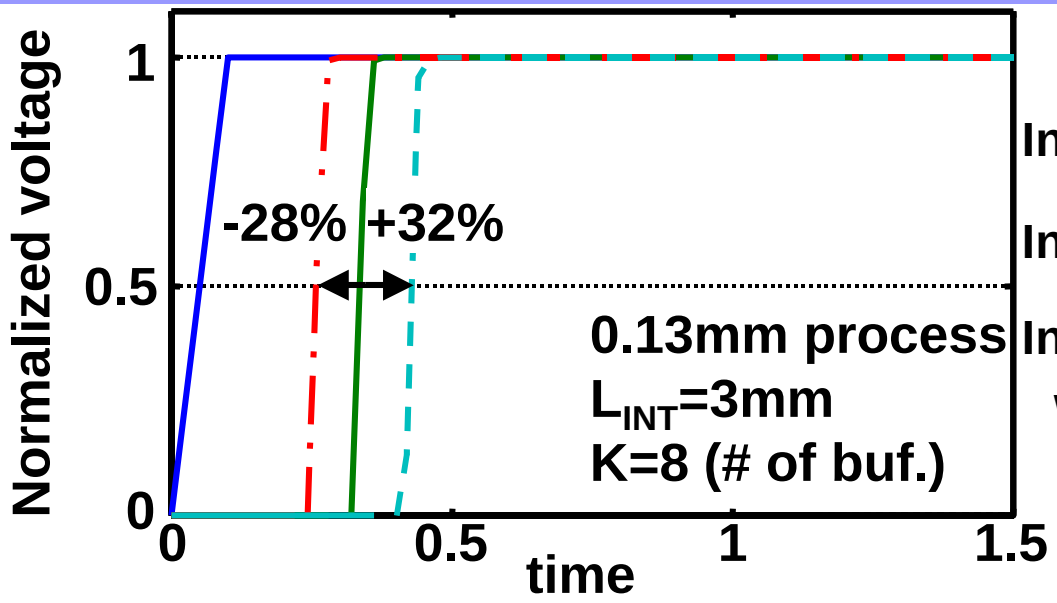


$$\frac{t_{pd}}{RC} = \frac{1}{2} + 2\eta - \frac{1}{\sqrt{6}} \log \frac{e}{2} \sqrt{1 + 8\eta + 6\eta^2}$$

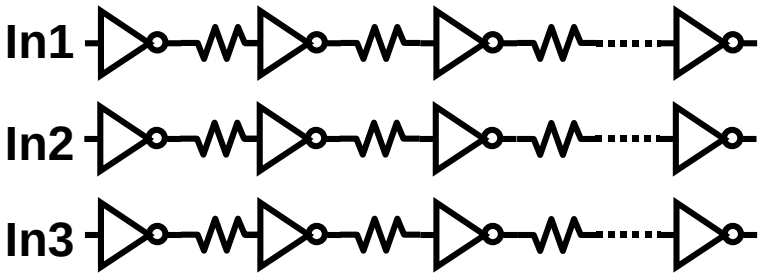
$$\approx 1.63\eta + 0.37 (\eta \le 2)\ (\eta = C_C / C)$$

H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," 1998 ASPDAC, Digest of Tech. Papers, pp.35-43, Feb. 1998.

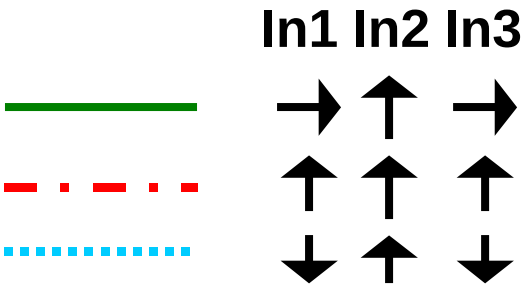
Coupling among Interconnections

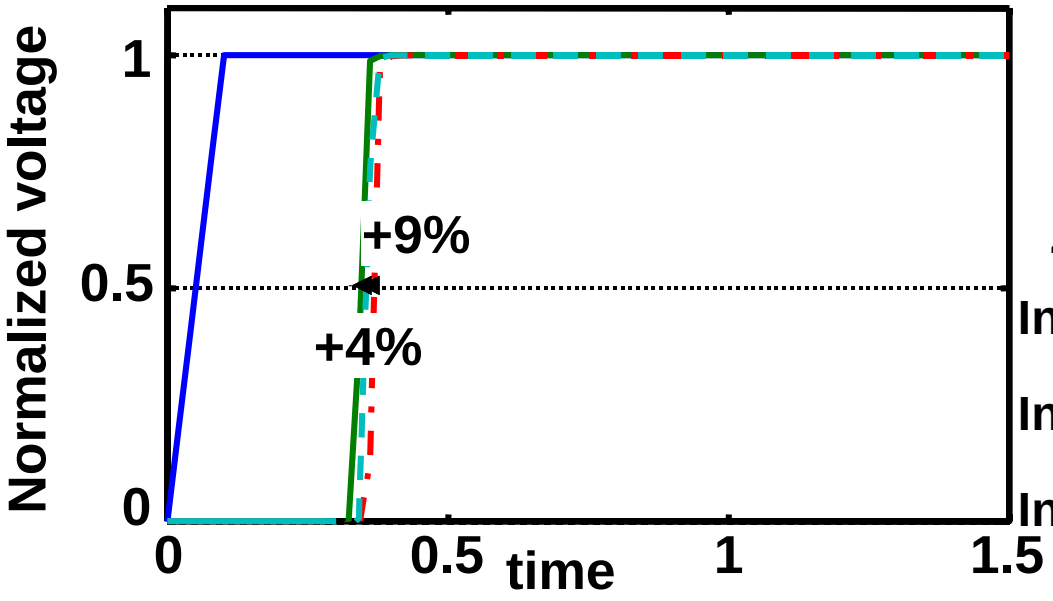


Normal buffer insertion

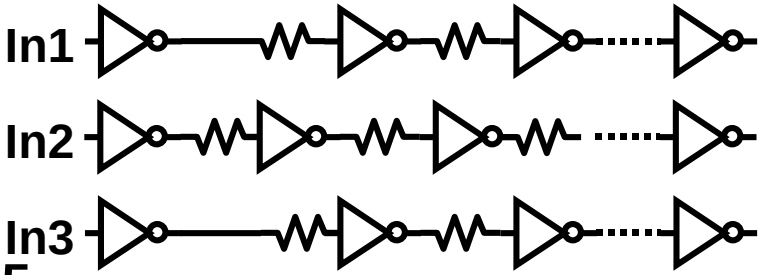


W_N/W_P=25μ/38μ





Zigzag buffer insertion



DSM interconnect design issues

Larger current

- **IR drop (static and dynamic)**
- **Reliability (electro-migration)**

Smaller geometry / Denser pattern

- **RC delay**
- **Crosstalk noise**
- **Delay fluctuation**
- **Signal Integrity**

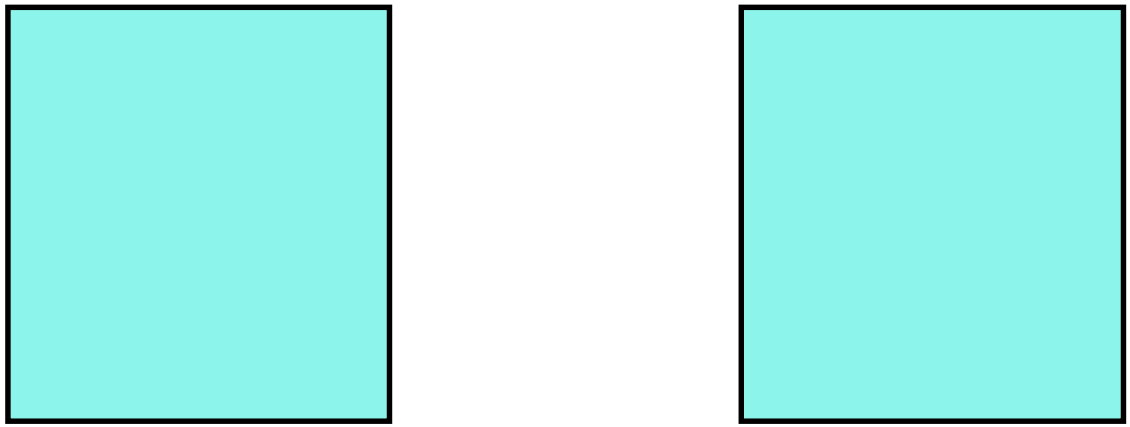
Higher speed

- **Inductance**
- **EMI**

Interconnect Cross-Section and Noise

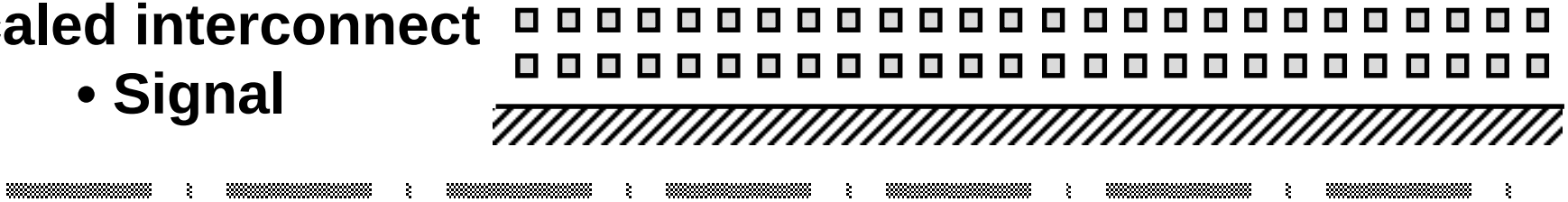
Unscaled / anti-scaled

- **Clock**
- **Long bus**
- **Power supply**



Scaled interconnect

- **Signal**



1V 20W →20A current

5% noise →0.05V noise →~0.02V / 20A→~10μm thick Cu

Thick layer interconnect, area pad, package are co-designed.

DSM interconnect design issues

Larger current

- IR drop (static and dynamic)
- Reliability (electro-migration)

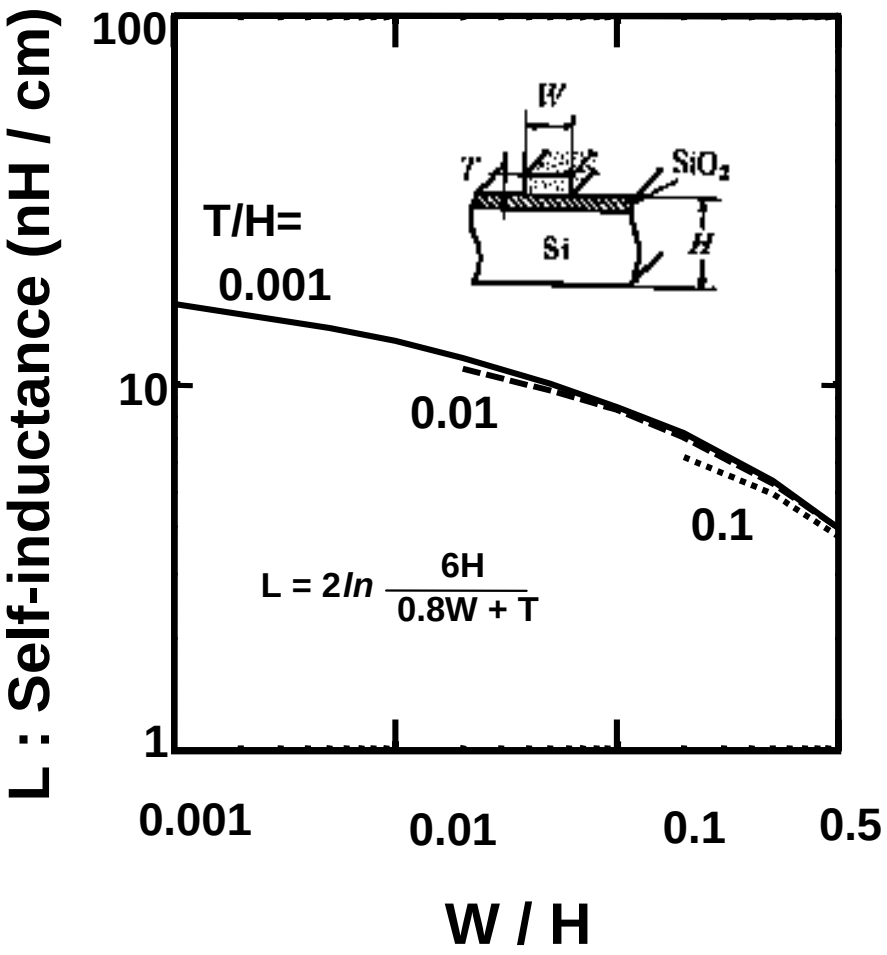
Smaller geometry / Denser pattern

- RC delay
- Crosstalk noise
- Delay fluctuation
- Signal Integrity

Higher speed

- Inductance
- EMI

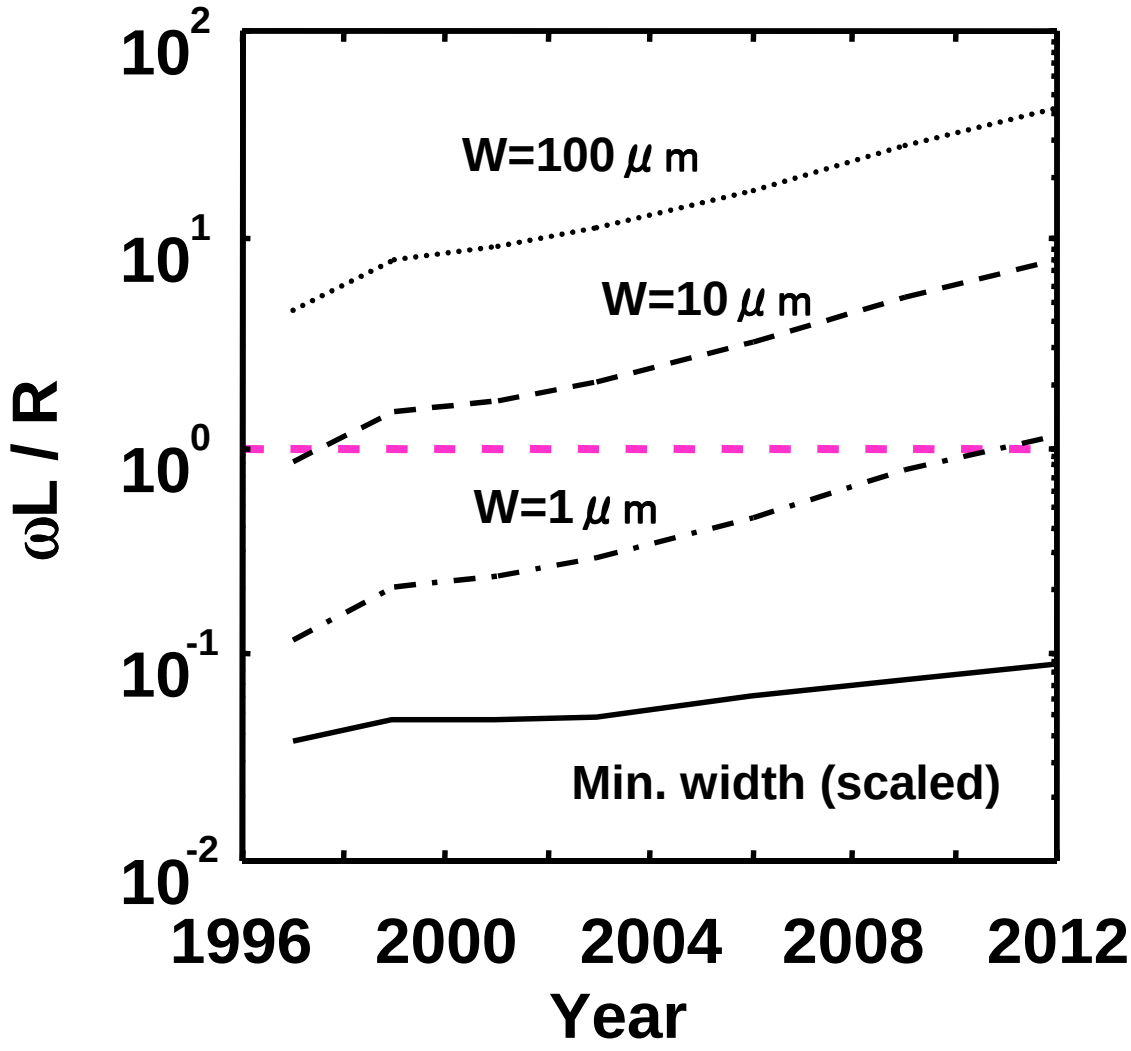
Inductance



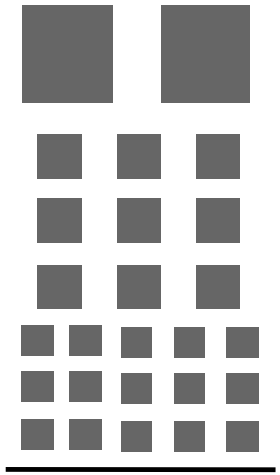
- Now RC effects surmounts LC effects because R > |jωL|.
- In the future, both of R and ωL increase (but for signal lines R > |jωL|).
- Exception in low-R lines
- Inductive effects should be considered in wide clock lines in a fast processor, power supply lines and wide-bit bus lines changed at the same time.
- Clock lines are placed on power plane to reduce inductive effects.

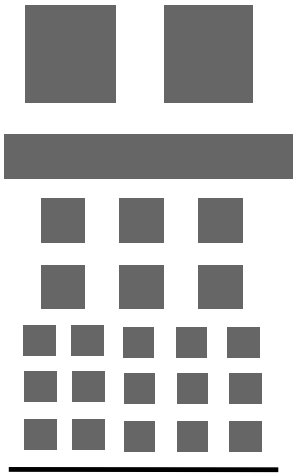
[1] D.A.Priore, "Inductance on Silicon for Sub-micron CMOS VLSI," Symp. on VLSI Circuits, 1993.

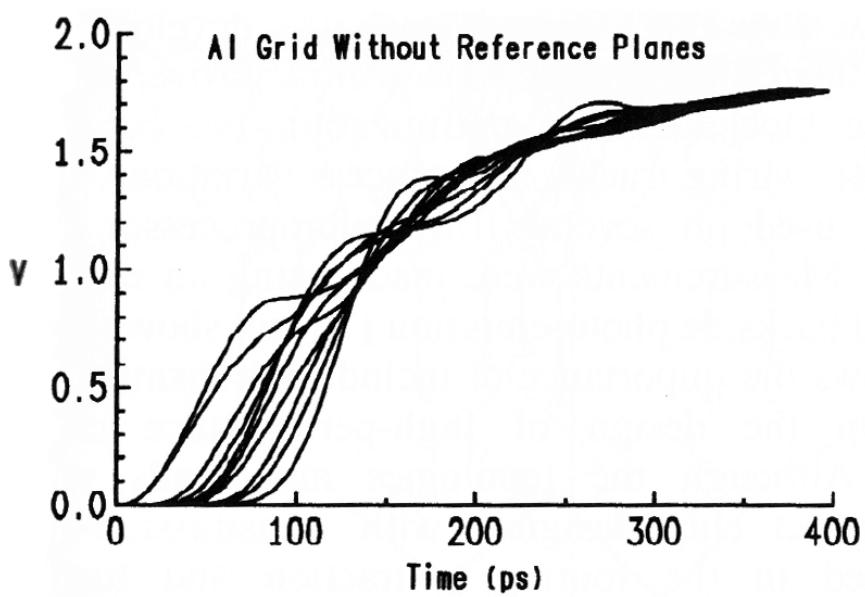
Inductive Effects

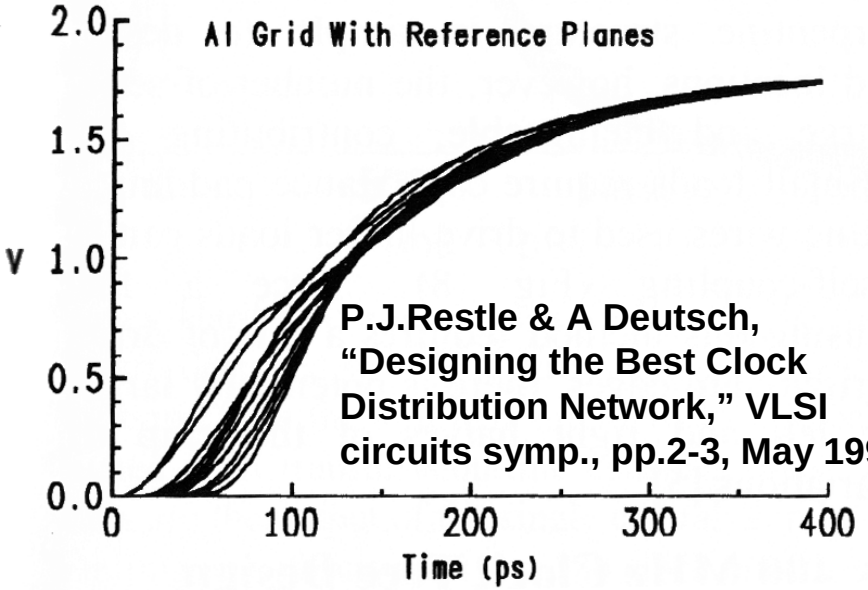


Inductive Effects in Clock Lines









P.J.Restle & A Deutsch, "Designing the Best Clock Distribution Network," VLSI circuits symp., pp.2-3, May 1998.

Board design practice is imported in LSI.

T.Sakurai

Three crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

VLSI Design in 2010

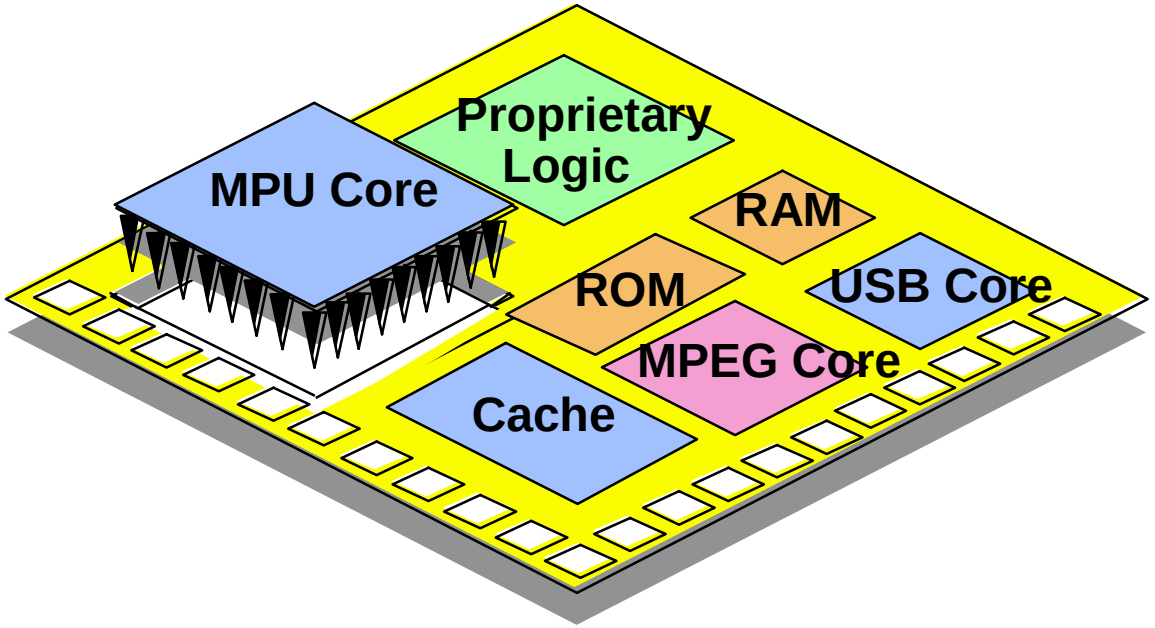
Designing a map of 10m wide roads for a world atlas

T.Sakurai

Overcome complexity crisis

- **Re-use and sharing of design**
- **Design in higher abstraction**

IP (A inc.)
IP (B univ.)
IP (C inst.)
IP (D semi.)

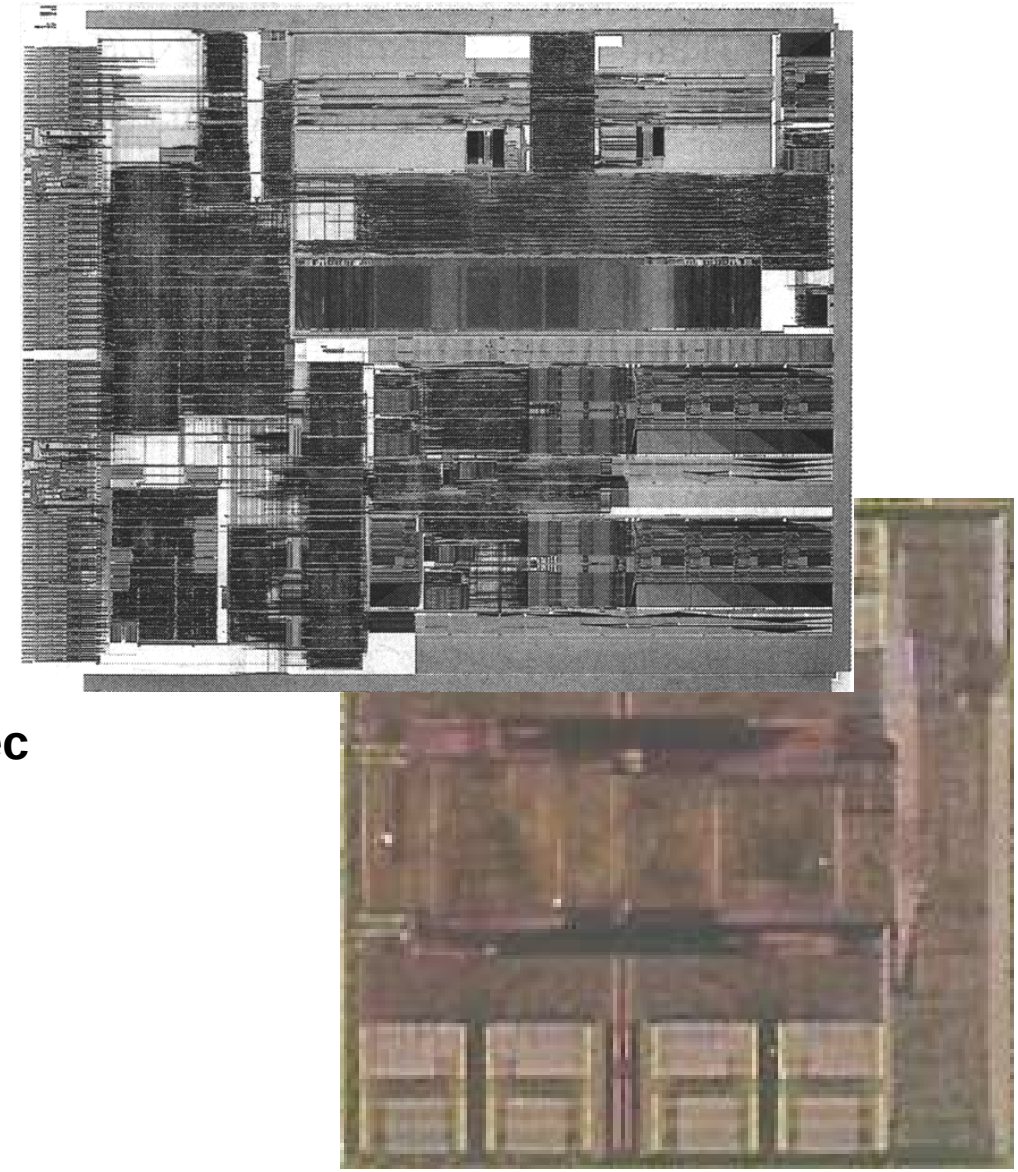


IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

System LSI for Games

- Clock freq. 300MHz
- 10M transistors
- Graphics synthesizer integrate

  40M tr. With embedded DRAM
- Memory bandwidth 3.2GB/s
- Floating operation 6.2GFLOPS/sec
- 3D CG 6.6M polygon/sec
- MPEG2 decode

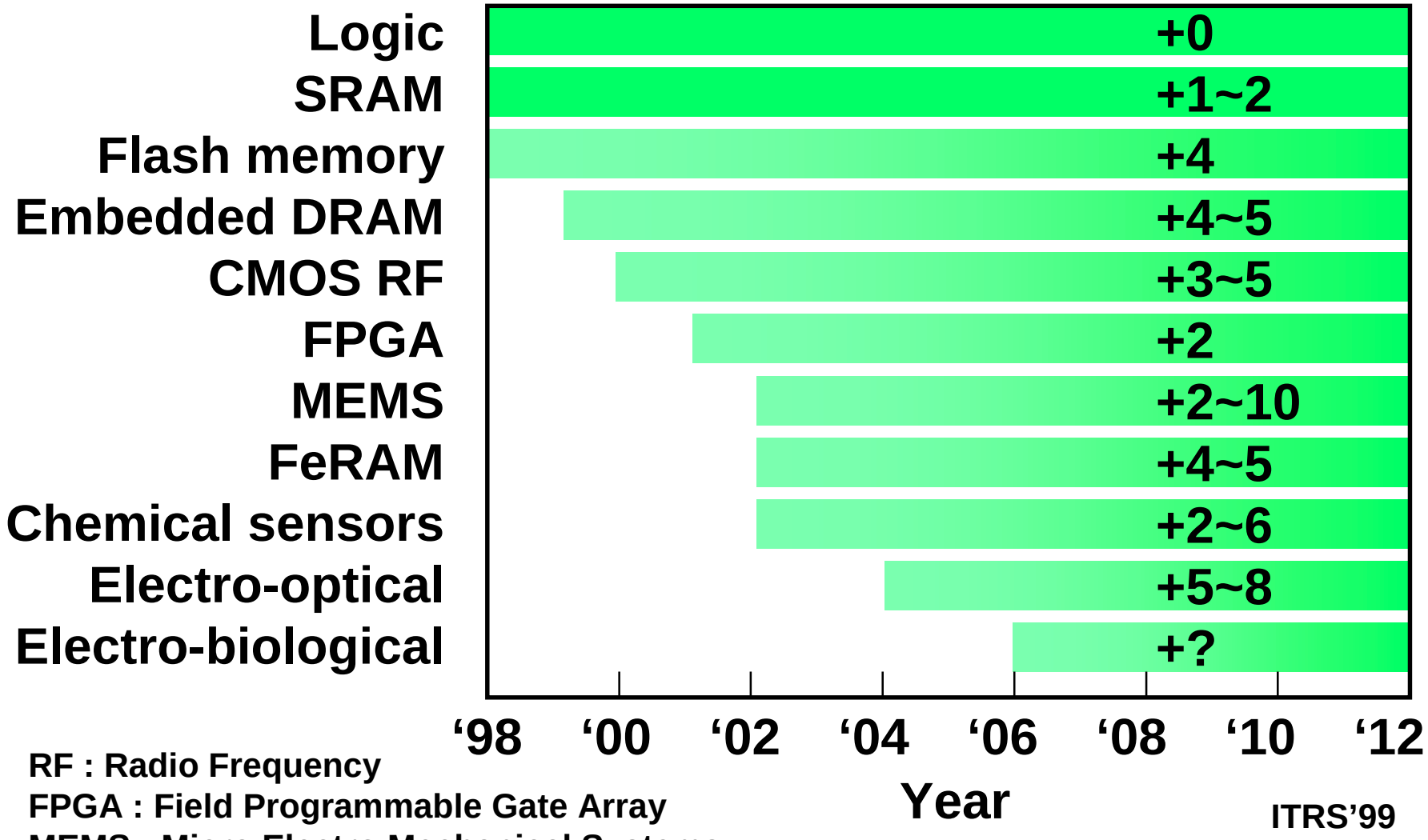


T.Sakurai

Issues in System-on-Chip

- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

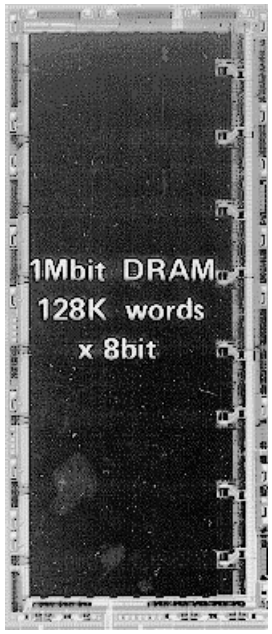
Technologies integrated on a chip

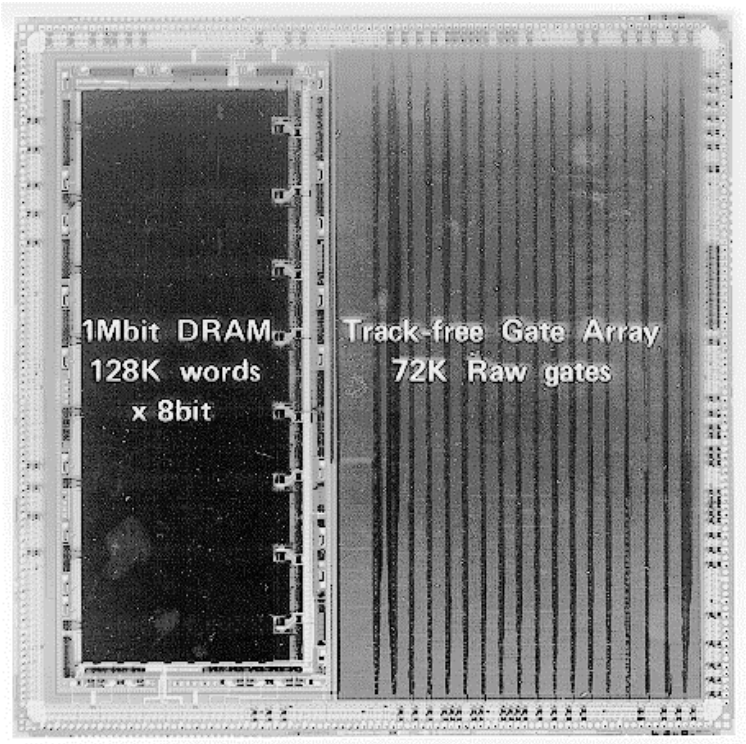


ITRS'99

RF : Radio Frequency
FPGA : Field Programmable Gate Array
MEMS : Micro Electro Mechanical Systems
FeRAM : Ferroelectric RAM

DRAM embedding





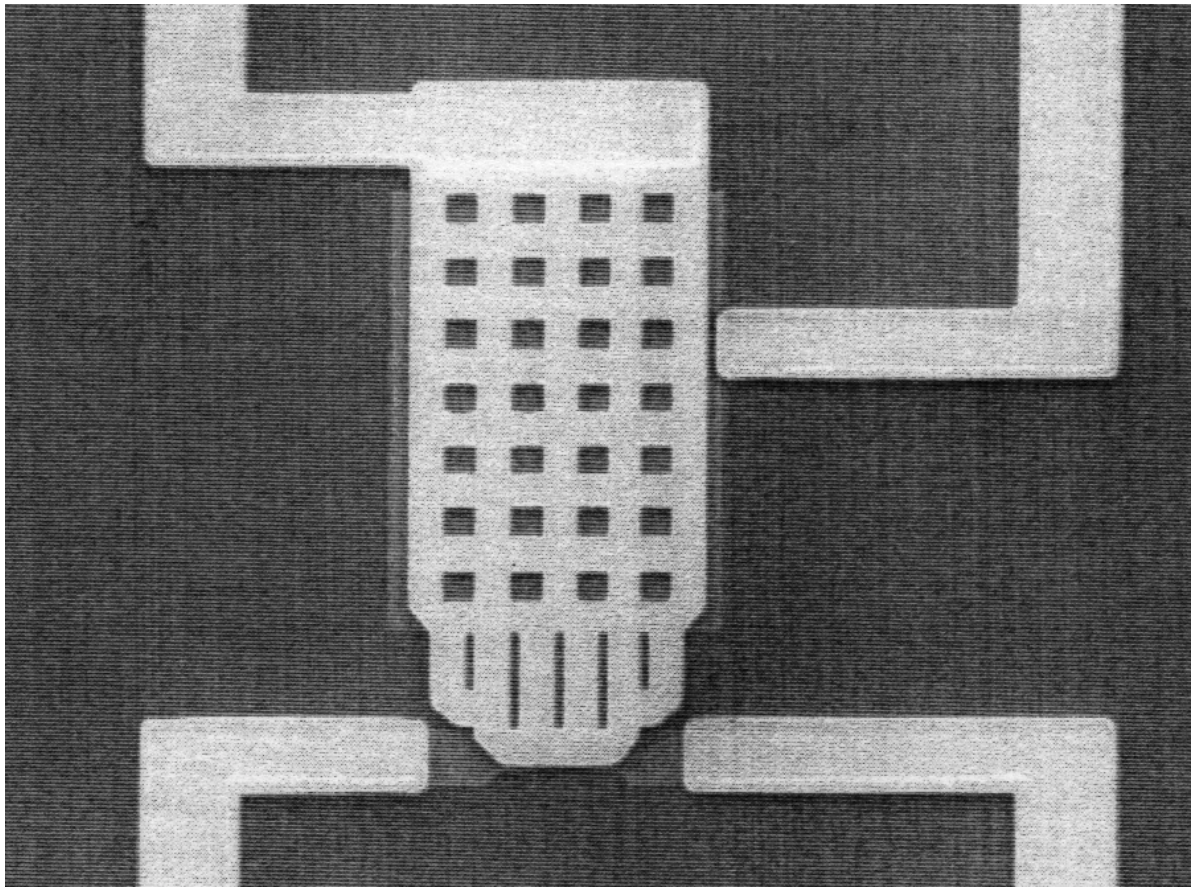
DRAM **Processor** **System LSI**

K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- **Two orders of magnitude improvement in bandwidth and power**

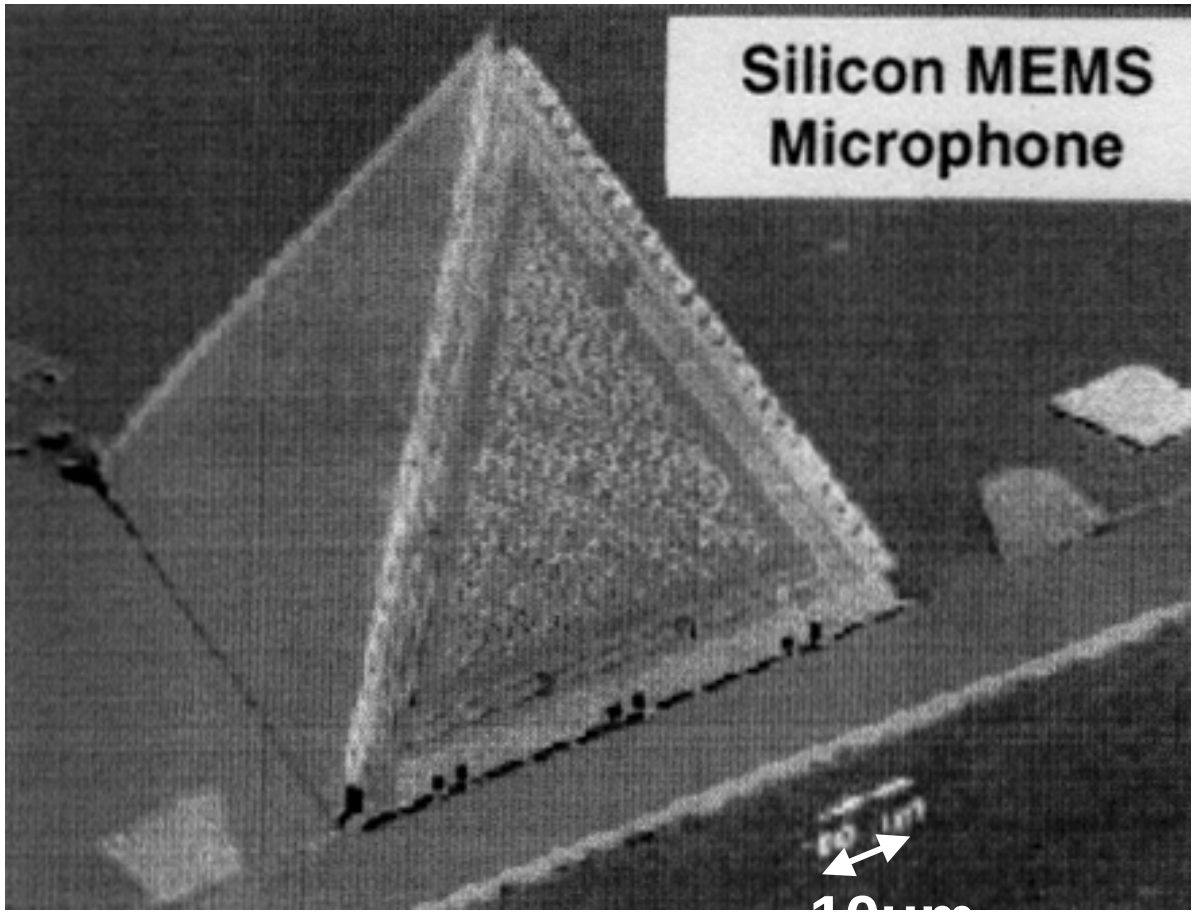
BUT EXPENSIVE!

Micro-machined mechanical switch



G.Weinberger, “The New Millennium: Wireless Technologies for a Truly Mobile Society,” ISSCC, pp.20-24, Feb. 2000.

Silicon MEMS microphone



Will soon exceed the performance of the best commercial microphones, yet be inexpensive and potentially integrated with on-chip electronics.

M.Pinto, "Atoms to Applets: Building Systems ICs in the 21st Century," ISSCC, pp.26-30, Feb. 2000.

System-in-Package

ELECTRONIC ENGINEERING
EE TIMES
eet.com The industry newspaper for engineers and technical management Monday November 8, 1999

Expanding role of packaging seen relegating SoC to niche status

System-chip may topple . . .

By Robert Ristelhueber

INDIAN WELLS, CALIF. – The wheels might be coming off the system-on-chip (SoC) bandwagon, if the chatter at last week's Dataquest Semiconductor conference is any barometer of industry sentiment. Heavyweights including IBM and Lucent Technologies indicated that costs may relegate SoC to niche status, with new packaging techniques stepping into the breach.

"A couple of years ago we really thought that the embedded DRAM model would be the panacea for many applications," said John Kelly, general manager of IBM Microelectronics. "It's not always the right thing. In many applications it still remains much cheaper to do it with multichip modules. It gives you satisfactory performance and often for lower cost."

"We have systems-on-chip now that are really 'system on chips,' " said John Dickson, president of Lucent Technologies' Microelectronics Group. "We do it that way because it's most cost-effective, and the customer will prefer it that way because it offers more flexibility."

The subject was broached at the conference here by a Dataquest analyst who claimed that SoC designs will increasingly be supplanted in coming years by multichip packaging as higher mask costs squeeze SoC profitability.

Chip designers have often been willing to add mask steps

▸CONTINUED ON PAGE 6

IBM's Kelly: 'In many apps, cheaper to do it with multichip modules.'

. . . as industry grapples with impact of cores mode

By Peter Clarke and Brian Fuller

EDINBURGH, SCOTLAND – Intellectual property cores were a hot topic last week, both here at the IP99 Europe conference and at Dataquest Inc.'s annual semiconductor conference in Indian Wells, Calif. But as the industry struggles with new business models, new customer-supplier relationships and fast-moving technology, there was scant agreement on either side of the Atlantic on how the cores market will unfold.

On one thing there was agreement: IP cores and design reus

In some apps, multichip modules do the job more cheaply, conference told

'System-in-package' could make SoC a niche

▸CONTINUED FROM PAGE 1

and complexity to their logic devices in order to place analog and memory functions onto chips. "But when we get below 0.2 micron we get a cost shock, and the [return on investment] will be diminished or even eliminated in many cases," said Clark Fuhs, vice president and director of Dataquest's Semiconductor Manufacturing Programs.

Mask costs will dramatically rise at deep submicron because of the use of phase-shift and optical proximity correction techniques as well as more expensive, 193-nm lithography equipment, putting low-volume SoC at a cost disadvantage, Fuhs said.

Militating against SoC designs for many applications is the wide disparity in revenue per square inch among the various blocks in the chip, Fuhs said. "The DSP or microprocessor block can be getting $150 or $200 per square inch, the FPGA about $120, the analog block about $35, the memory block about $50 to $60 . . . You're basically diluting your high-value logic pieces with all these other low-value pieces, yet you're adding cost because you're adding mask levels."

An alternative is to fabricate the different blocks as discrete chips, placed close together using chip-scale packaging, Fuhs said. "This enables you to build the pieces in fabs that are optimized for those pieces. You can build analog in a 0.7-micron fab, standard logic can be done in 0.35 or even 0.5 micron, and for the memory you can buy a wafer from somebody and break it up. The package is more expensive, but the overall system cost is going to be substantially less.

"The concept here is to take some level of interconnect . . . and simply move [it] from the chip into the package."

Fuhs noted that Intel's Pentium III is actually an 11-level-metal device—six levels of aluminum inside the chip and five levels of copper outside. And he showed a photograph of a Sony digital Handycam, which he said contains 20 chip-scale devices, "so this technology is here, it's real."

National's Halla touts 'integrated disintegration.'

In the not-too-distant future, he said, wafer foundries will give customers a choice of implementing a design either as a system-on-chip or as several discrete devices using chip-scale packaging.

To survive, the SoC must evolve to fit a more standard-product model that would allow it to increase volume and become more cost-efficient, Fuhs said. He predicted that within five years, multichip packaging will be growing faster than SoC designs.

That view has its detractors. "Mask sets cost in excess of a couple hundred thousand dollars, whether you do small chips or large chips," said National Semiconductor Corp. chief executive officer Brian Halla, who has championed the notion of an information appliance-on-a-chip. "I can get tremendously more performance out of the same square inches of silicon by having it all together instead of having it two inches apart on a board.

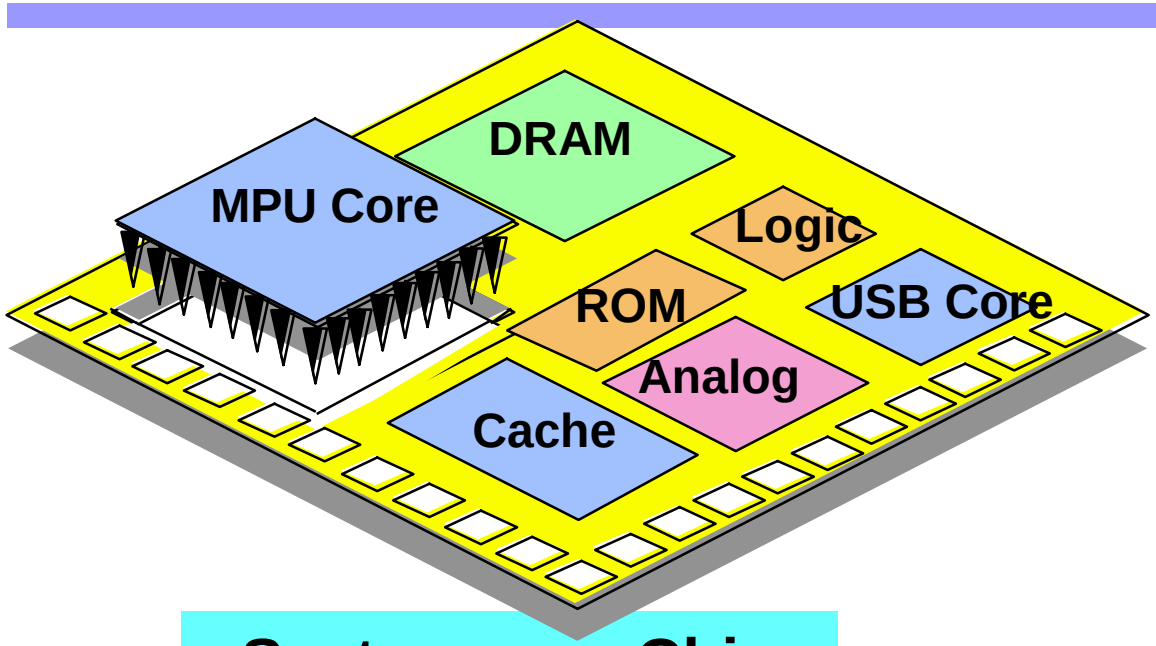
"SoC isn't a marketing crusade anymore; it's something you can do because the technology allows it," Halla added. "A very small die can contain an awful lot of functionality."

Halla noted that Intel used to say graphics shouldn't be combined with the microprocessor, because the pace of innovation differs between those parts; but Intel's upcoming Timna processor, he said, combines both functions.

"Having said all that, there are cases where we agree [about putting a system on a package]," he said. "There is a substrategy of ours called integrated disintegration, which means there are analog functions you can pull off the chip because they are such a tiny portion of the overall chip, and yet they are the most difficult thing to port to the next-generation [process] technology."

IBM's Kelly said that "SoC integration has to be done se-

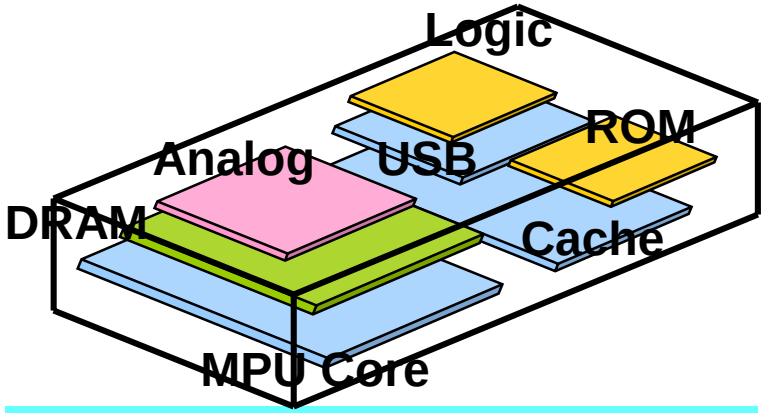
SoC vs. SiP



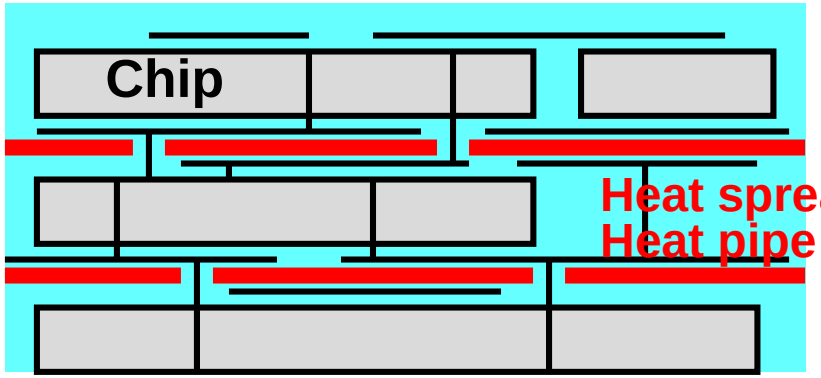
System on a Chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

- Heat dissipation is an issue

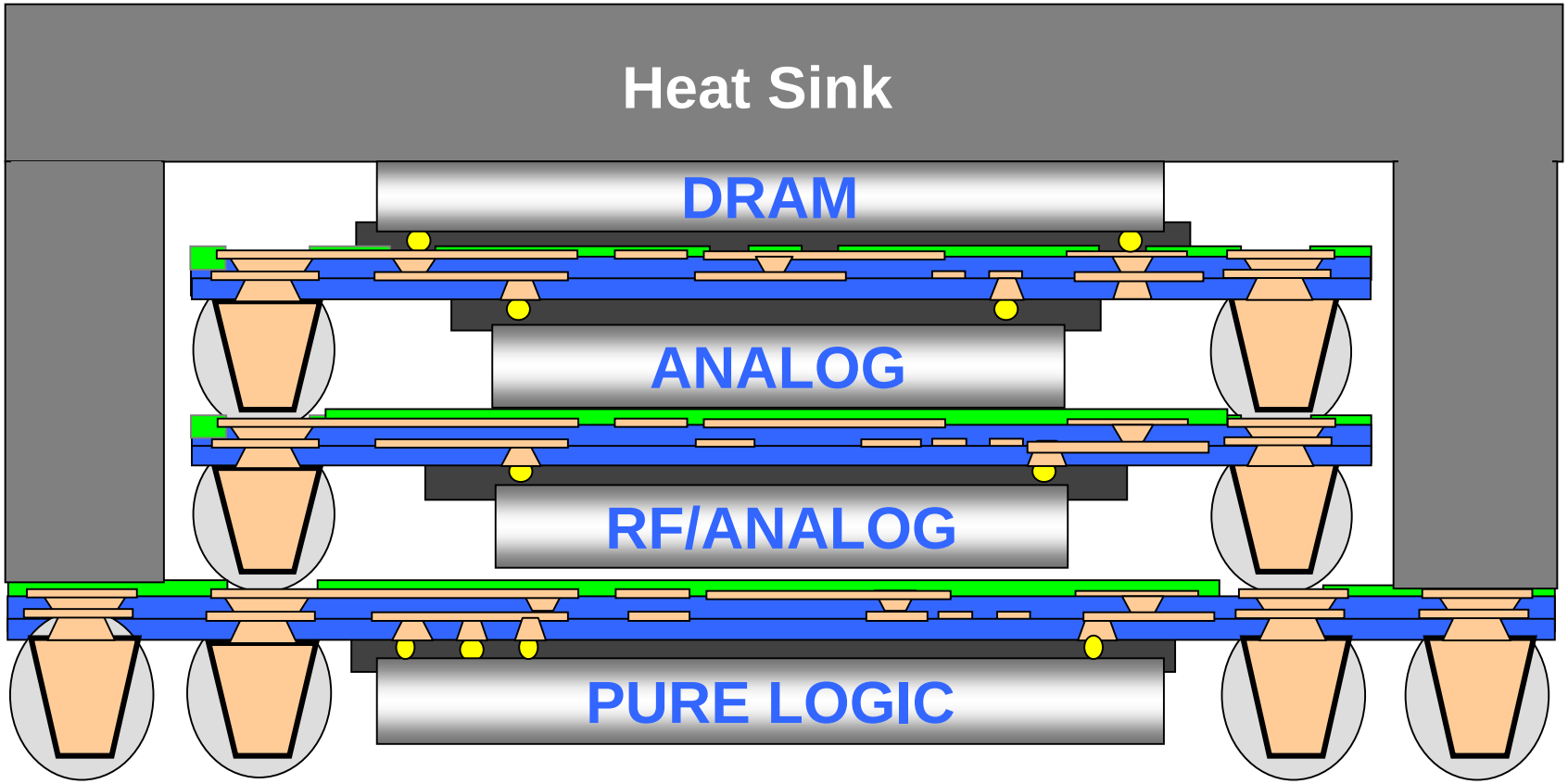


System in a Package



T.Sakurai

Superconnect example based on three-dimensional assembly

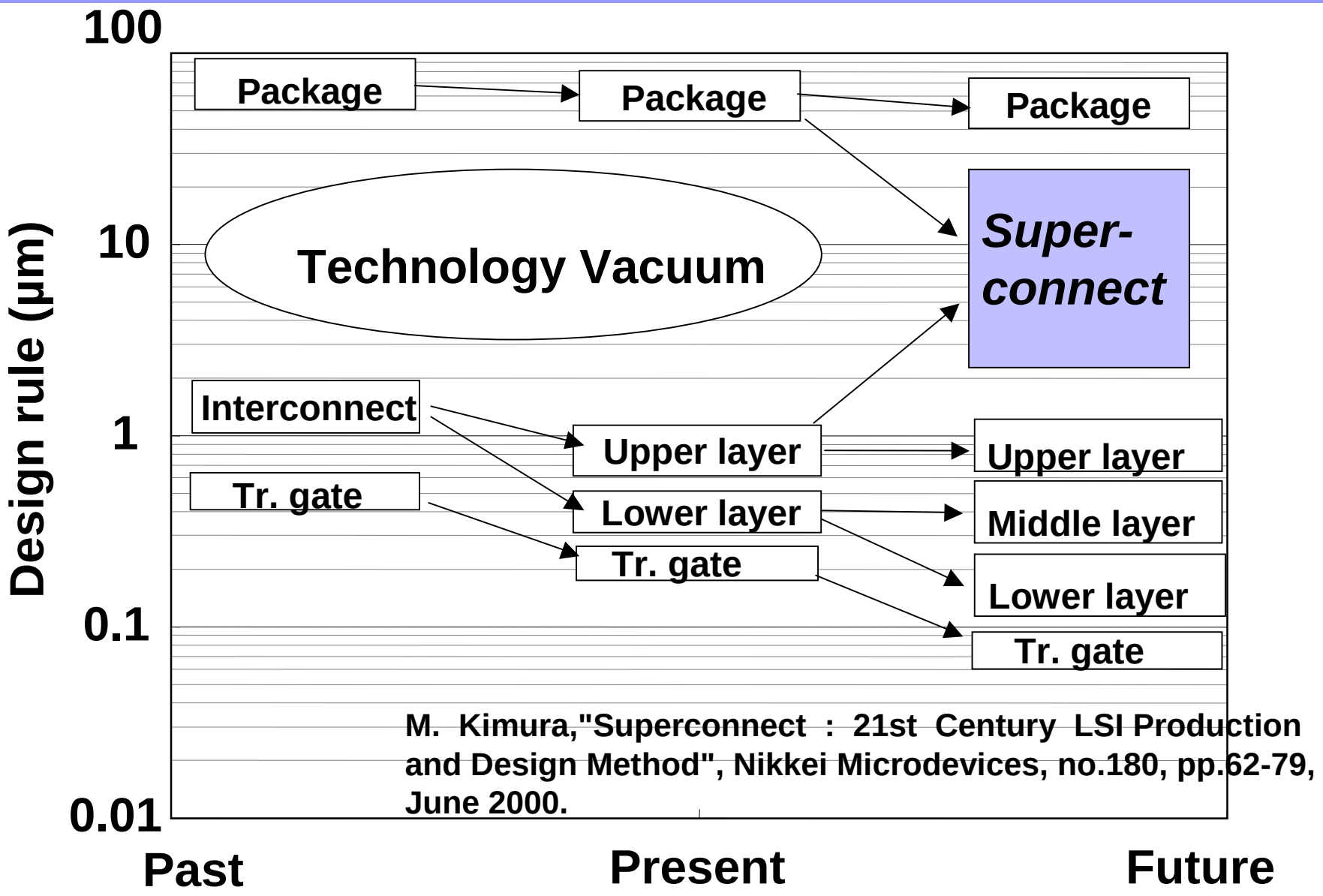


K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, “3-D Assembly Interposer Technology for Next-Generation Integrated Systems,” ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

System-in-Packageの課題

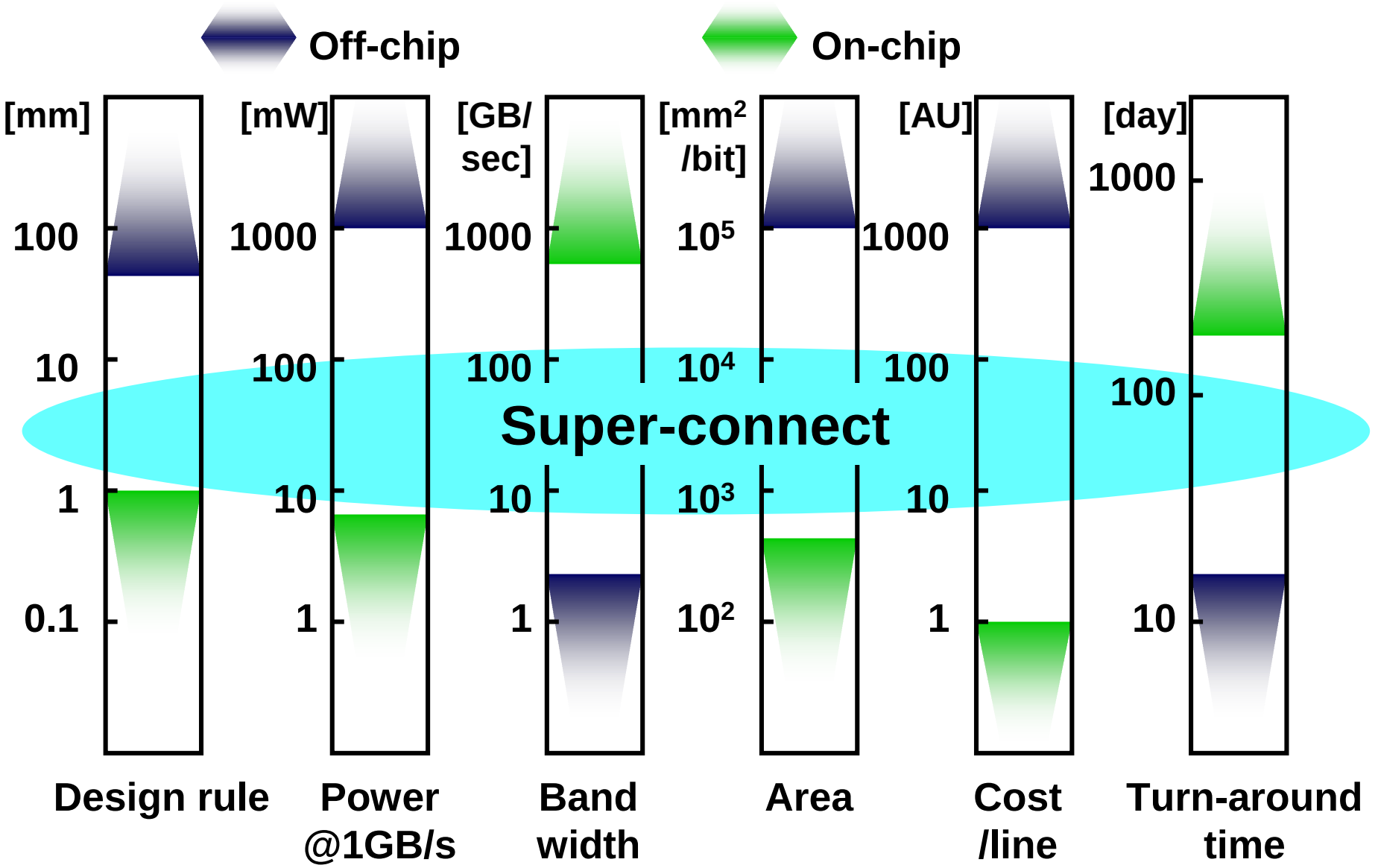
- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

Super-connect technology



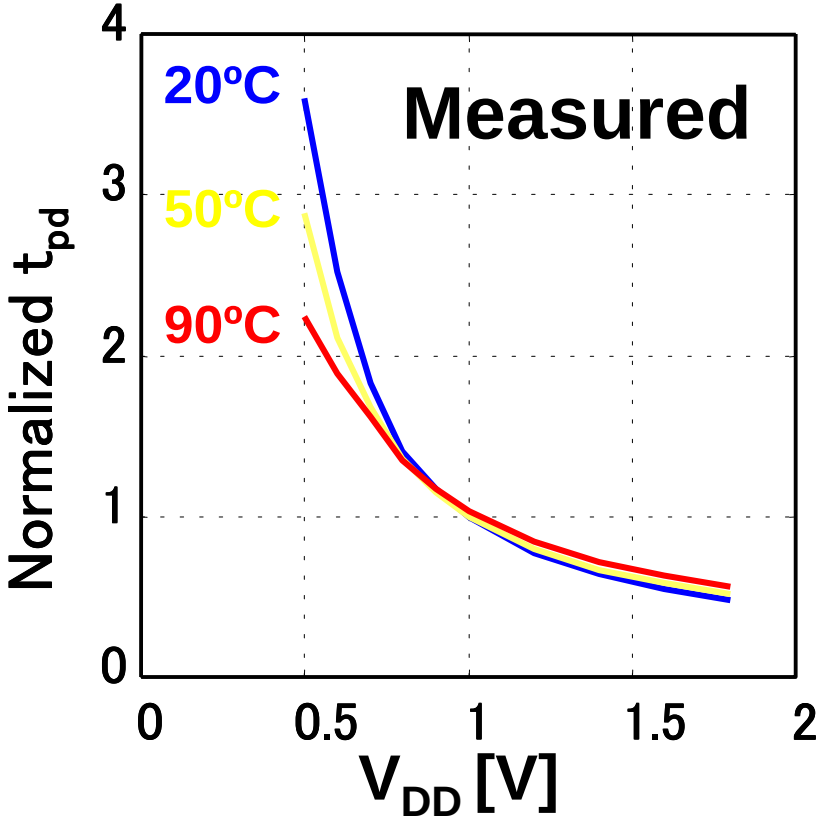
M. Kimura,"Superconnect : 21st Century LSI Production and Design Method", Nikkei Microdevices, no.180, pp.62-79, June 2000.

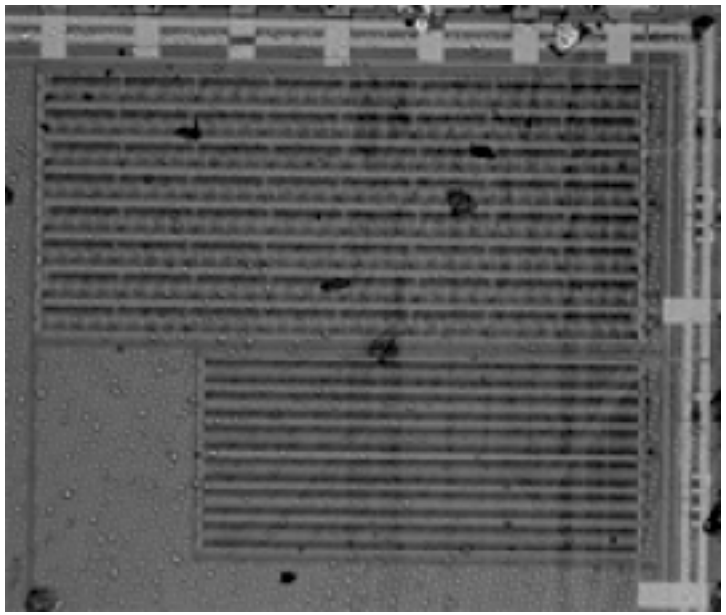
Super-connect



T.Sakurai

0.5V LSIでの逆温度特性





Photograph of 32bit FA

0.3μm CMOS

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

Assembly & Packaging

“There is an increased awareness in the industry that assembly and packaging is becoming a differentiator in product development.”

International Technology Roadmap for Semiconductors, ITRS’99 p.213

LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	μm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (μP)		21M	3.6G	170
DRAM capacity		1G	1T	1000
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	μcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

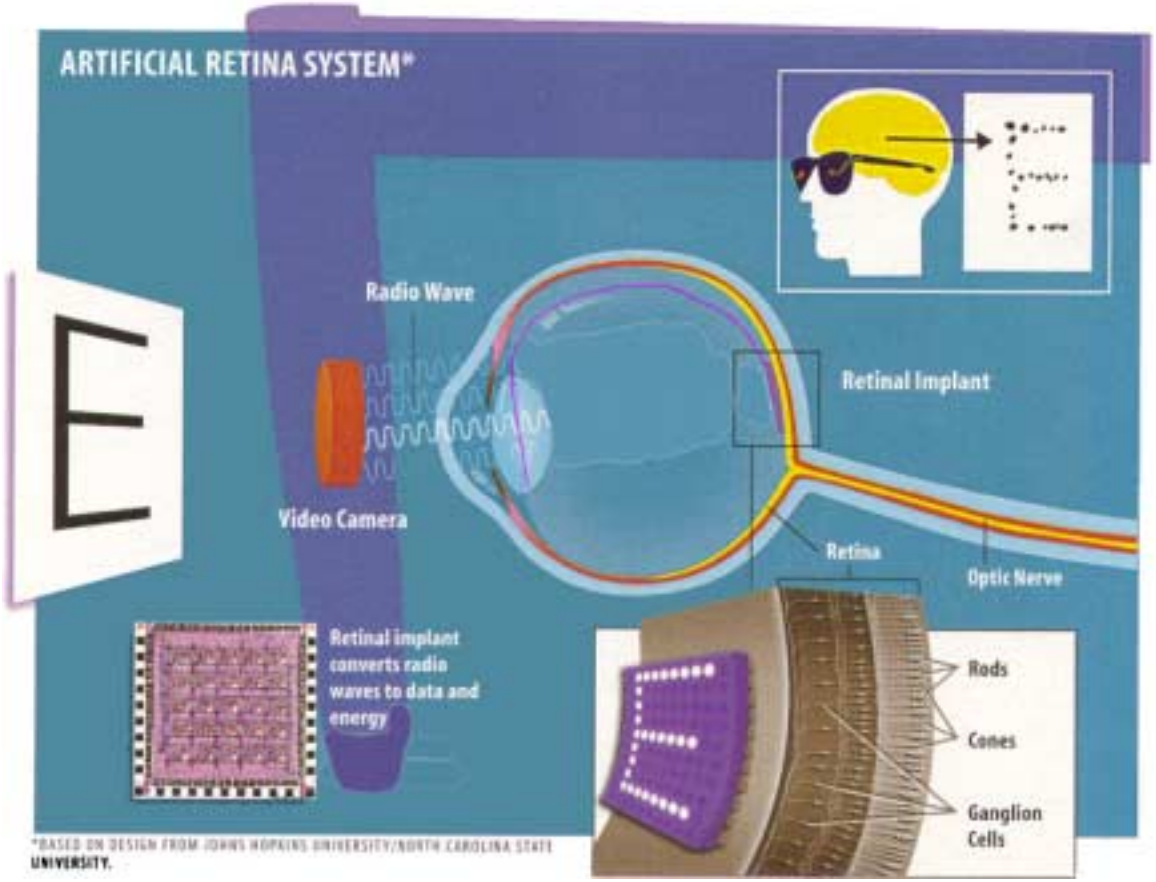
International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA) , International Technology Roadmap for Semiconductors: 1999 edition. Austin, TX:International SEMATECH, 1999.

T.Sakurai

Prosthesis - Dual Intraocular Units

NC STATE UNIVERSITY

Retinal Prosthesis



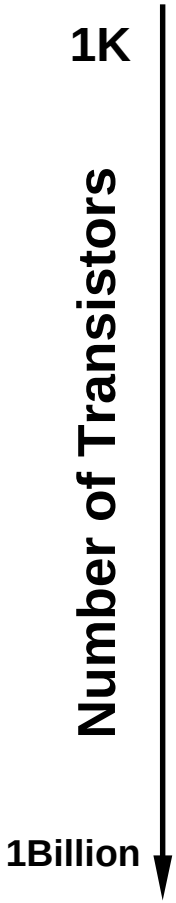
Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html

Summary – Interconnect & SiP

- New possibilities with buffered interconnects may open up new tools opportunity.
- Silicon-in-Package needs new tools that support co-design of VLSI's, package and assembly.

  New design closure issues

Super-expoenentially increasing design challenges



Functionality + Testability

Functionality + Testability + Wire delay

Functionality + Testability + Wire delay+ Power management

Functionality + Testability + Wire delay+ Power management + Embedded software

Functionality + Testability + Wire delay+ Power management + Embedded software + Signal integrity

Functionality + Testability + Wire delay+ Power management + Embedded software + Signal integrity + RF

Functionality + Testability + Wire delay+ Power management + Embedded software + Signal integrity + RF +Hybrid chips

Functionality + Testability + Wire delay+ Power management + Embedded software + Signal integrity + RF +Hybrid chips + Packaging

Functionality + Testability + Wire delay+ Power management + Embedded software + Signal integrity + RF +Hybrid chips + Packaging + Management of physical limits

ITRS'99