実装プロセス工学シンポジウム
「スーパーコネクトに対応した層間接続プロセス」 2001年5月18日

スーパーコネクト（基調講演）

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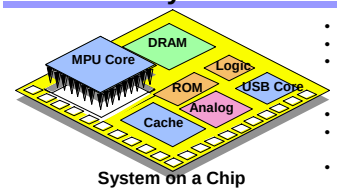
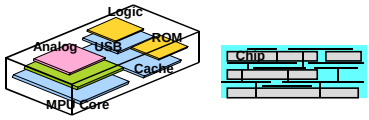
System in Package



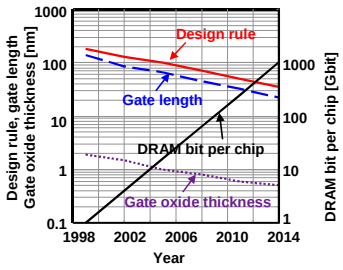
System on a Chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via
- Heat dissipation is an issue



System in Package

Moore's Law

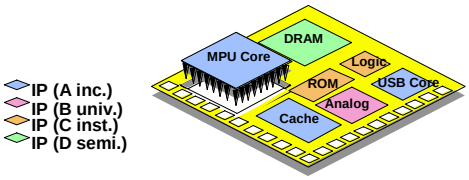


System-in-Packageの課題

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology
- low-cost, available known good die (reworkablility and module testing)

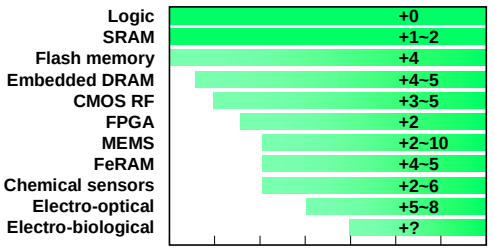
System on a Chip (SoC)

- Re-use and sharing of design
- Design in higher abstraction



IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

Technologies integrated on a chip



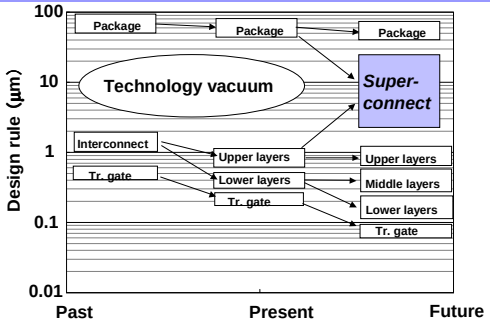
RF : Radio Frequency
FPGA : Field Programmable Gate Array
MEMS : Micro Electro Mechanical Systems
FeRAM : Ferroelectric RAM

ITRS'99

Issues in System-on-Chip

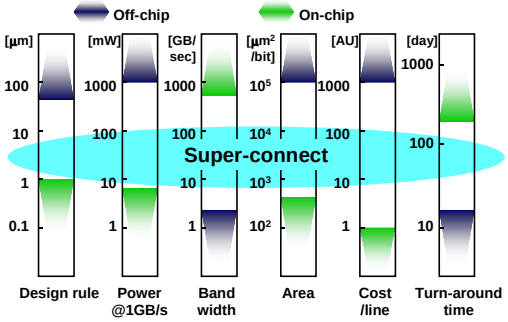
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

Super-connect

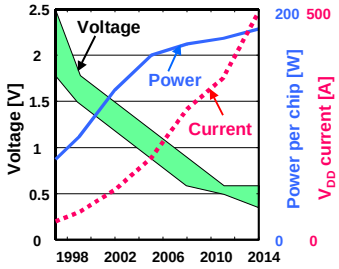


Nikkei microdevices

Super-connect



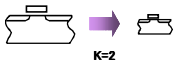
VDD, Power and Current Trend



International Technology Roadmap for Semiconductors 1998 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

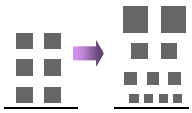
Scaling Law

Transistors		Scaling coefficients
V_{DD}	[V]	1/k
Tr. dimensions	[x]	1/k
Drain current	[I~1/x x/x V^1.3]	$1/k^{0.3}$
Gate capacitance	[C~1/x xx]	1/k
Tr. delay	[d~CV/I]	$1/k^{1.7}$
Tr. power	[P~VI~CVV/d]	$1/k^{1.3}$
Power density	**[p~P/x/x]**	$k^{0.7}$
Tr. density	**[n~1/x/x]**	k^2
Interconnects		
Type / Scaling scenario		**Local Scaled** / **Global Anti-scaled**
Line thickness	[T]	1/k / k
Width	[W]	1/k / k
Separation	[S]	1/k / k
Oxide thickness	[H]	1/k / 1
Length	[L]	1/k / 1
Resistance	[R_{INT}~L/W/T]	k / $1/k^2$
Capacitance	[C_{INT}~LW/H]	1/k / k
RC delay/Tr. delay	**[D~$R_{INT}C_{INT}$/d]**	$k^{1.7}$ / –
Current density	**[J~pWL/V /W/T]**	– / $k^{0.7}$
DC noise / V_{DD}	**[N~JWTR/V]**	– / $k^{1.7}$

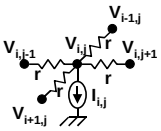


$$\alpha = 1.3$$

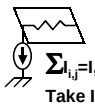
T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no.2, pp.584-594, Apr. 1990.



IR Drop

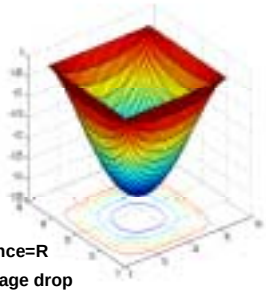


$$V_{i,j}=(V_{i-1,j}+V_{i+1,j}+V_{i,j-1}+V_{i,j+1})/4-r\,I_{i,j}$$



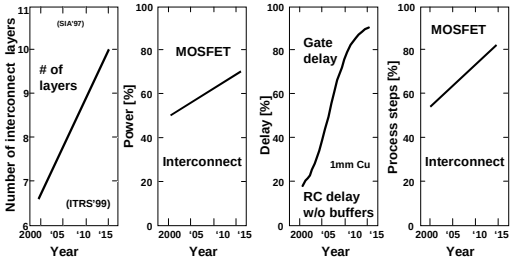
$\Sigma I_{i,j}=I$, Sheet resistance=R

Take IR as unity voltage drop



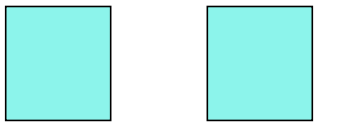
Interconnect determines cost & perf.

P: Power, D: Delay, A: Area, T:Turn-around

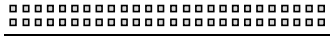


Interconnect Cross-Section and Noise

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply



Scaled interconnect
- Signal



1V 20W → 20A current
2% noise on VDD & VSS → ~0.02V / 20A → ~10μm thick Cu
Thick layer interconnect, area pad, package are co-designed.

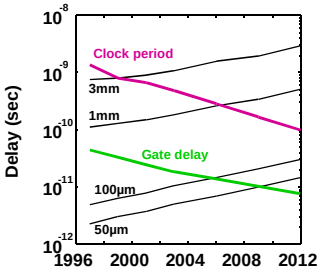
DSM interconnect design issues

Larger current
- IR drop (static and dynamic)
- Reliability (electro-migration)

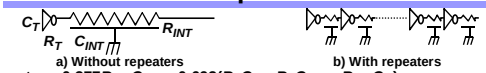
Smaller geometry / Denser pattern
- RC delay
- Signal Integrity
- Crosstalk noise
- Delay fluctuation

Higher speed
- Inductance
- EMI

RC delay and gate delay



Repeaters



a) Without repeaters b) With repeaters

$$t_{05} \approx 0.377R_{INT}C_{INT} + 0.693(R_TC_T + R_TC_{INT} + R_{INT}C_T)$$

C_0 :Gate capacitance of minimum MOSFET

R_0 :Gate effective resistance of minimum MOSFET

$$Delay \approx k\left[p_1\frac{R_{INT}}{k}\frac{C_{INT}}{k} + p_2\left(\frac{R_0}{h}hC_0 + \frac{R_0}{h}\frac{C_{INT}}{k} + \frac{R_{INT}}{k}hC_0\right)\right]: Buffered$$

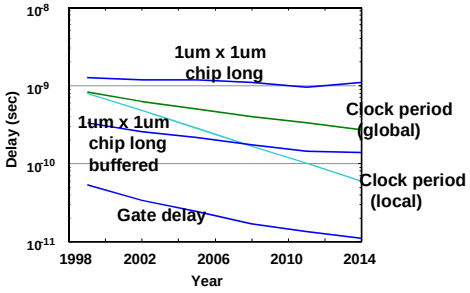
$$\frac{\partial Delay}{\partial h} = 0 \rightarrow h_{OPT} = \sqrt{\frac{C_{INT}R_0}{R_{INT}C_0}}: Optimized\ size\ of\ buffer\ inverter$$

$$\frac{\partial Delay}{\partial k} = 0 \rightarrow k_{OPT} = \sqrt{\frac{p_1}{p_2}}\sqrt{\frac{R_{INT}C_{INT}}{R_0C_0}}: Optimized\ number\ of\ stages$$

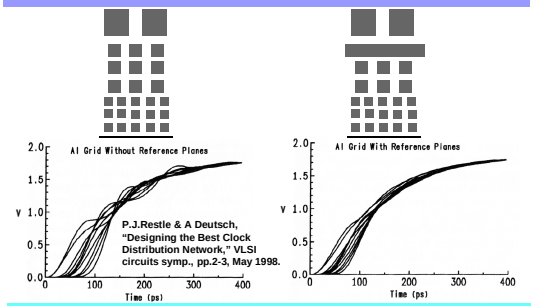
$$Delay_{OPT} = 2\left(\sqrt{p_1p_2} + p_2\right)\sqrt{R_{INT}C_{INT}R_0C_0} \approx 2.4\sqrt{\tau_{INT}\tau_{MOS}}$$

$$Cap.\ of\ gates = k_{OPT}h_{OPT}C_0 = \sqrt{p_1/p_2}C_{INT} = 0.73C_{INT}$$

Buffered interconnect delay

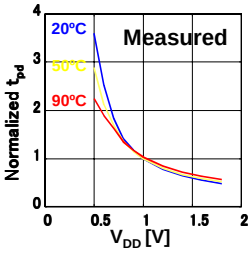


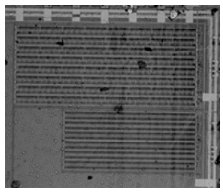
Inductive Effects in Clock Lines



Board design practice is imported in LSI.

0.5V LSIでの逆温度特性



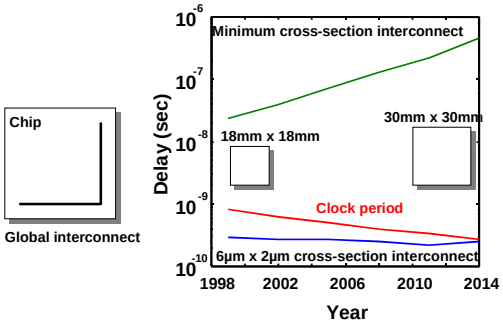


Photograph of 32bit FA

0.3µm CMOS

K.Kanda, K.Nose, H.Kawaguchi, and T.Sakurai,"Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's",CICC99, pp.563-566, May 1999.

RC delay of global interconnections



LSI in 2014

Year	Unit	1999	2014	Factor
Design rule	µm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (µP)		21M	3.6G	170
DRAM capacity		1G	1T	1000
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	µcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

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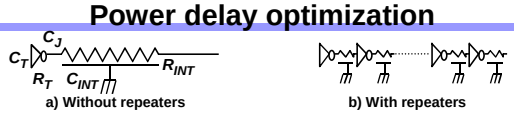
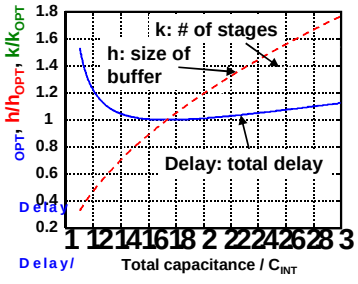
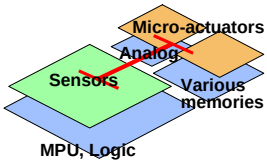
Power delay optimization



a) Without repeaters b) With repeaters



Possible electronic system in 2014



- Sensors/actutors
- 0.035µm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design for power lines, clocks, and long wires (super-connect)