Workshop on Advanced CMOS '01/10/31

Recent topics in realizing low-power, high-speed VLSI's

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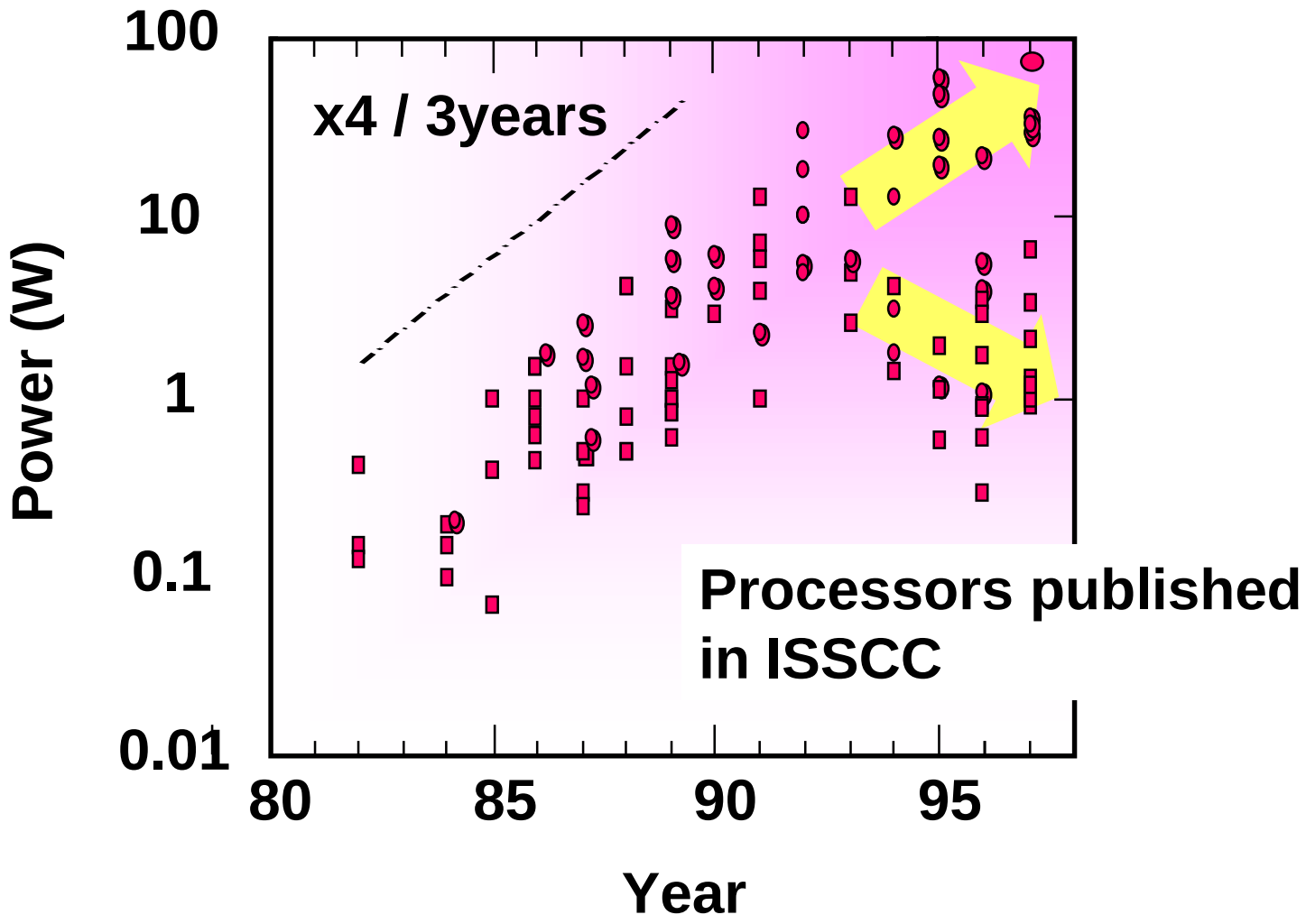
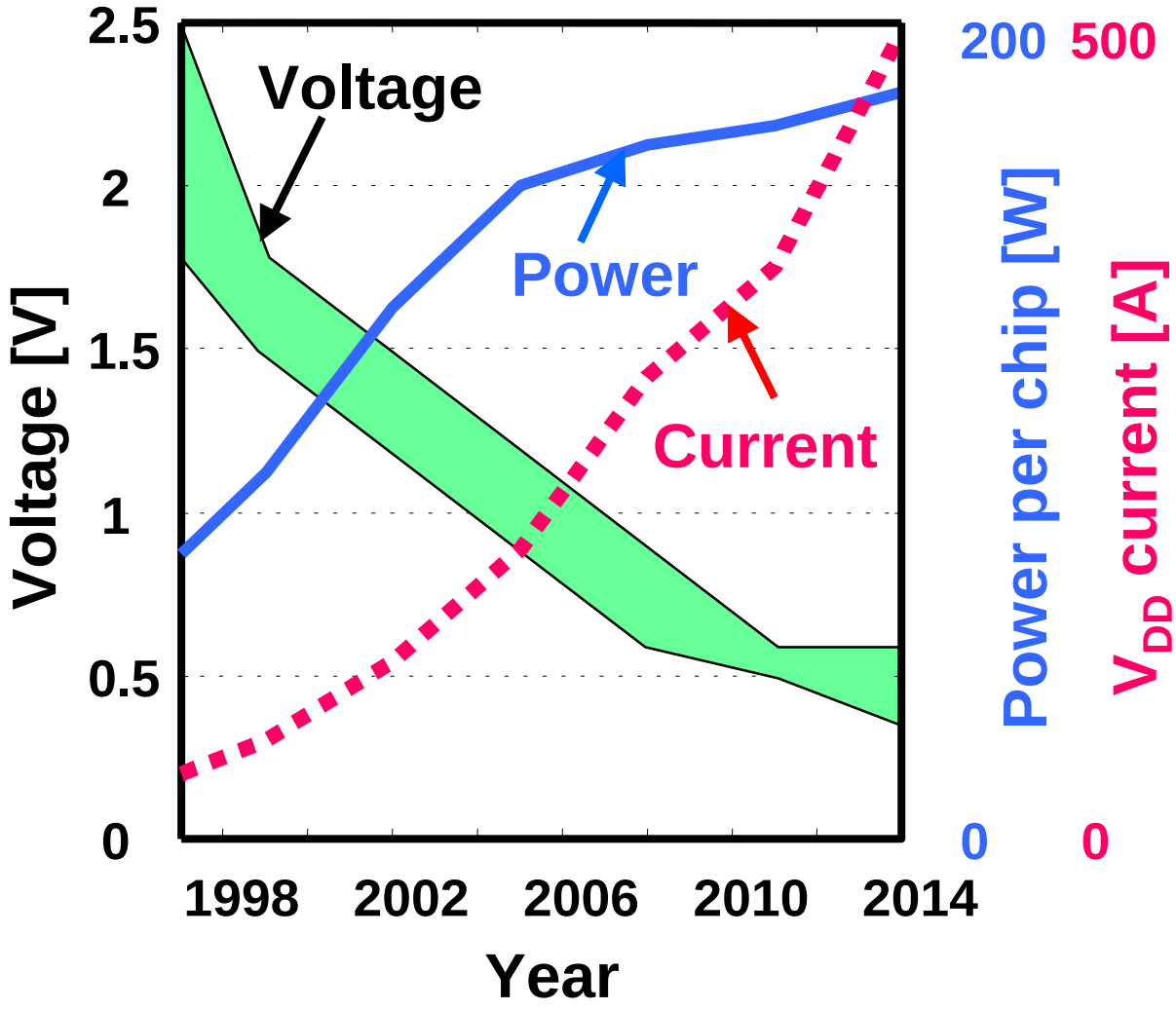
- **Multi-tox: Cooperation between technology and circuit**
- **VDD/VTH hopping: Cooperation between H/W & S/W**
- **Bus shuffling: Cooperation between circuit and CAD**

Ever Increasing VLSI Power



V_{DD}, power and current trend



International Technology Roadmap for Semiconductors 1999 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

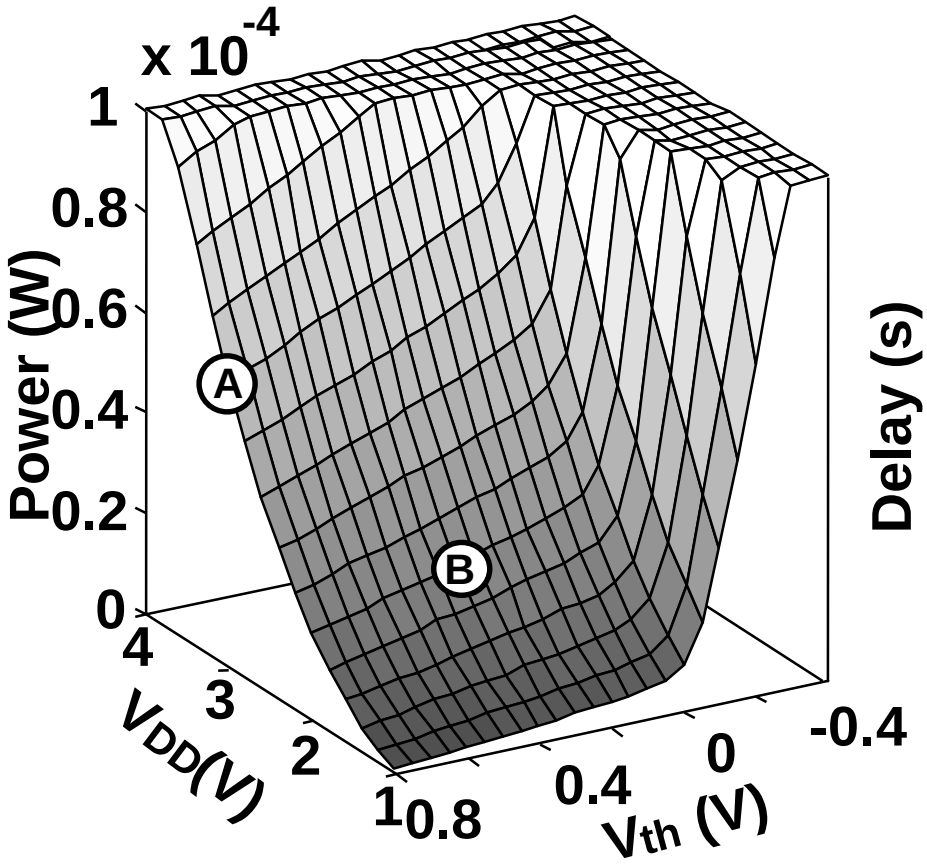
T.Sakurai

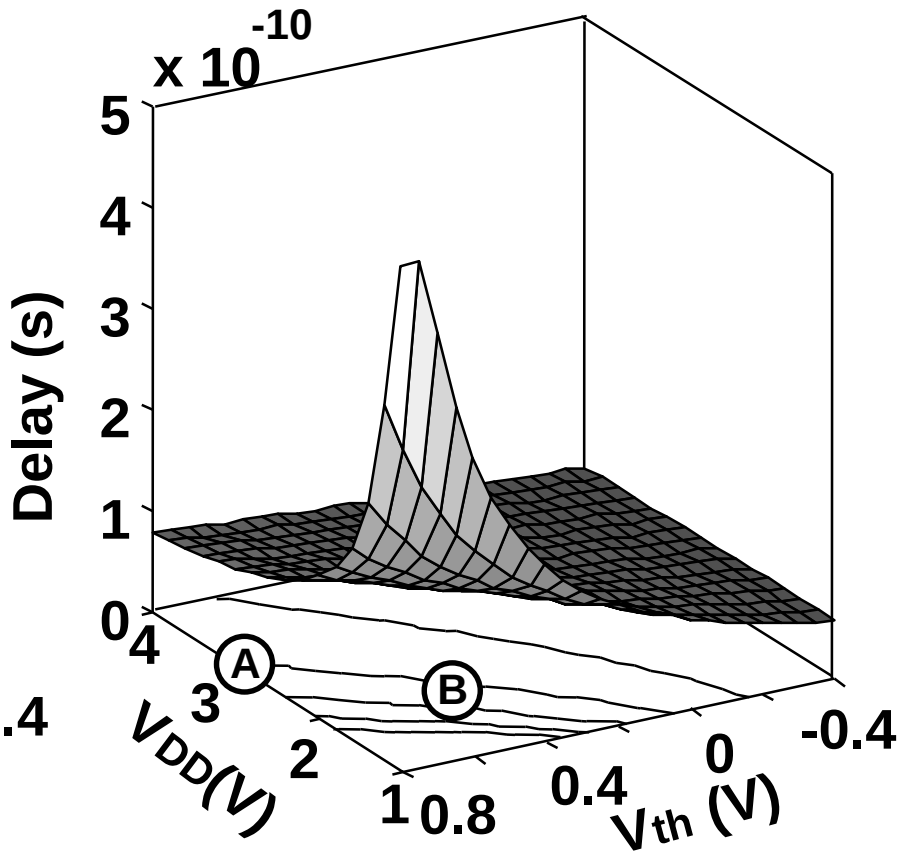
Power & Delay Dependence on V_{DD} & V_{TH}

$$Power = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD} + I_0 \cdot 10^{-\frac{V_{TH}}{S}} \cdot V_{DD} + Gate / Drain\ leak$$

$$Delay = \frac{k \cdot Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

(α=1.3)





Controlling V_{DD} and V_{TH} for low power

Low power → Low V_{DD} → Low speed → Low V_{TH} → High leakage → V_{DD}-V_{TH} control

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Software-hardware cooperation

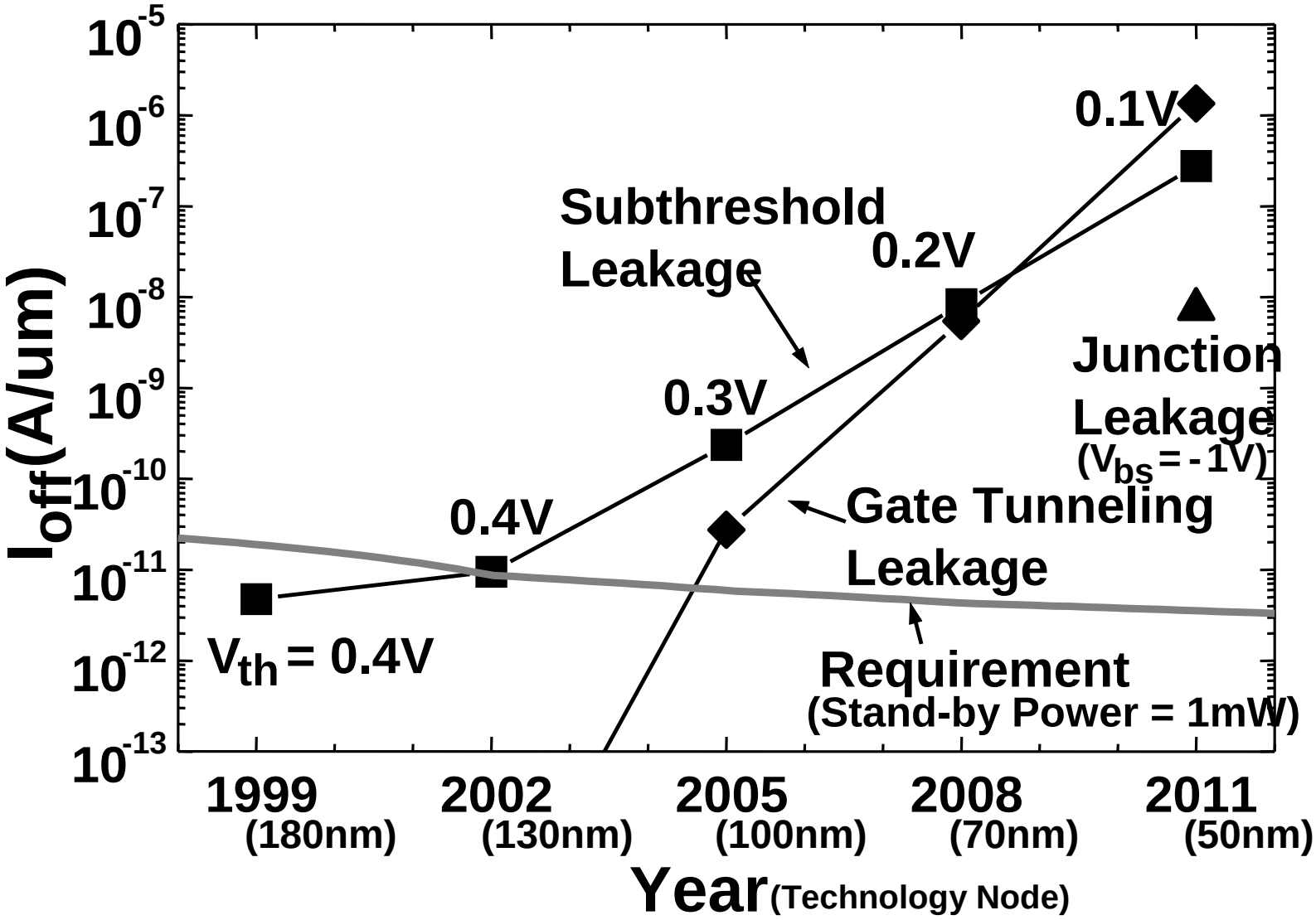
Technology-circuit cooperation

*) MTCMOS: Multi-Threshold CMOS

*) VTCMOS: Variable Threshold CMOS

- Multiple : spatial assignment
- Variable : temporal assignment

Transistors Go Leaky



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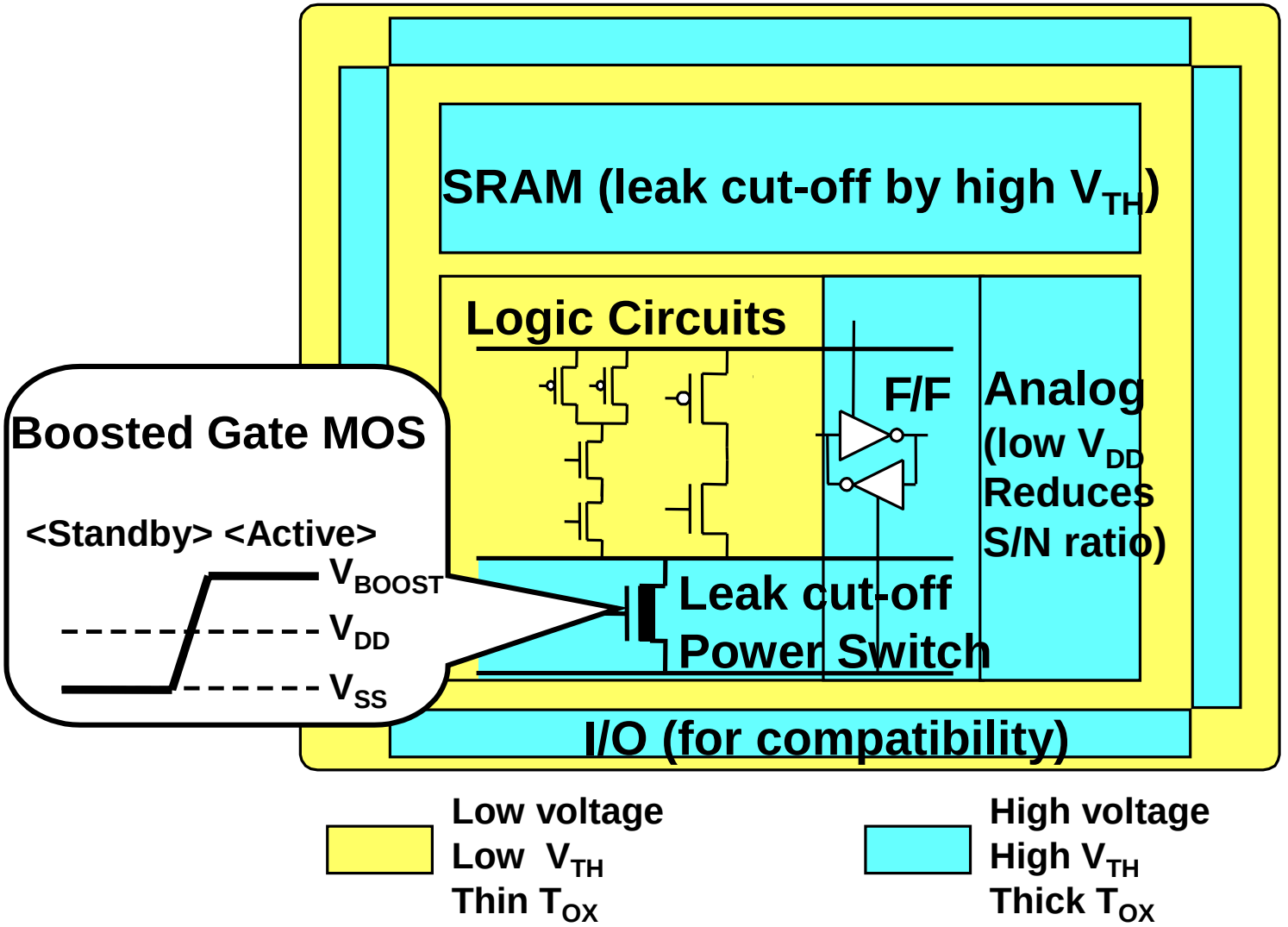
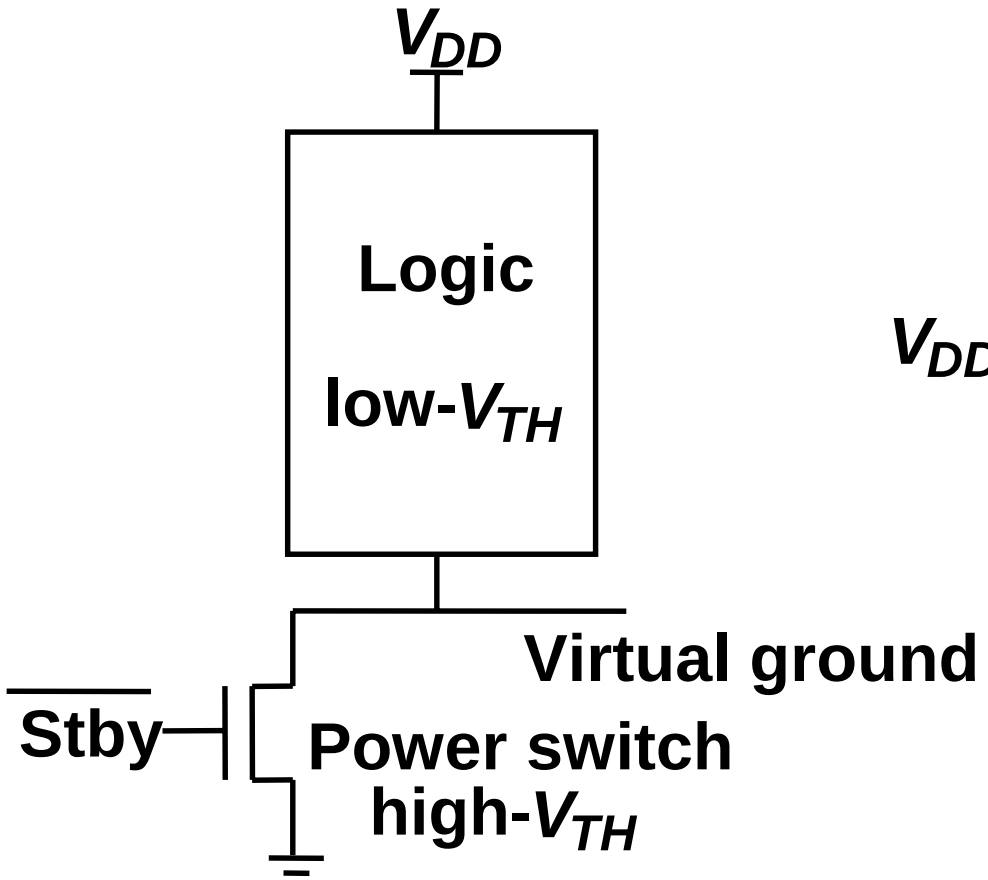
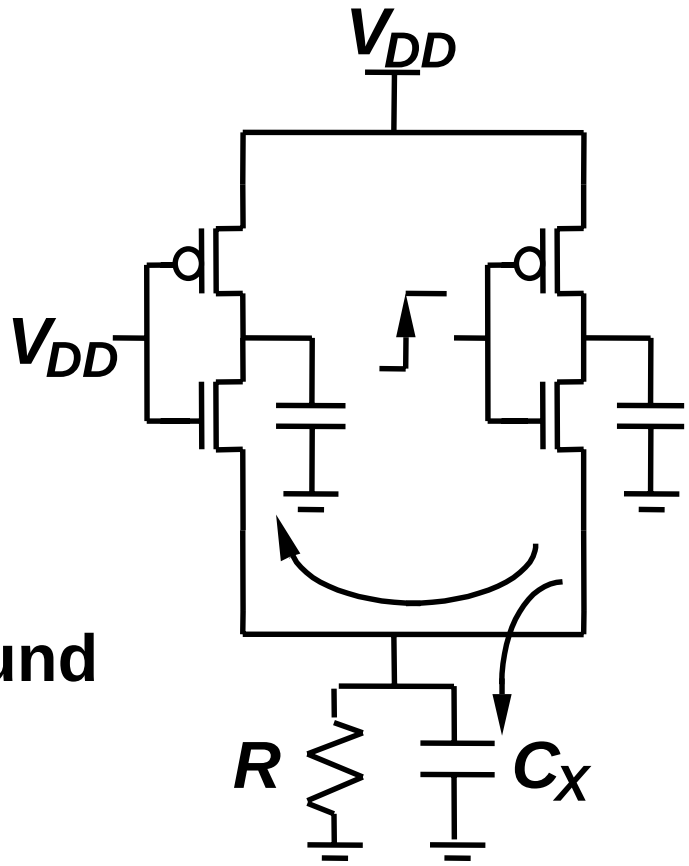
GSI's in Deep-Submicron Era



T.Inukai, M.Takamiya, K.Nose, H.Kawaguchi, T.Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC'00, p.409, May 2000.

Power Switch Gate Width in BGMOS





Kao, DAC'97, pp.409-414.

Degrade circuit speed unpredictably

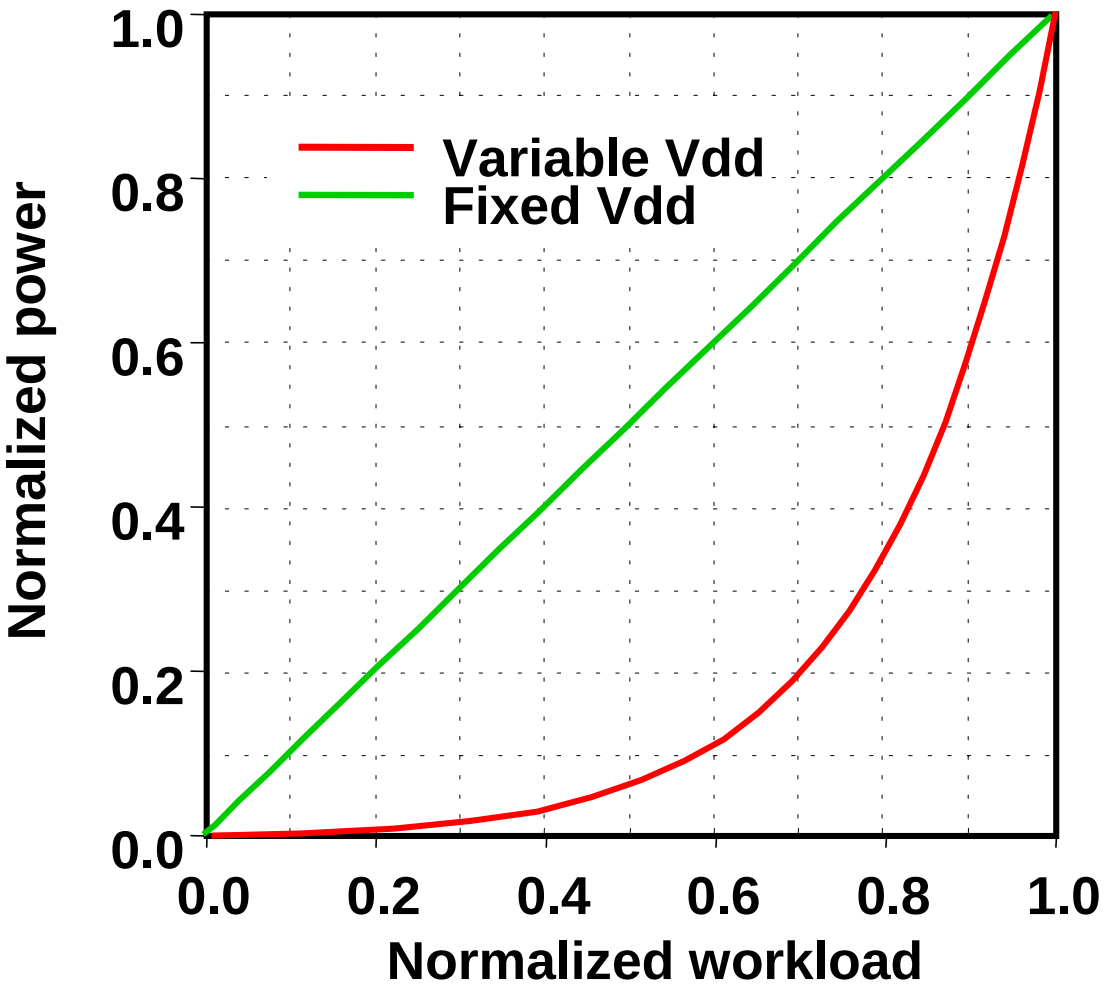
Controlling V_{DD} and V_{TH} for Low Power

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

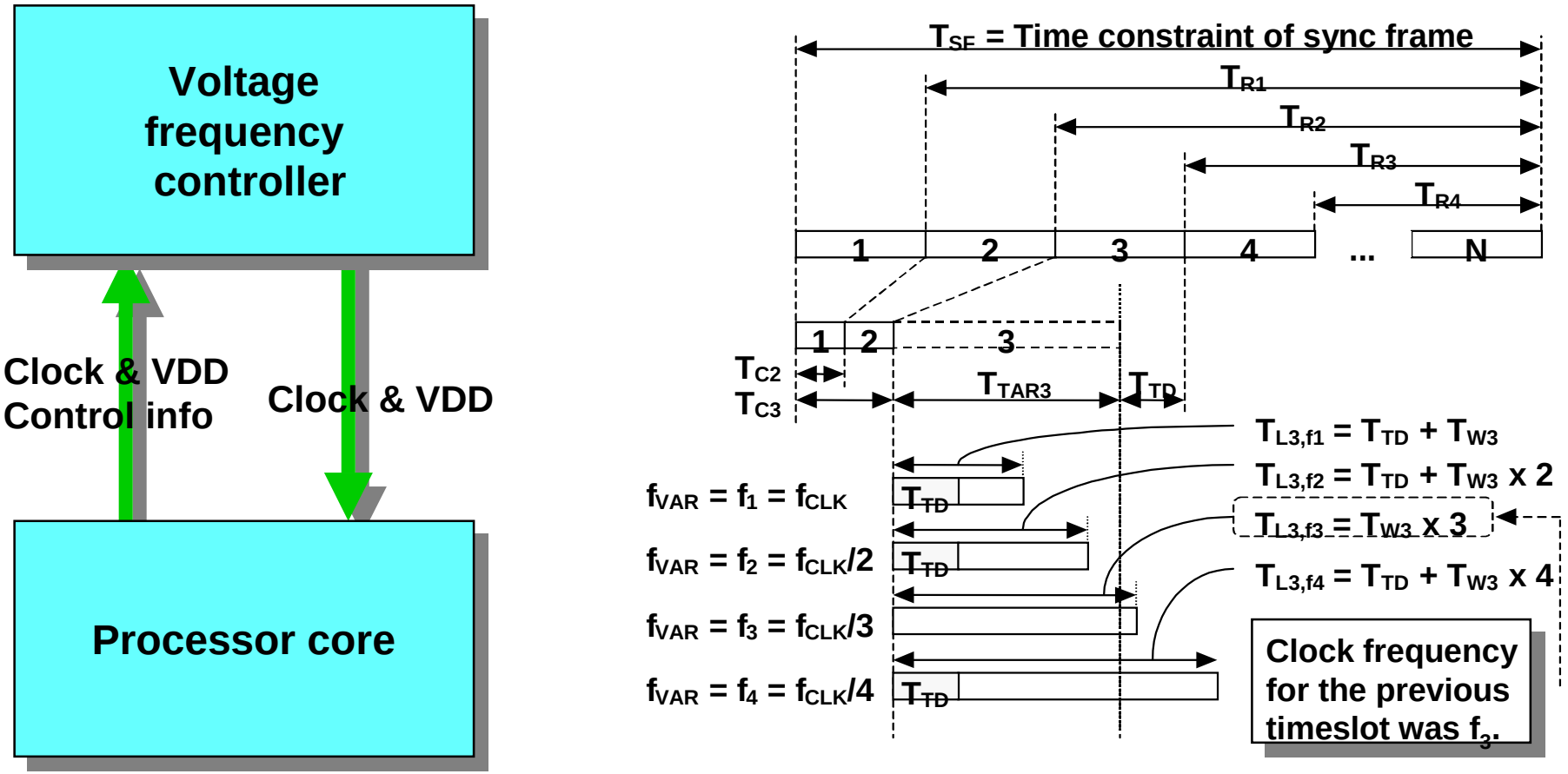
If you don't need to hussle, V_{DD} should be as low as possible

Power $\propto f V_{DD}^2 \sim f^3$

V_{DD} should be lowered to the minimum level which ensures the real-time operation.



Application Slicing and Software Feedback Loop in Voltage Hopping

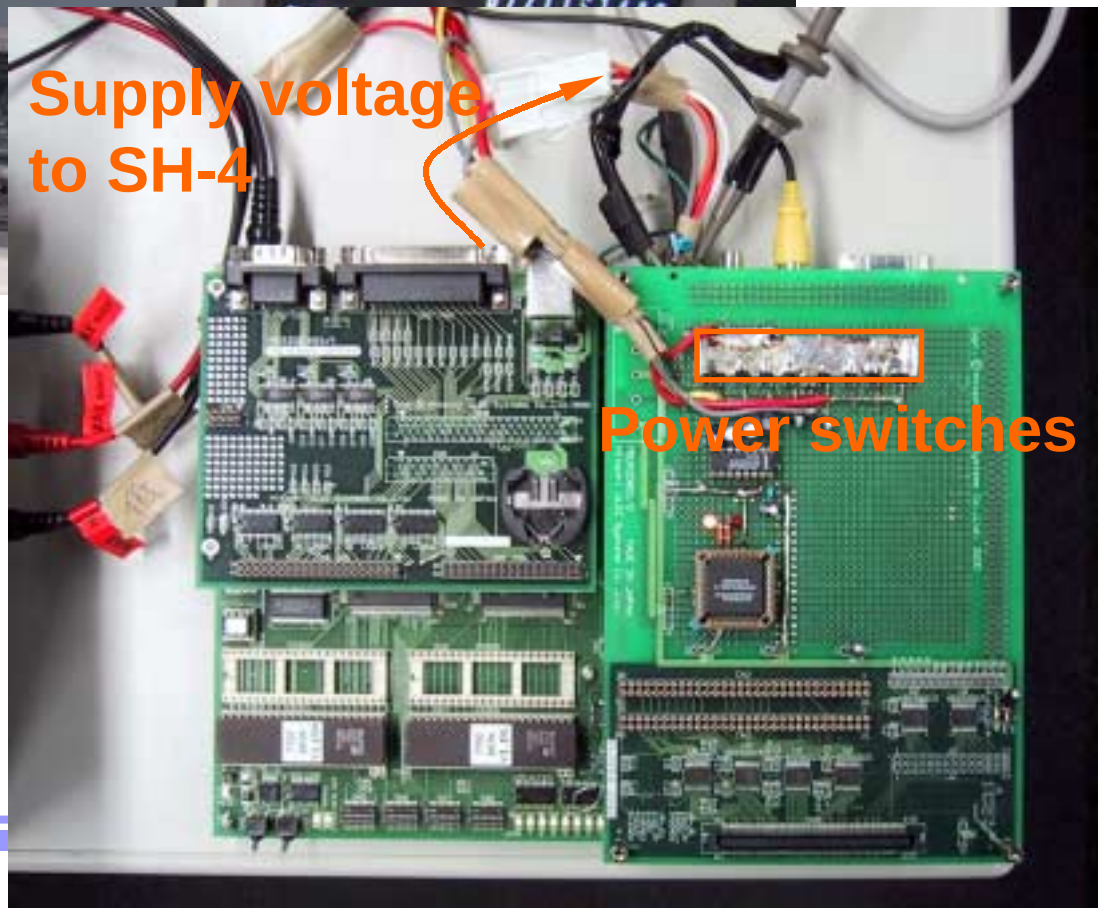


S.Lee and T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications,"ASPDAC'00, A5.2, pp.381~pp.386, Jan. 2000.

S.Lee and T.Sakurai, "Run-time Voltage Hopping for Low-power Real-time Systems," DAC'00, June 2000.

VDD-Hopping Hardware Snapshot

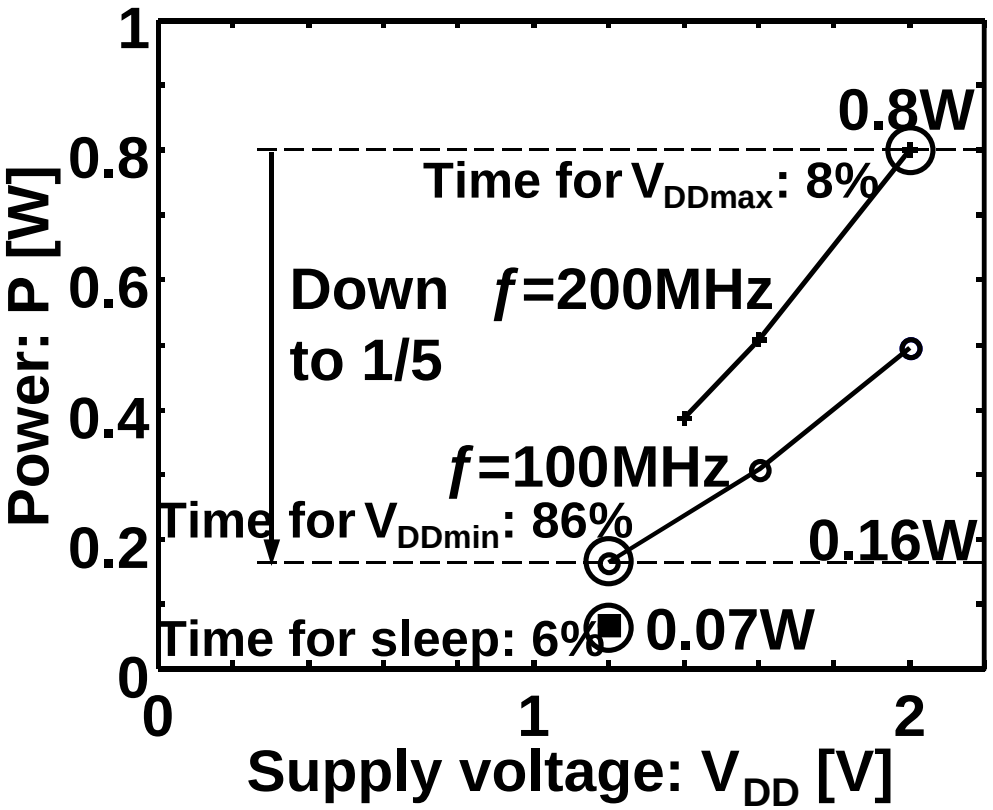
(A) System



(B) SH-4 embedded board

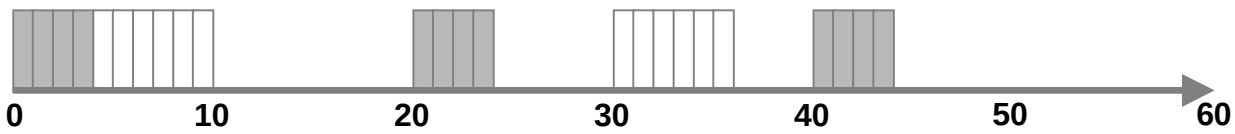
Measured Power Characteristics

Total power = 0.8 x 0.08 + 0.16 x 0.86 + 0.07 x 0.06 = 0.2W

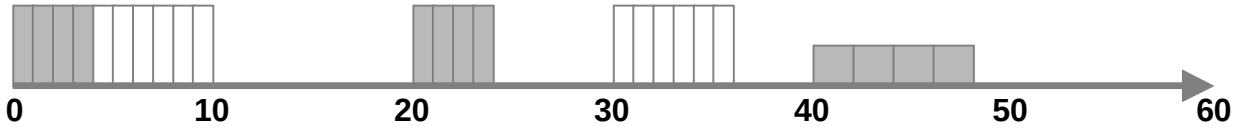


VDD hopping can cut down power consumption to 1/4

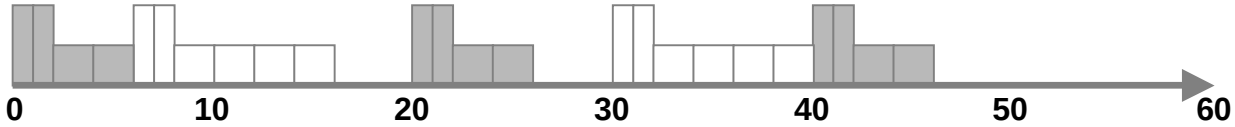
Power Conscious Operating System



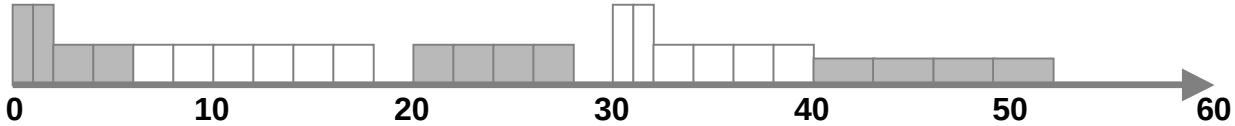
Conventional rate-monotonic scheduling (power consumption=1)



Speed control with power-conscious OS (power consumption=0.85)



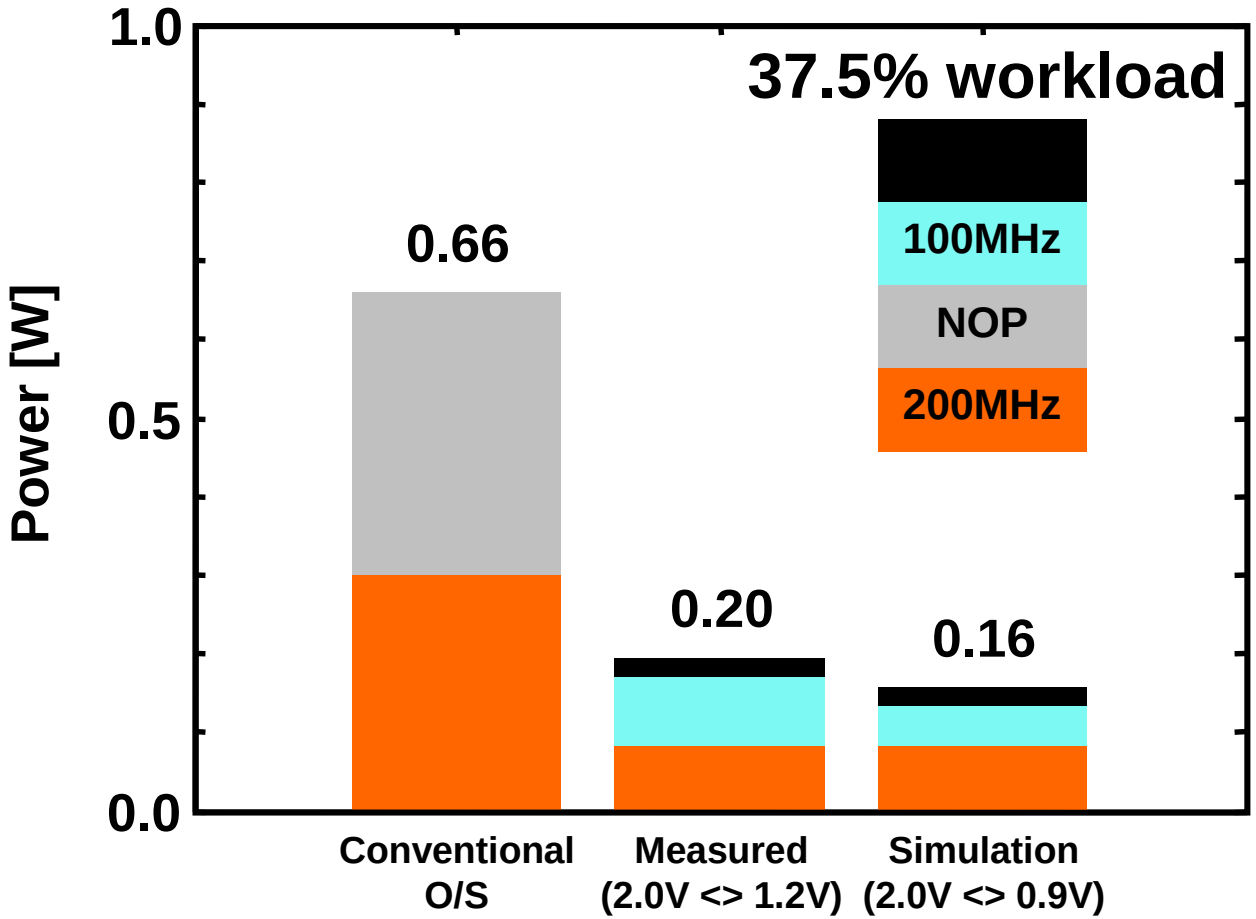
Speed control within application slices (power consumption=0.47)



Proposed scheduling: cooperation of OS and applications (power consumption=0.24)

Y.S.Shin, H.Kawaguchi, T.Sakurai, "Cooperative Voltage Scaling (CVS) between OS and Applications for Low-Power Real-Time Systems," CICC'01, pp.553-556, May 2001.

Power Comparison

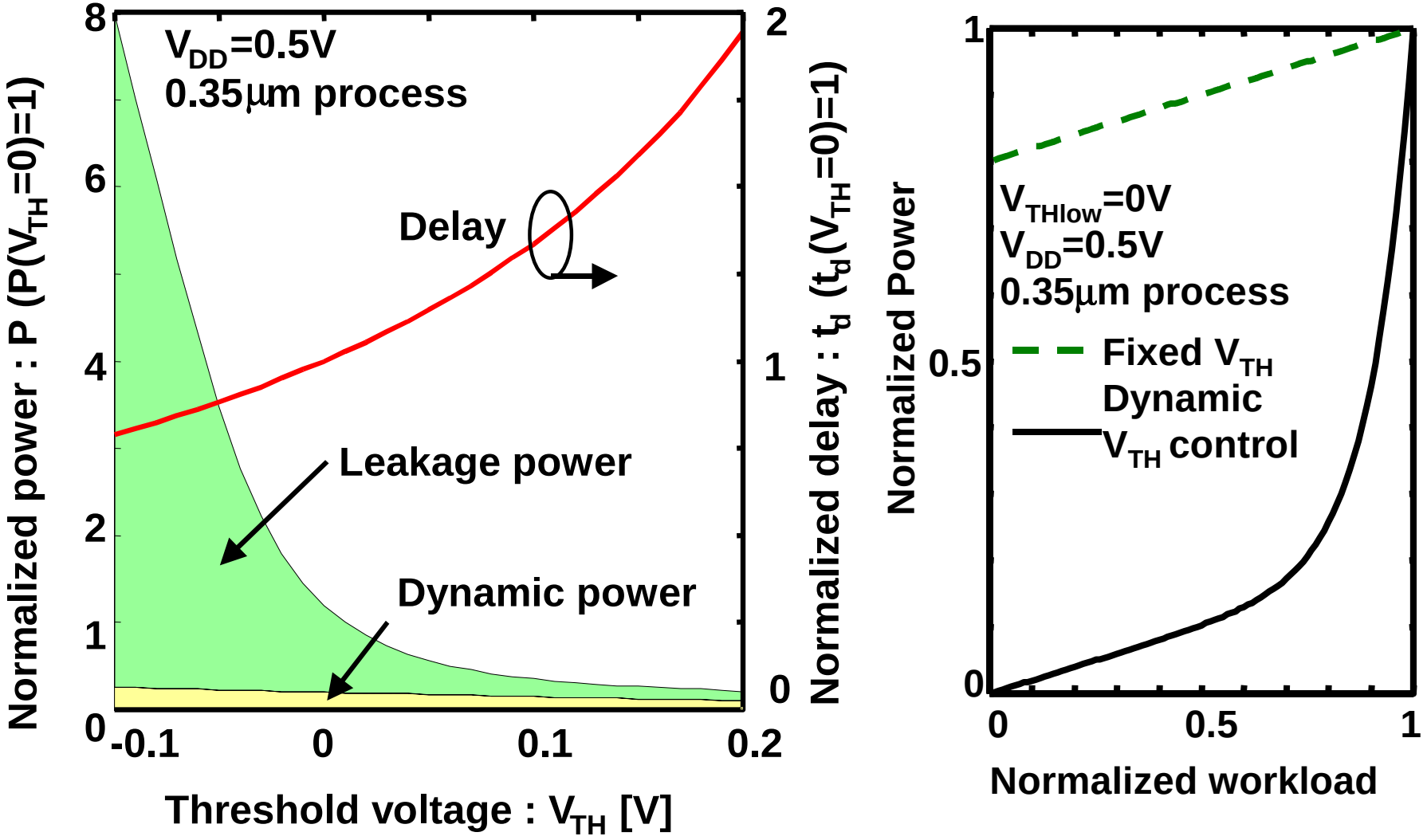


Controlling V_{DD} and V_{TH} for low power

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

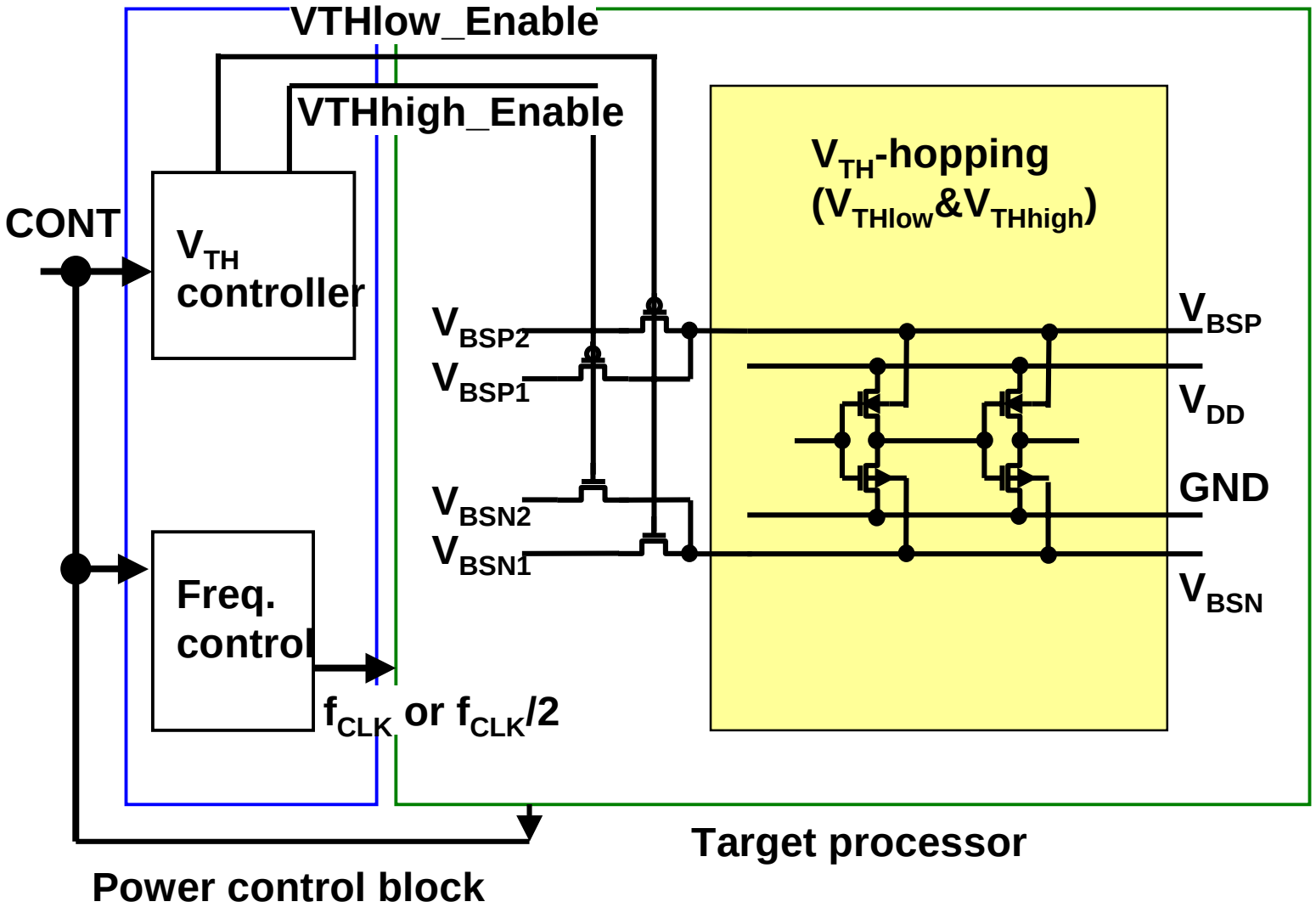
$$Power = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD} + I_0 \cdot 10^{-\frac{V_{TH}}{S}} \cdot V_{DD}$$

V_{TH}-Hopping

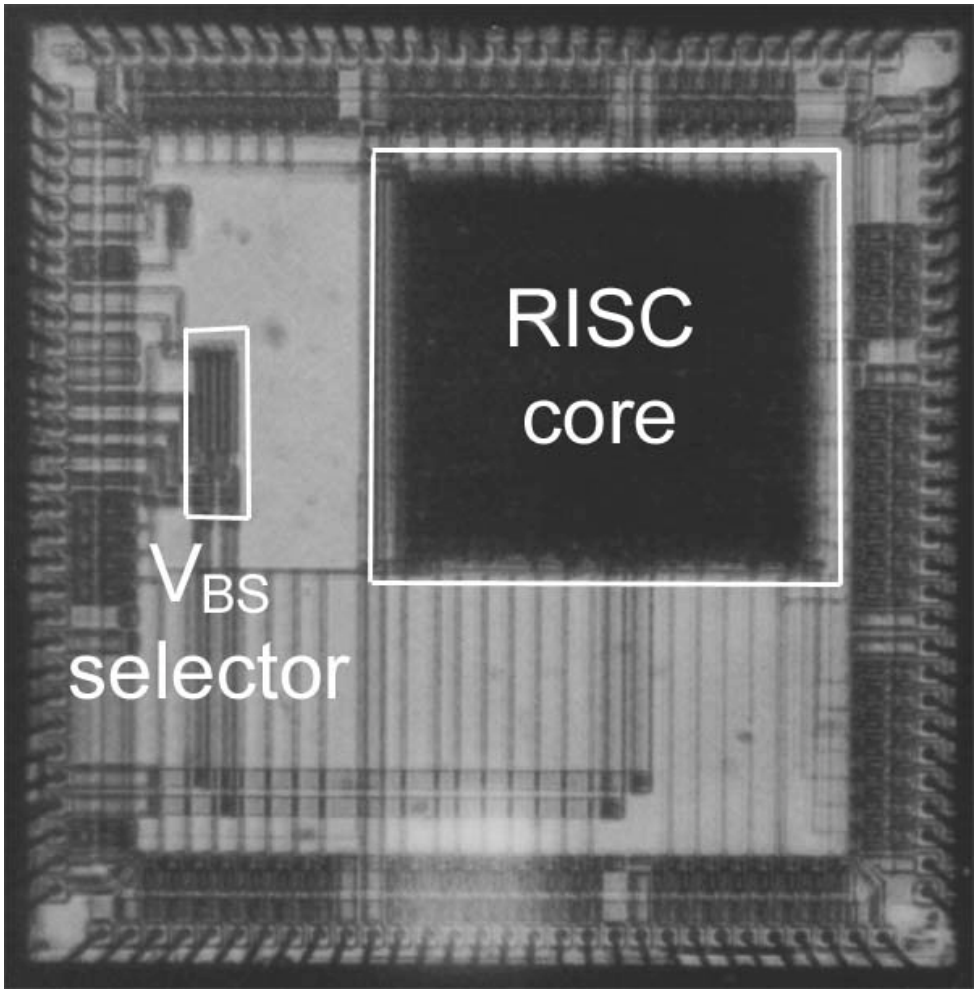


K. Nose, M.Hirabayashi, H.Kawaguchi, S.Lee and T.Sakurai, "VTH-hopping Scheme for 82% Power Saving in Low-voltage Processors," to be published, CICC 2001.

Schematic of V_{TH}-Hopping



Microphotograph of RISC Processor



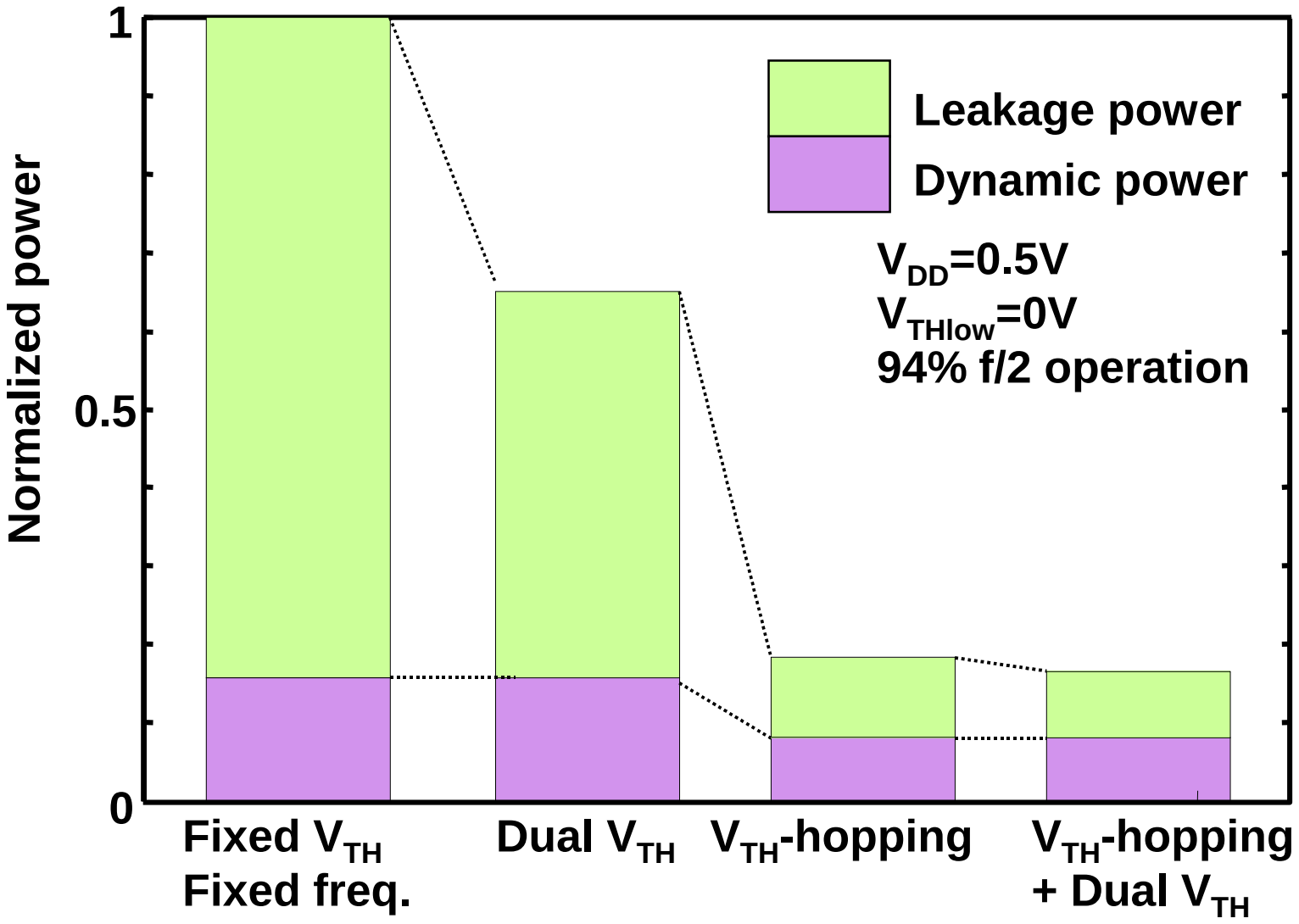
0.6μm process

Overhead of V_{TH}-hopping = 14%

RISC core = 2.1mm x 2.0mm

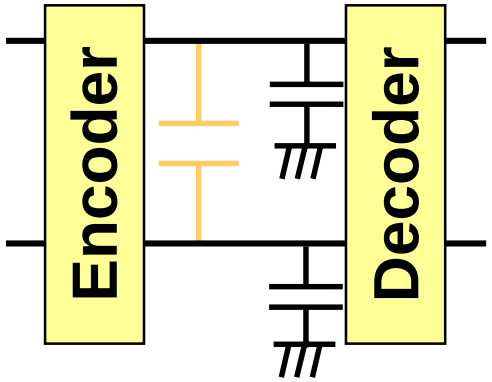
V_{BS} selector = 0.2mm x 0.6mm

Power Comparison

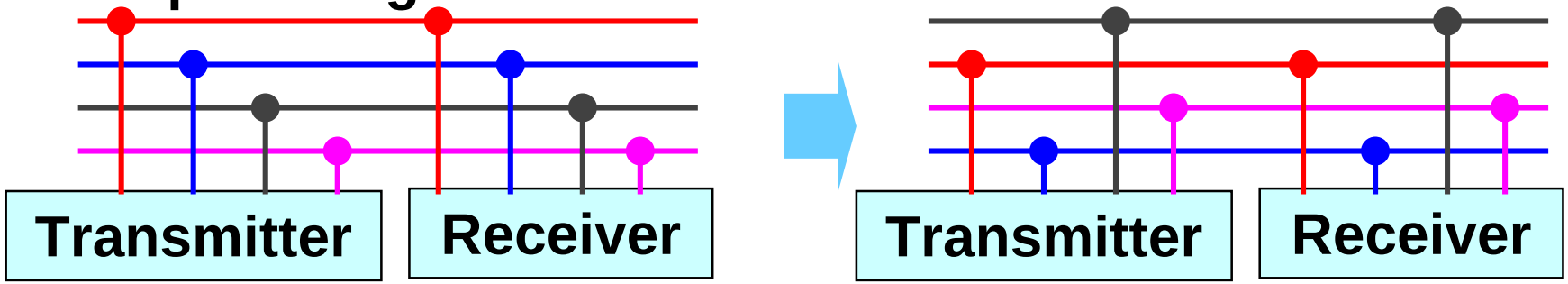


Bus Shuffling

- On-chip bus coding for low-power
  - Area, delay, power overhead for codec
  - No consideration on coupling cap.



- Bus shuffling
  - Shuffling bus so as to minimize power dissipation considering coupling capacitance.
  - Eventually no overhead
  - Requires signal statistical characteristics

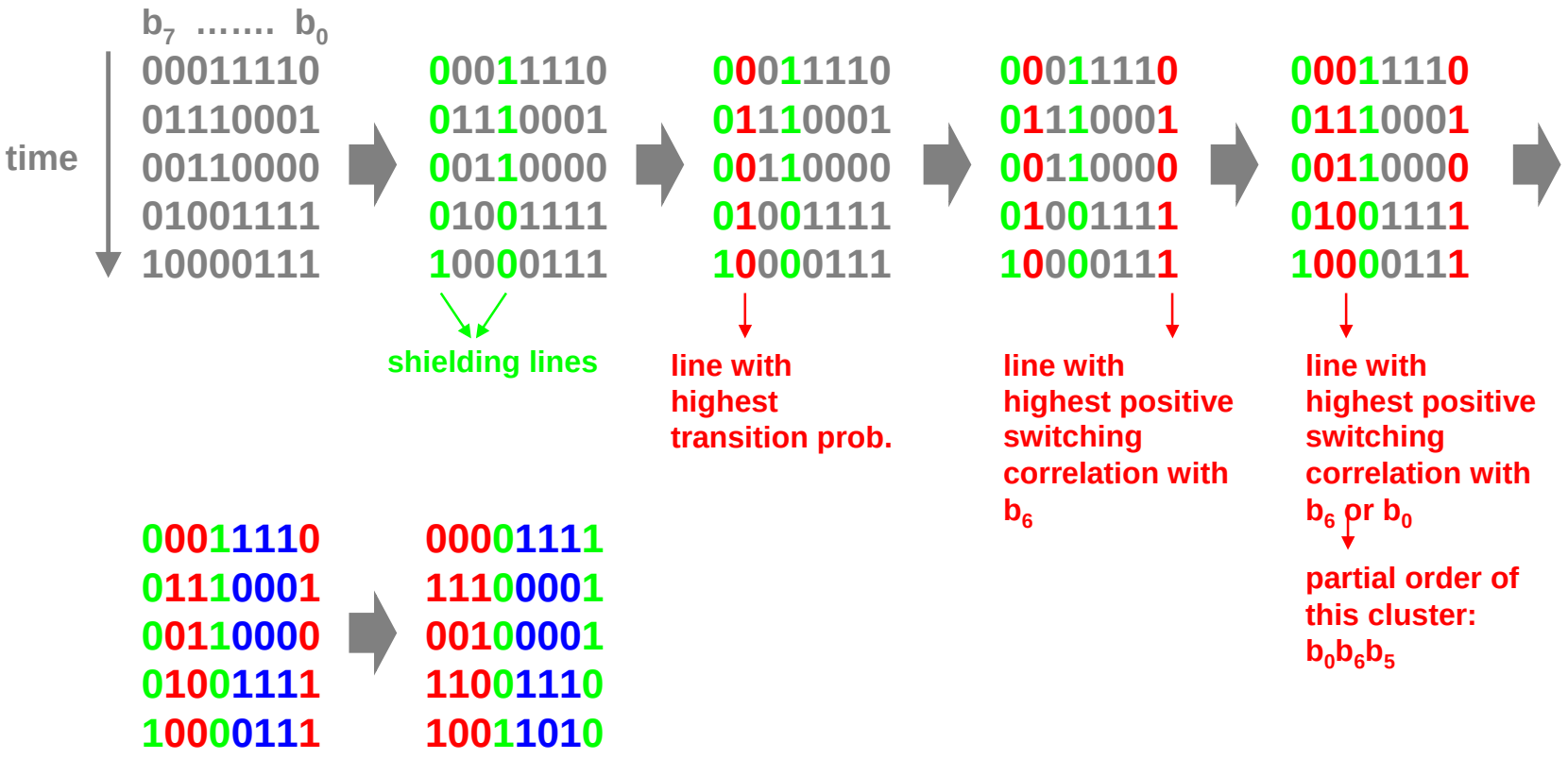


Normal layout　　Shuffled bus layout

Y. Shin and T. Sakurai, “Coupling-driven bus design for low-power application-specific systems,” Proc. Design Automation Conf. (DAC), pp.750-753, June 2001.

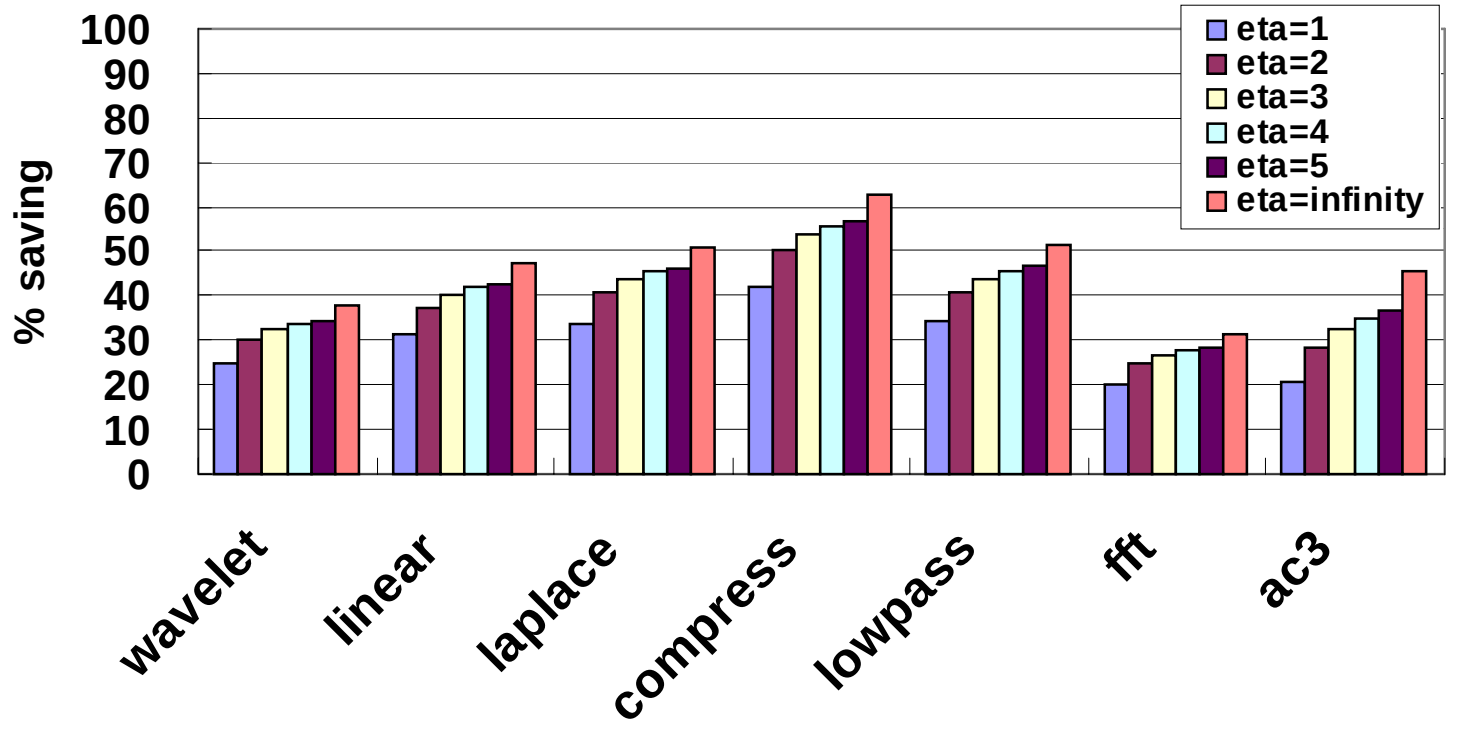
Bus Shuffling

- **Example**



Experiments

- Result of heuristic
  - 7 data address sets
  - About 40% power saving compared to un-shuffled buses



$\eta = \frac{\text{coupling cap.}}{\text{grounding cap.}}$

Summary

- **Multi-t_{OX} / Multi-V_{TH} is effective for achieving low power in standby mode.**

  : Cooperation between technology and circuit

  : Cooperation between circuit and CAD (needed)

- **V_{DD}-hopping and V_{TH}-hopping are effective for achieving low power in active mode.**

  : Cooperation between hardware and software

  : Cooperation between application and O/S

- **Bus shuffling is effective for bus interconnections**

  : Cooperation between circuit and CAD