Issues of Current LSI Technology and an Expectation for New System-Level Integration

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1. Abstract

Power, interconnection and complexity crises are stringent in designing future deeper submicron LSI's. A new system-level integration using superconnect technology may solve some of the issues related to the current LSI technology. The system-level integration may also open up new application area.

2. Scaling and Issues of Current LSI Technology

Taking a close look at the scaling law as in Fig.1, we can see that the following three crises are leaning over the LSI technology.

- Power crisis
- Interconnection crisis
- Complexity crisis

The power crisis is depicted in Fig.2. Lower operation voltage naturally increases operation current, which in turn requires thicker metal layers for the current to be distributed throughout the chip without IR-drop. One of the key approaches to low-power design is the memory embedding. By embedding memories, inter-chip communication power can be reduced by two orders of magnitude. The memory embedding, however, is an expensive option, since it increases process steps. A new system-level integration can be a solution to this problem.

As for the interconnection crisis, RC delay increase and IR-drop issue are some of the more stringent issues. Thicker metal layer used in an interposer/package/board may mitigate the problem.

Complexity crisis can only be solved by re-use of the pre-designed blocks and designing at higher abstraction level. Thus, System-on-a-Chip (SoC) where many pre-designed IP's are amalgamated at the higher abstraction is one of the candidates to cope with the complexity crisis. Future electronic systems, however, cannot be built only with the SoC, since many SoC issues have become evident as follows.

- Huge initial investment for masks & development
- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

The huge investment in developing the SoC process to embed different kinds of technologies is one of the most vital issues.

3. System-Level Integration

Recently, however, a new system-level integration called 'superconnect' is attracting attention[1-4], which may solve SoC problems. The superconnect connects separately built and tested chips not by printed circuit boards but rather directly to construct high-performance yet low-cost electronic systems as shown in Fig.4. The superconnect may use around 10 micron level design rules as shown in Fig.5 [4]. Sometimes LSI's in the superconnect are connected in three-dimensional fashion to achieve the higher performance and the smaller geometry. System-in-a-Package (SiP) composed of stacked chips using bonding or interposers as shown in Fig.6 is one realization of the superconnect. The superconnect mitigate IR-drop problems and RC delay problems.

There has been a large gap between on-chip and off-chip interconnects in terms of power, density, performance, cost and turn-around-time as shown in Fig.4. Basically, the large gap comes from the big difference between the design rules of on-chip and off-chip interconnects as shown in Fig.7. It can be said that there is a technology vacuum at present between 1μm level on-chip interconnect and 100μm level off-chip interconnect. The superconnect will fill the gap between on-chip and off-chip interconnect, making use of 10μm level design rule.

Some of the important issues in the future system-level integration are as follows.

- Special design tools for placement & route for co-design of LSI's and assembly
- High-density reliable substrate and metallization technology

(see the other side)

- low-cost, available known good die (reworkablility and module testing)

References

[1] T.Sakurai, "Superconnect Technology," Trans. C of IEICE, May 2001.

[2] M.Koyanagi et al., “Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology,” ISSCC Digest of Tech. Papers, pp.270-271, Feb.2001.

[3] K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, “3-D Assembly Interposer Technology for Next-Generation Integrated Systems,” ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

[4] M.Kimura, "Superconnect: 21st Century LSI Production and Design Method", Nikkei Microdevices, no.180, pp.62-79, June 2000.

Transistors		Scaling coefficients
V_{DD}	[V]	1/k
Tr. dimensions	[x]	1/k
Tr. current	[I~1/x x/x V^1.3]	$1/k^{0.3}$
Tr. capacitance	[C~1/x xx]	1/k
Tr. delay	[d~CV/I]	$1/k^{1.7}$
Tr. power	[P~VI~CVV/d]	$1/k^{1.3}$
Power density	**[p~P/x/x]**	$k^{0.7}$
Tr. density	**[n~1/x/x]**	k^2
Interconnections		
Type / Scaling scenario		**Local Scaled** / **Global Anti-scaled**
Line thickness	[T]	1/k / k
Width	[W]	1/k / k
Separation	[S]	1/k / k
Oxide thickness	[H]	1/k / 1
Length	[L]	1/k / 1
Resistance	[Rint~L/W/T]	k / $1/k^2$
Capacitance	[Cint~LW/H]	1/k / k
RC delay/Tr. delay	**[D~RintCint/d]**	$k^{1.7}$ / –
Current density	**[J~pWL/V /W/T]**	– / $k^{0.7}$
DC noise / Vdd	**[N~JWTR/V]**	– / $k^{1.7}$

$$I_{DS} = \frac{\mu\varepsilon}{2t_{ox}}\frac{W}{L}(V_{GS}-V_{TH})^{\alpha} \approx [1/x \times x/xV^{1.3}]$$

T.Sakurai&A.Newton,"Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas",IEEE JSSC, vol25, no.2, pp.584-594, Apr. 1990.

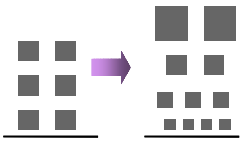


Fig.1 Scaling law

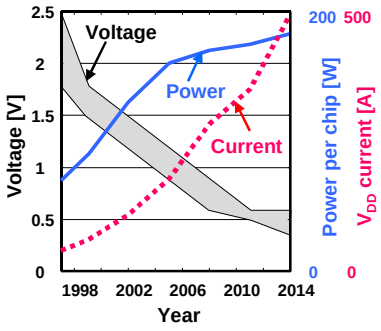


Fig.2 Trend in power and current increase

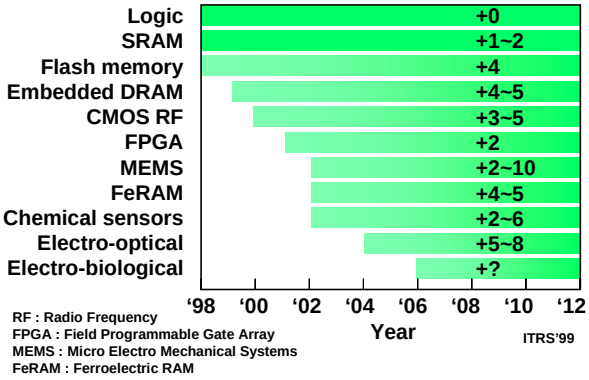
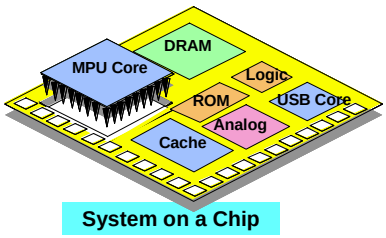


Fig.3 Mask increase by SoC



- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via
- Heat dissipation is an issue

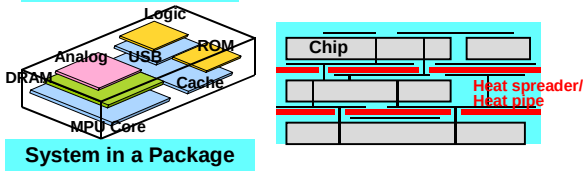


Fig.4 SoC and SiP

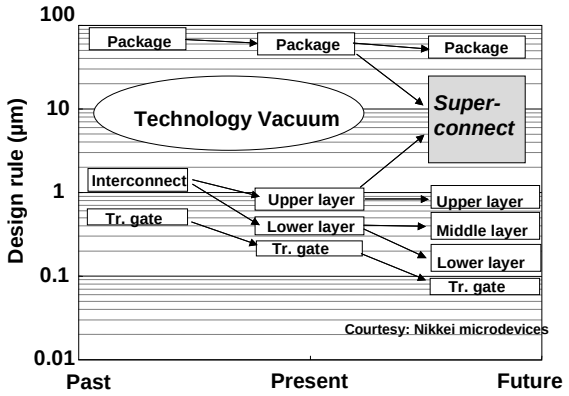


Fig.5 Technology vacuum around 10um level

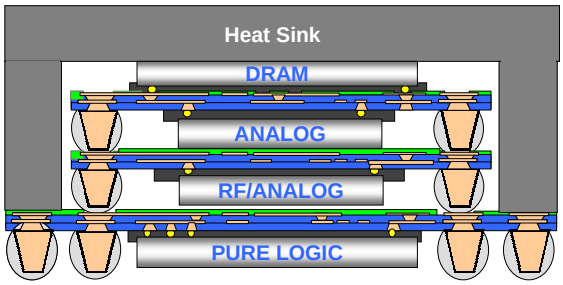


Fig.6 An example of SiP using interposers [3]

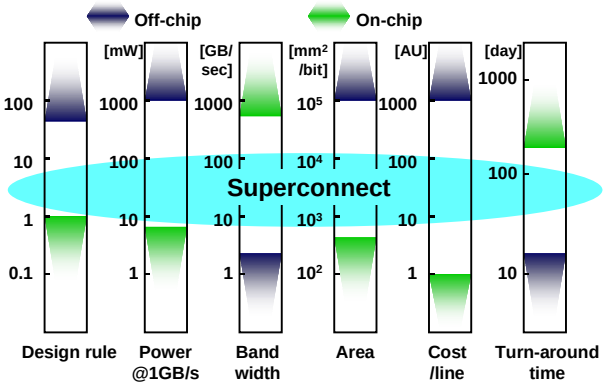


Fig.7 Performance gap between present on-chip and off-chip connection