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# Issues of Current LSI Technology and Expectation for New System-Level Integration

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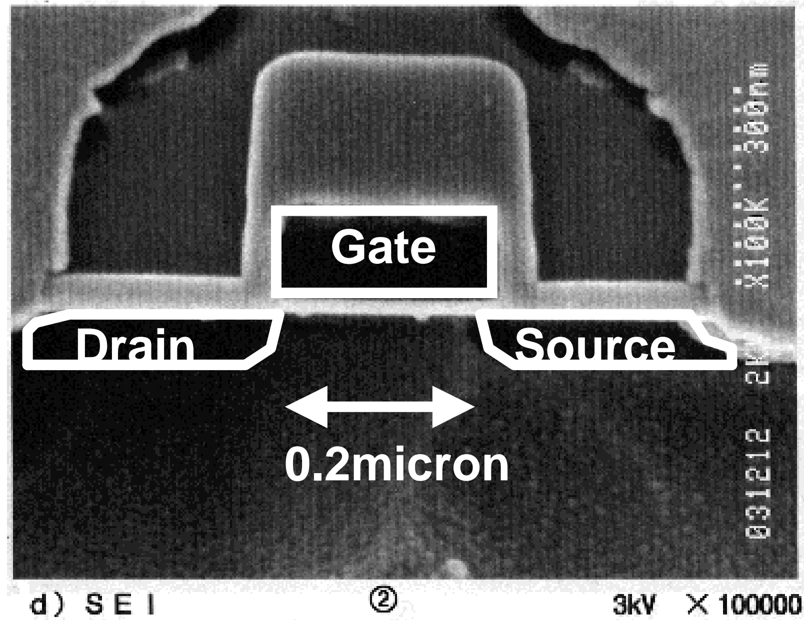
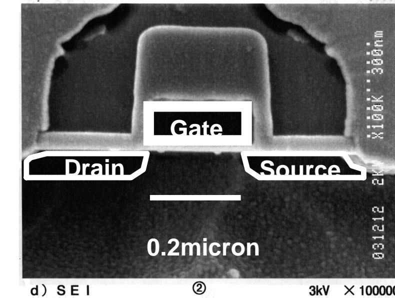
- **Issues in LSI designs**
- **Issues in System-on-a-Chip**
- **New system level integration**

# Scaling Law




Size 1/2




**Favorable effects**

| | |
|---|---|
| Size | x1/2 |
| Voltage | x1/2 |
| Electric Field | x1 |
| Speed | x3 |
| Cost | x1/4 |

**Unfavorable effects**

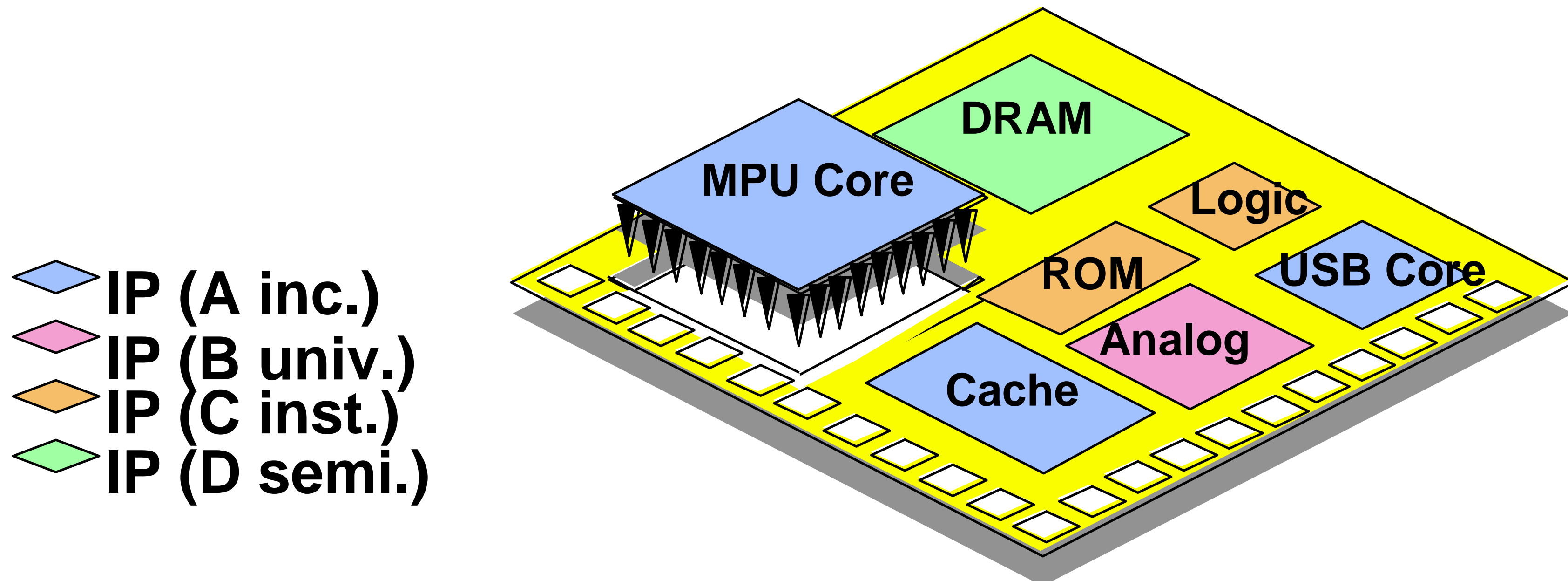
| | |
|---|---|
| Power density | x1.6 |
| RC delay/Tr. delay | x3.2 |
| Current density | x1.6 |
| Voltage noise | x3.2 |
| Design complexity | x4 |

# Three major crises in VLSI designs

- Power crisis
- Interconnection crisis
- Complexity crisis

# System-on-a-Chip (SoC)

- Re-use and sharing of design
- Design in higher abstraction

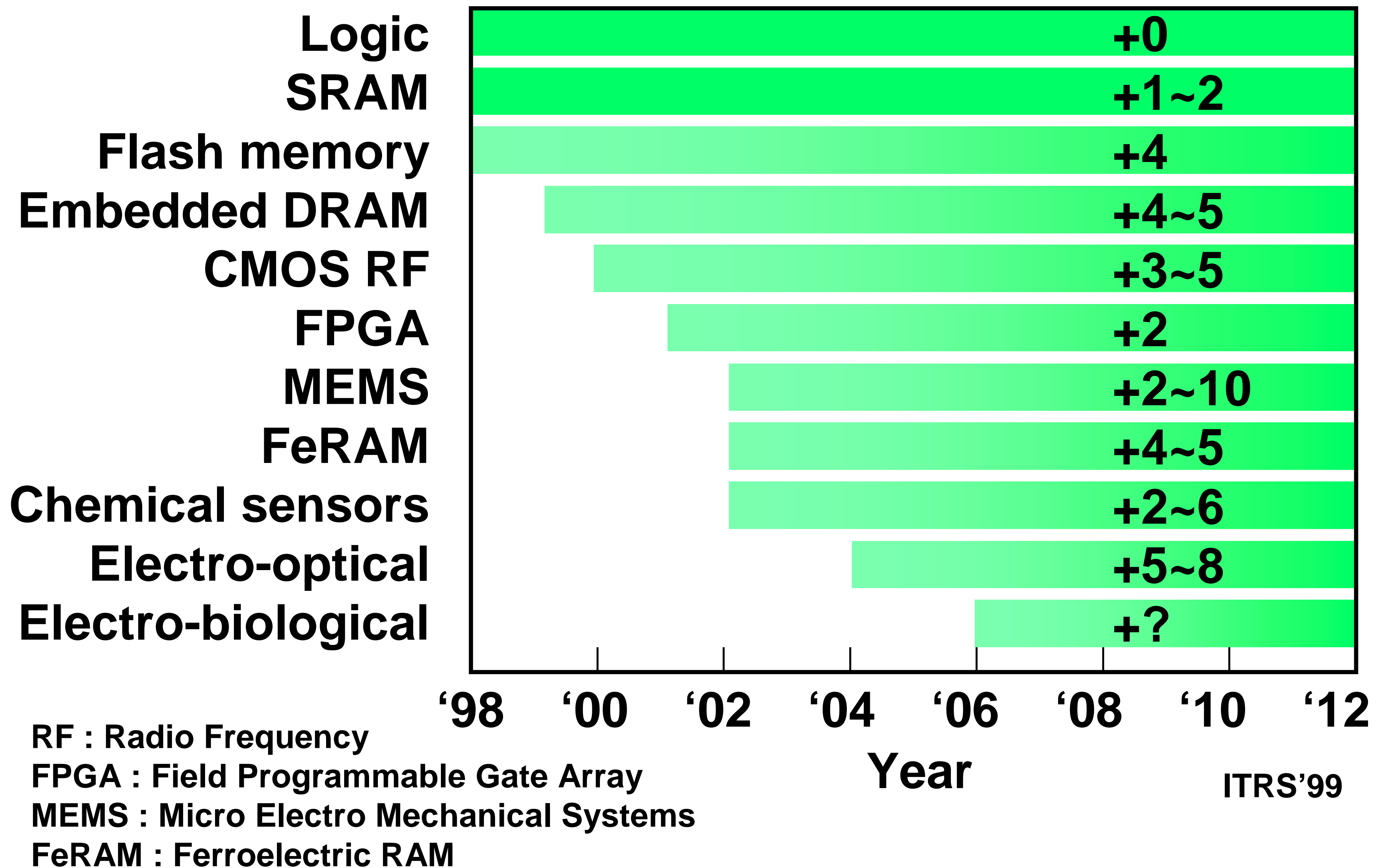



IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

# Issues in System-on-a-Chip

- Un-distributed IP's (i.e. CPU, DSP of a certain company)
- Low yield due to larger die size
- Huge initial investment for masks & development
- IP testability, upfront IP test cost
- Process-dependent memory IP's
- Difficulty in high precision analog IP's due to noise
- Process incompatibility with non-Si materials and/or MEMS

# Technologies integrated on a chip



# New system level integration

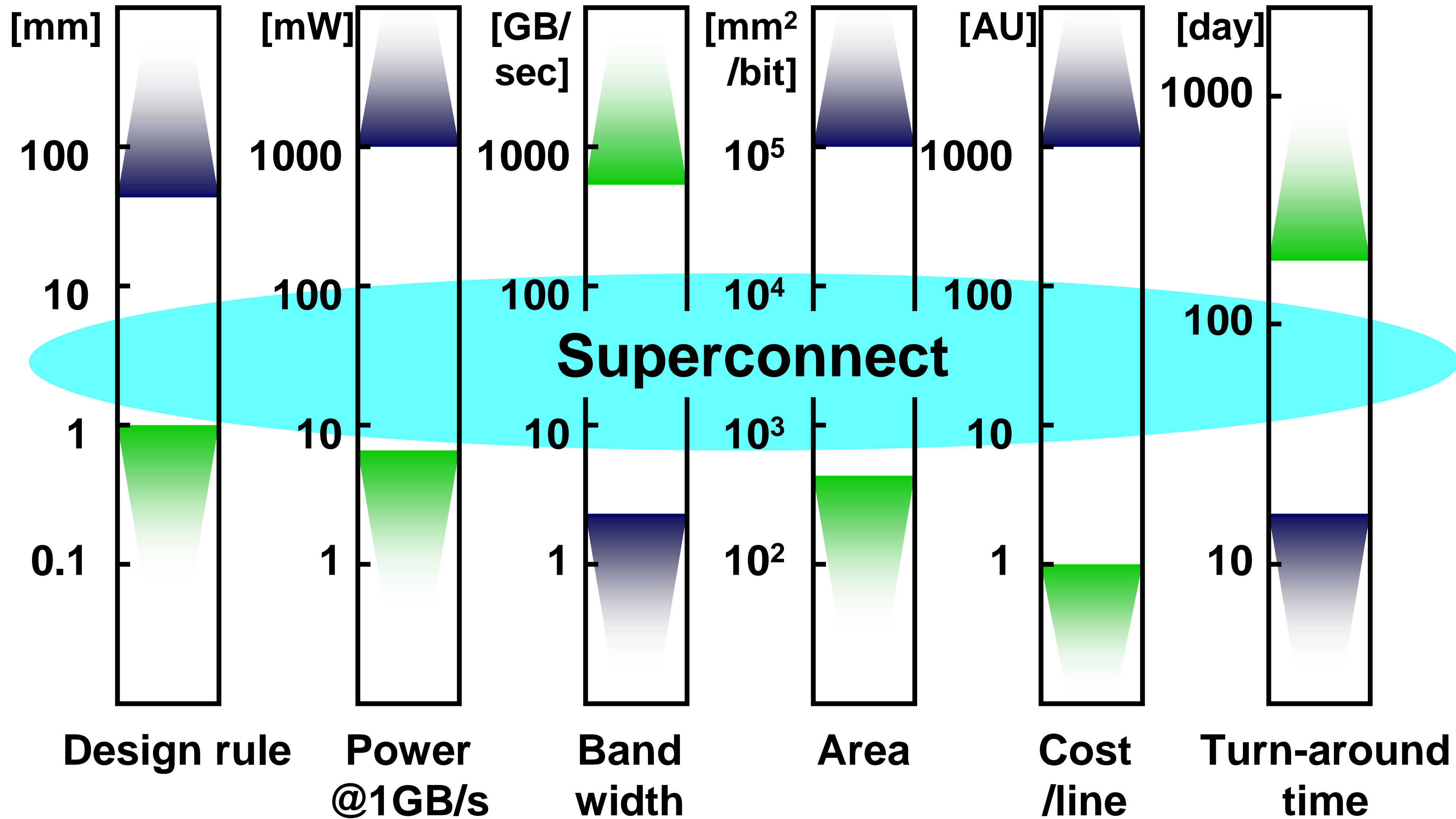
- SoC : High-performance but issues remain
- Printed circuit board (PCB) : Low-performance

- New system level integration : Superconnect

  - Connects separately built and tested chips not by the PCB but rather directly to construct high-performance yet low-cost electronic systems

  - May use around 10 micron level design rules

# Large performance gap between on-chip and off-chip interconnect

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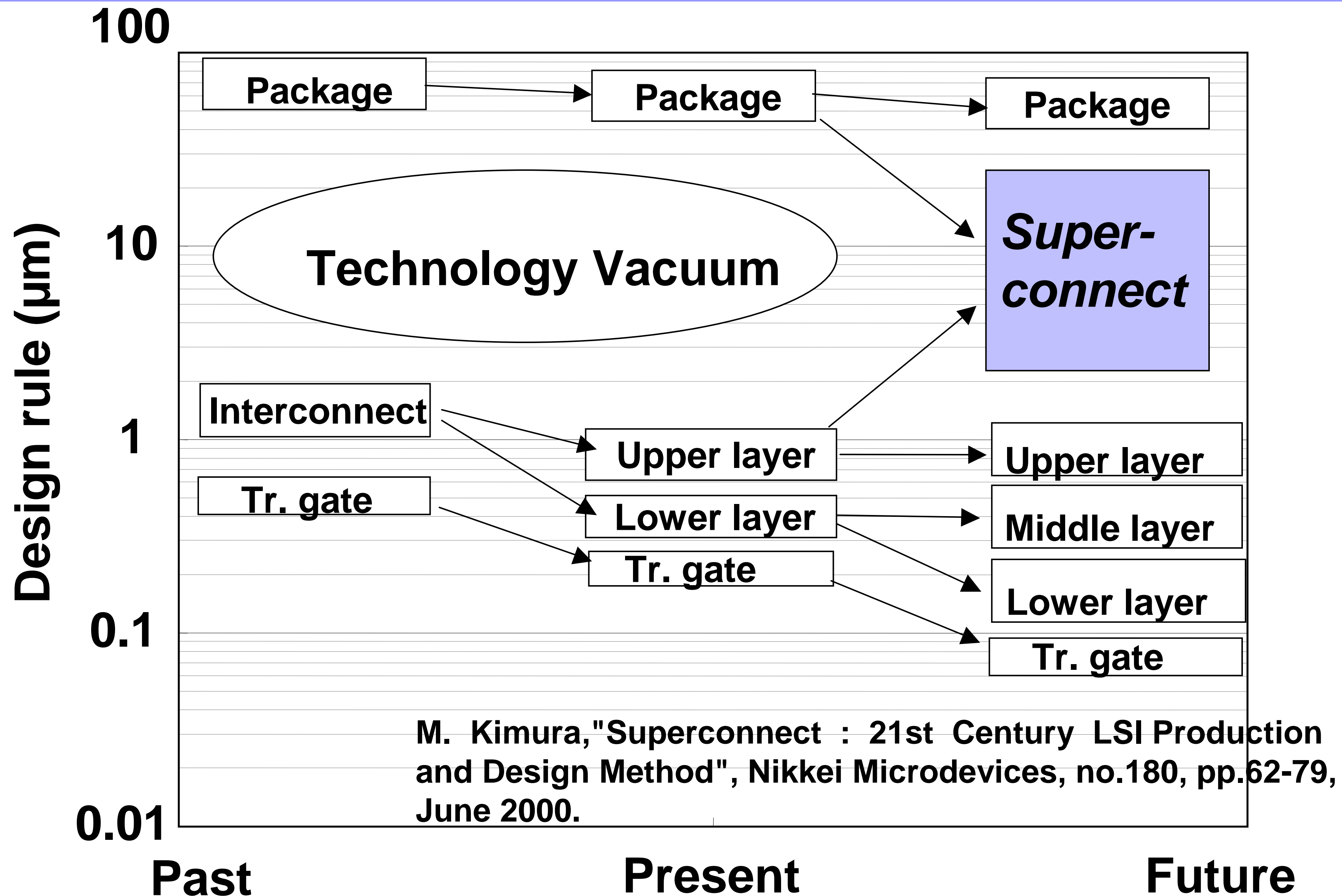
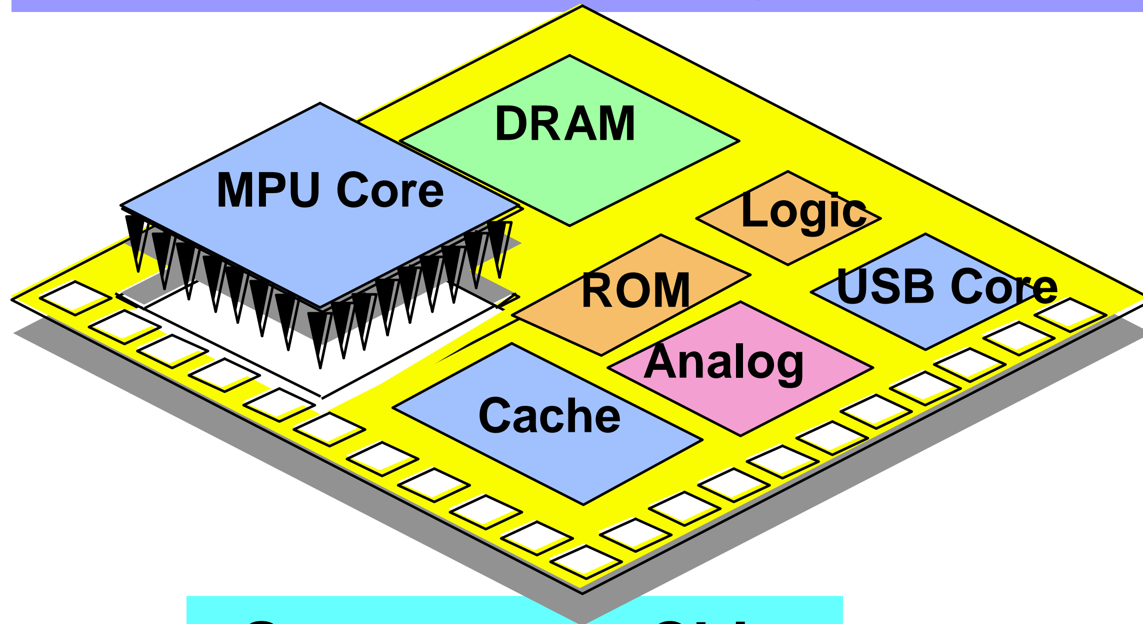
# Superconnect technology




M. Kimura,"Superconnect : 21st Century LSI Production and Design Method", Nikkei Microdevices, no.180, pp.62-79, June 2000.

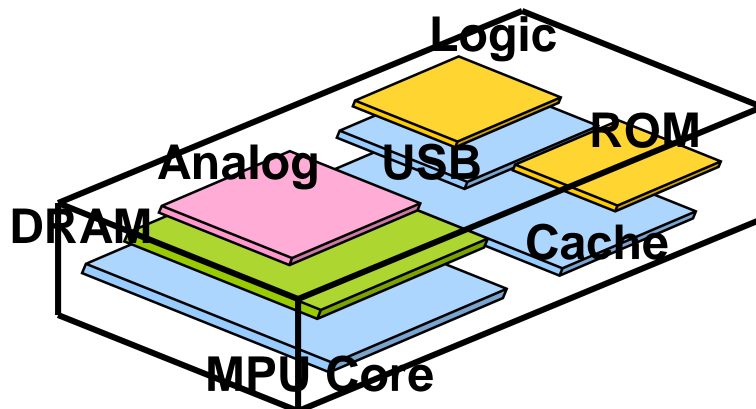
# SoC vs. System-in-a-Package



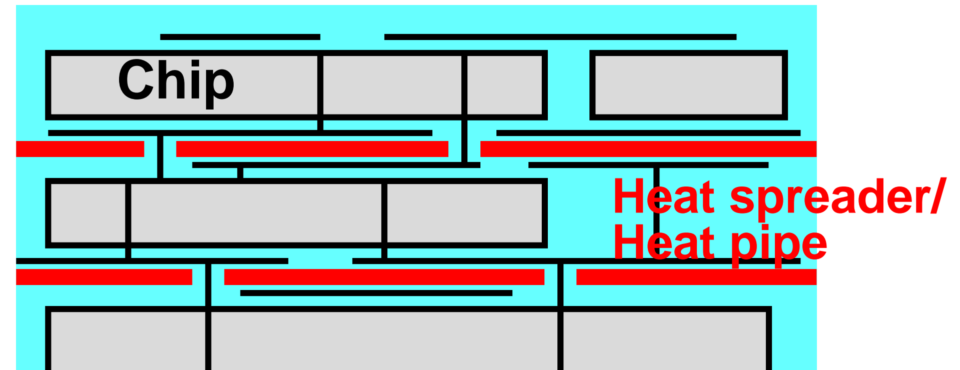

System-on-a-Chip

- Smaller area
- Shorter interconnect
- Optimized process for each die (Analog, DRAM, MEMS…)
- Good electrical isolation
- Through-chip via

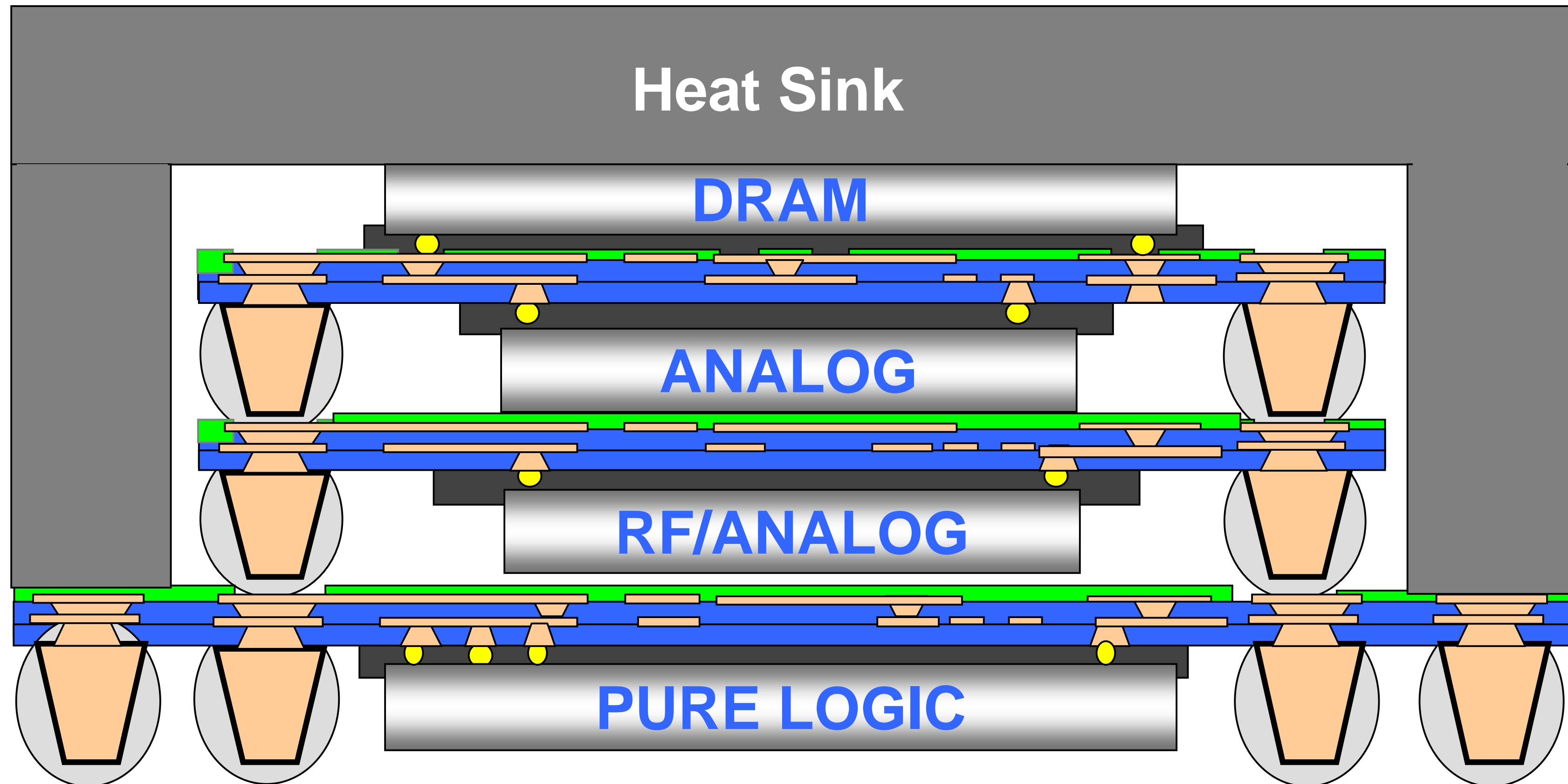
- Heat dissipation is an issue




System-in-a-Package

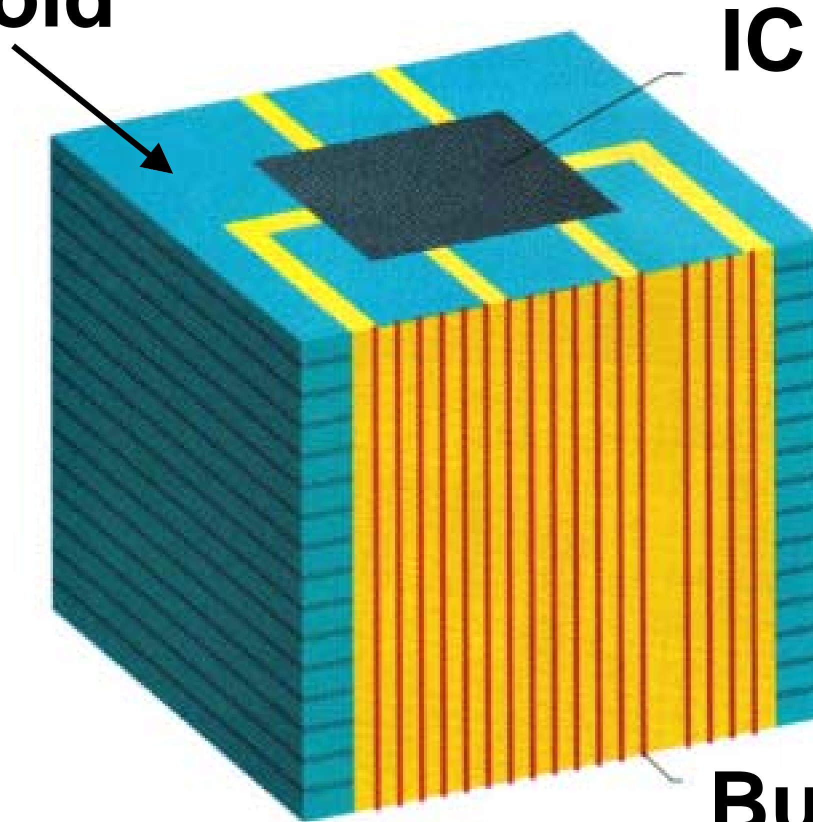


# Superconnect example based on three-dimensional assembly




K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, "3-D Assembly Interposer Technology for Next-Generation Integrated Systems," ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

# Another superconnect example: System-in-a-Cube




H.Goldstein, “Packages Go Vertical,” IEEE Spectrum, pp.46-51, Aug.2001.

# Issues in superconnect

- **Special design tools for placement & route for co-design of LSI's and assembly**
- **High-density reliable substrate and metallization technology**
- **Low-cost, available known good die (reworkablility and module testing)**

# System-in-Package

ELECTRONIC ENGINEERING

EE TIMES

eet.com The industry newspaper for engineers and technical management Monday, November 8, 1999

Expanding role of packaging seen relegating SoC to niche status

## System-chip may topple ...

*By Robert Ristelhueber*

INDIAN WELLS, CALIF. – The wheels might be coming off the system-on-chip (SoC) bandwagon, if the chatter at last week's Dataquest Semiconductor conference is any barometer of industry sentiment. Heavyweights including IBM and Lucent Technologies indicated that costs may relegate SoC to niche status, with new packaging techniques stepping into the breach.

"A couple of years ago we really thought that the embedded DRAM model would be the panacea for many applications," said John Kelly, general manager of IBM Microelectronics. "It's not always the right thing. In many applications it still remains much cheaper to do it with multichip modules. It gives you satisfactory performance and often for lower cost."

"We have systems-on-chip now that are really 'system on chips,' " said John Dickson, president of Lucent Technologies' Microelectronics Group. "We do it that way because it's most cost-effective, and the customer will prefer it that way because it offers more flexibility."

The subject was broached at the conference here by a Dataquest analyst who claimed that SoC designs will increasingly be supplanted in coming years by multichip packaging as higher mask costs squeeze SoC profitability.

Chip designers have often been willing to add mask steps

▸CONTINUED ON PAGE 6

IBM's Kelly: 'In many apps, cheaper to do it with multichip modules.'

## ... as industry grapples with impact of cores mode

*By Peter Clarke and Brian Fuller*

EDINBURGH, SCOTLAND – Intellectual property cores were a hot topic last week, both here at the IP99 Europe conference and at Dataquest Inc.'s annual semiconductor conference in Indian Wells, Calif. But as the industry struggles with new business models, new customer-supplier relationships and fast-moving technology, there was scant agreement on either side of the Atlantic on how the cores market will unfold.

On one thing there was agreement: IP cores and design reuse

## In some apps, multichip modules do the job more cheaply, conference told

## 'System-in-package' could make SoC a niche

▸CONTINUED FROM PAGE 1

and complexity to their logic devices in order to place analog and memory functions onto chips. "But when we get below 0.2 micron we get a cost shock, and the [return on investment] will be diminished or even eliminated in many cases," said Clark Fuhs, vice president and director of Dataquest's Semiconductor Manufacturing Programs.

Mask costs will dramatically rise at deep submicron because of the use of phase-shift and optical proximity correction techniques as well as more expensive, 193-nm lithography equipment, putting low-volume SoC at a cost disadvantage, Fuhs said.

Militating against SoC designs for many applications is the wide disparity in revenue per square inch among the various blocks in the chip, Fuhs said. "The DSP or microprocessor block can be getting $150 or $200 per square inch, the FPGA about $120, the analog block about $35, the memory block about $50 to $60 ... You're basically diluting your high-value logic pieces with all these other low-value pieces, yet you're adding cost because you're adding mask levels."

An alternative is to fabricate the different blocks as discrete chips, placed close together using chip-scale packaging, Fuhs said. "This enables you to build the pieces in fabs that are optimized for those pieces. You can build analog in a 0.7-micron fab, standard logic can be done in 0.35 or even 0.5 micron, and for the memory you can buy a wafer from somebody and break it up. The package is more expensive, but the overall system cost is going to be substantially less.

"The concept here is to take some level of interconnect ... and simply move [it] from the chip into the package."

Fuhs noted that Intel's Pentium III is actually an 11-level-metal device–six levels of aluminum inside the chip and five levels of copper outside. And he showed a photograph of a Sony digital Handycam, which he said contains 20 chip-scale devices, "so this technology is here, it's real."

In the not-too-distant future, he said, wafer foundries will give customers a choice of implementing a design either as a system-on-chip or as several discrete devices using chip-scale packaging.

To survive, the SoC must evolve to fit a more standard-product model that would allow it to increase volume and become more cost-efficient, Fuhs said. He predicted that within five years, multichip packaging will be growing faster than SoC designs.

That view has its detractors. "Mask sets cost in excess of a couple hundred thousand dollars, whether you do small chips or large chips," said National Semiconductor Corp. chief executive officer Brian Halla, who has championed the notion of an information appliance-on-a-chip. "I can get tremendously more performance out of the same square inches of silicon by having it all together instead of having it two inches apart on a board.

National's Halla touts 'integrated disintegration.'

"SoC isn't a marketing crusade anymore; it's something you can do because the technology allows it," Halla added. "A very small die can contain an awful lot of functionality."

Halla noted that Intel used to say graphics shouldn't be combined with the microprocessor, because the pace of innovation differs between those parts; but Intel's upcoming Timna processor, he said, combines both functions.

"Having said all that, there are cases where we agree [about putting a system on a package]," he said. "There is a substrategy of ours called integrated disintegration, which means there are analog functions you can pull off the chip because they are such a tiny portion of the overall chip, and yet they are the most difficult thing to port to the next-generation [process] technology."

IBM's Kelly said that "SoC integration has to be done se-

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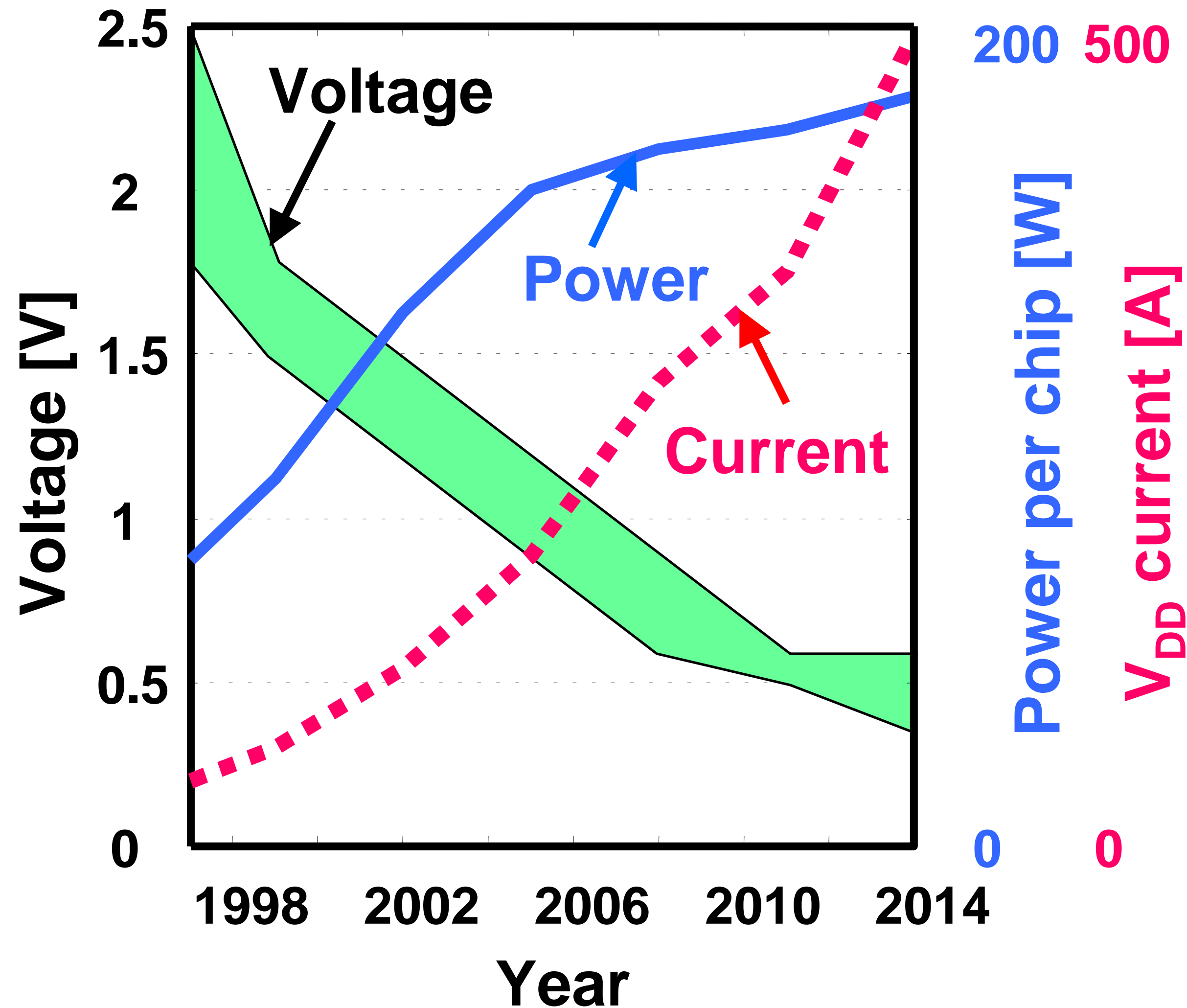
- Complexity crisis

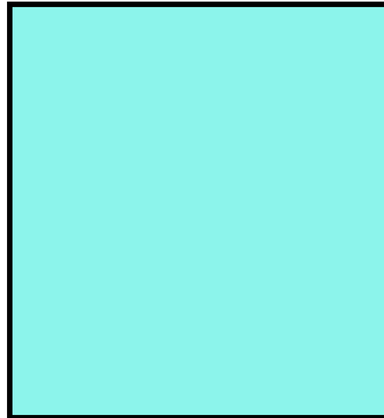
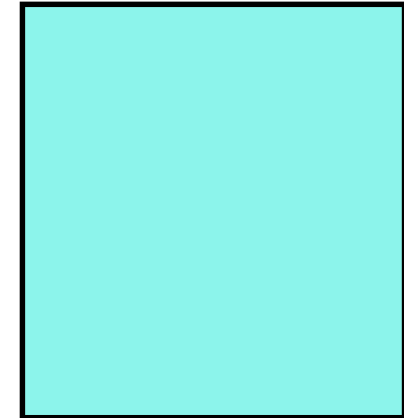
# $V_{DD}$, power and current trend



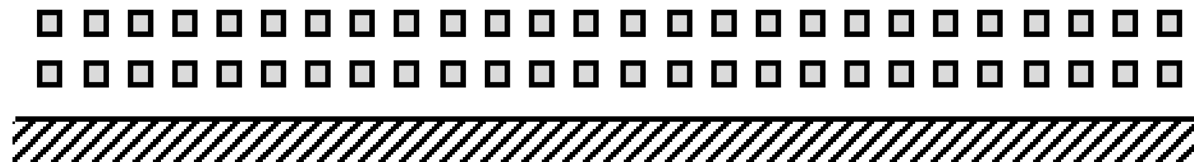

International Technology Roadmap for Semiconductors 1999 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

# Interconnect Cross-Section and Noise

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply

Scaled interconnect
- Signal



1V 20W →20A current

5% noise →0.05V noise →~0.02V / 20A→~10μm thick Cu

Thick layer interconnect, area pad, package are co-designed.

# Three crises in VLSI designs

- Power crisis
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# DSM interconnect design issues

**Larger current**

- IR drop (static and dynamic)
- Reliability (electro-migration)

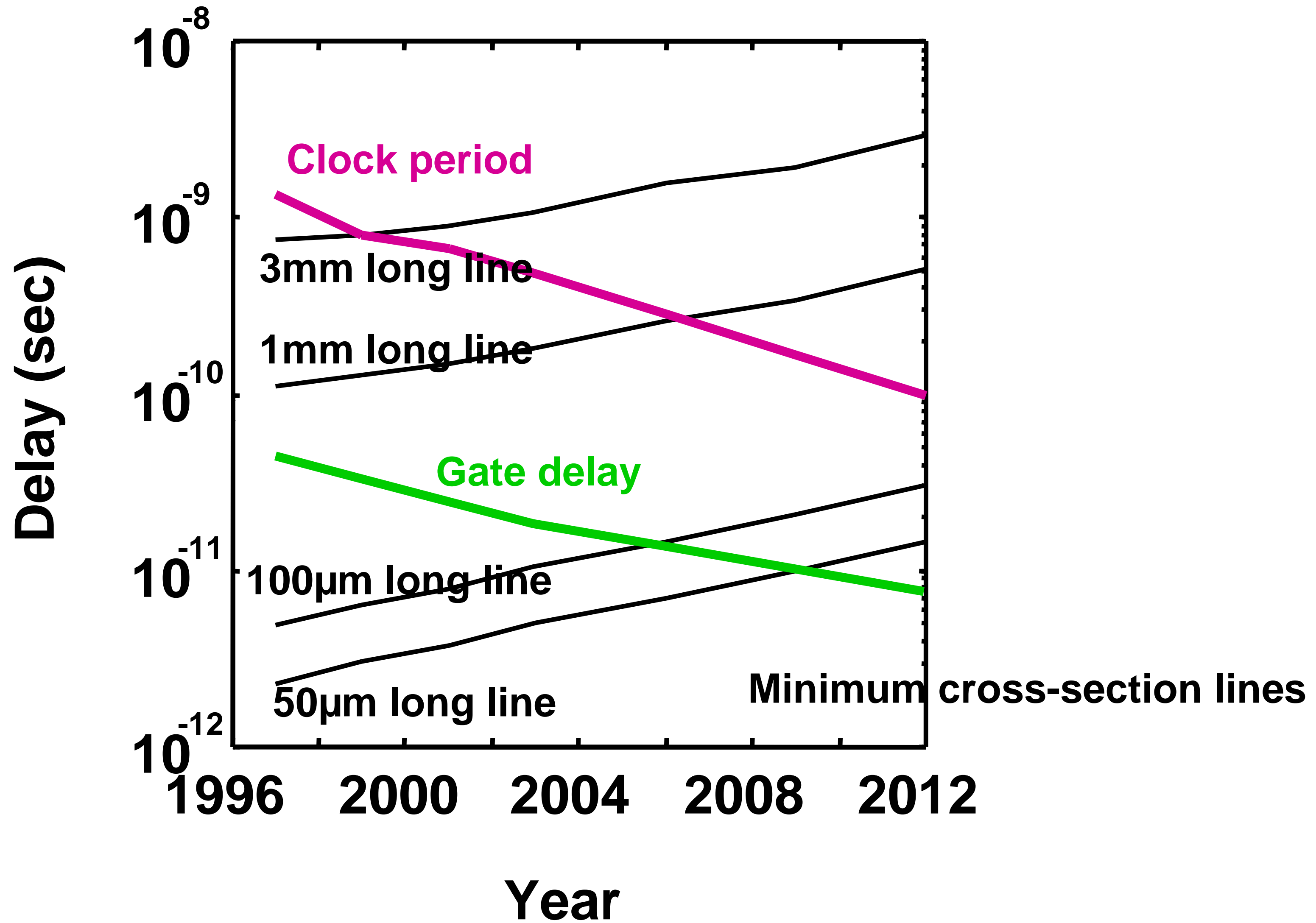
**Smaller geometry / Denser pattern**

- RC delay
- Signal Integrity
- Crosstalk noise
- Delay fluctuation

**Higher speed**

- Inductance
- EMI

# RC delay increase is a headache

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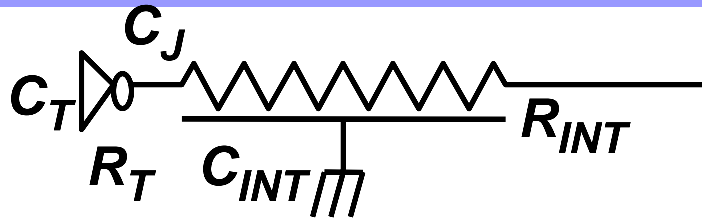
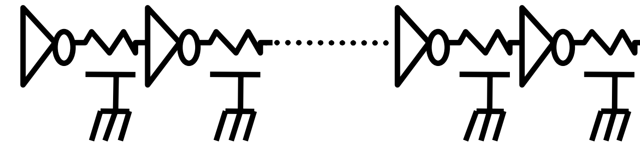
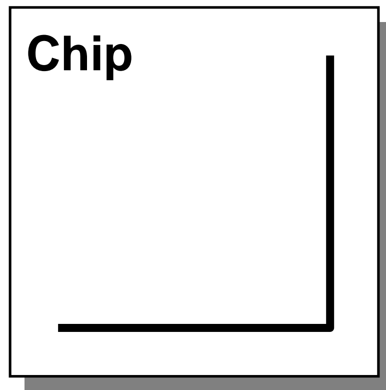
# Buffered interconnect delay



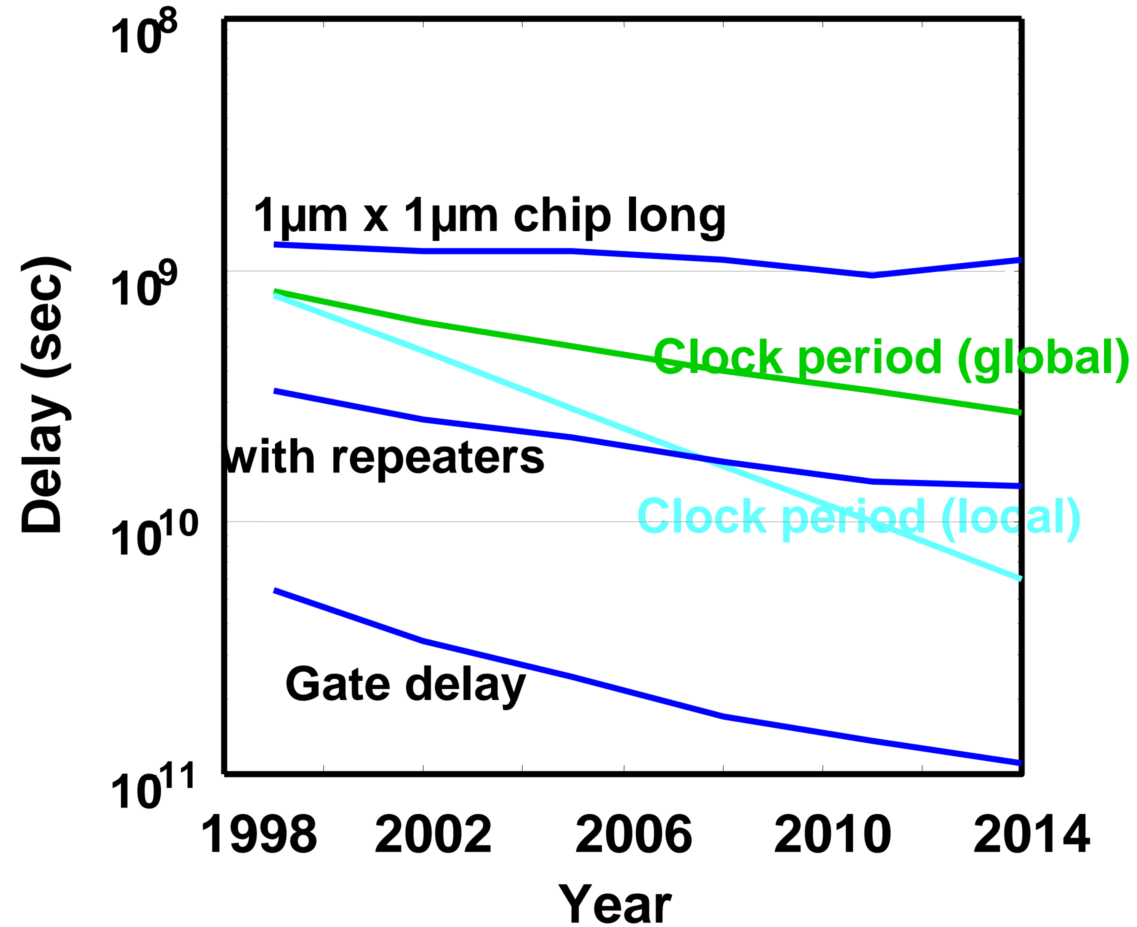

a) Without repeaters



b) With repeaters




Global interconnect

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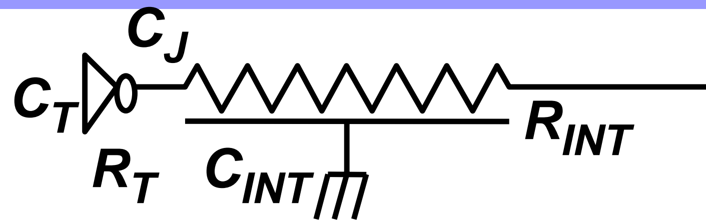
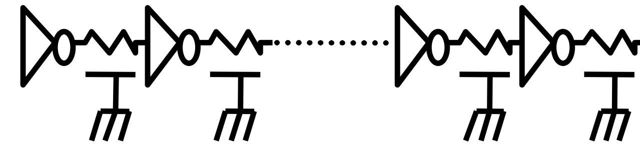
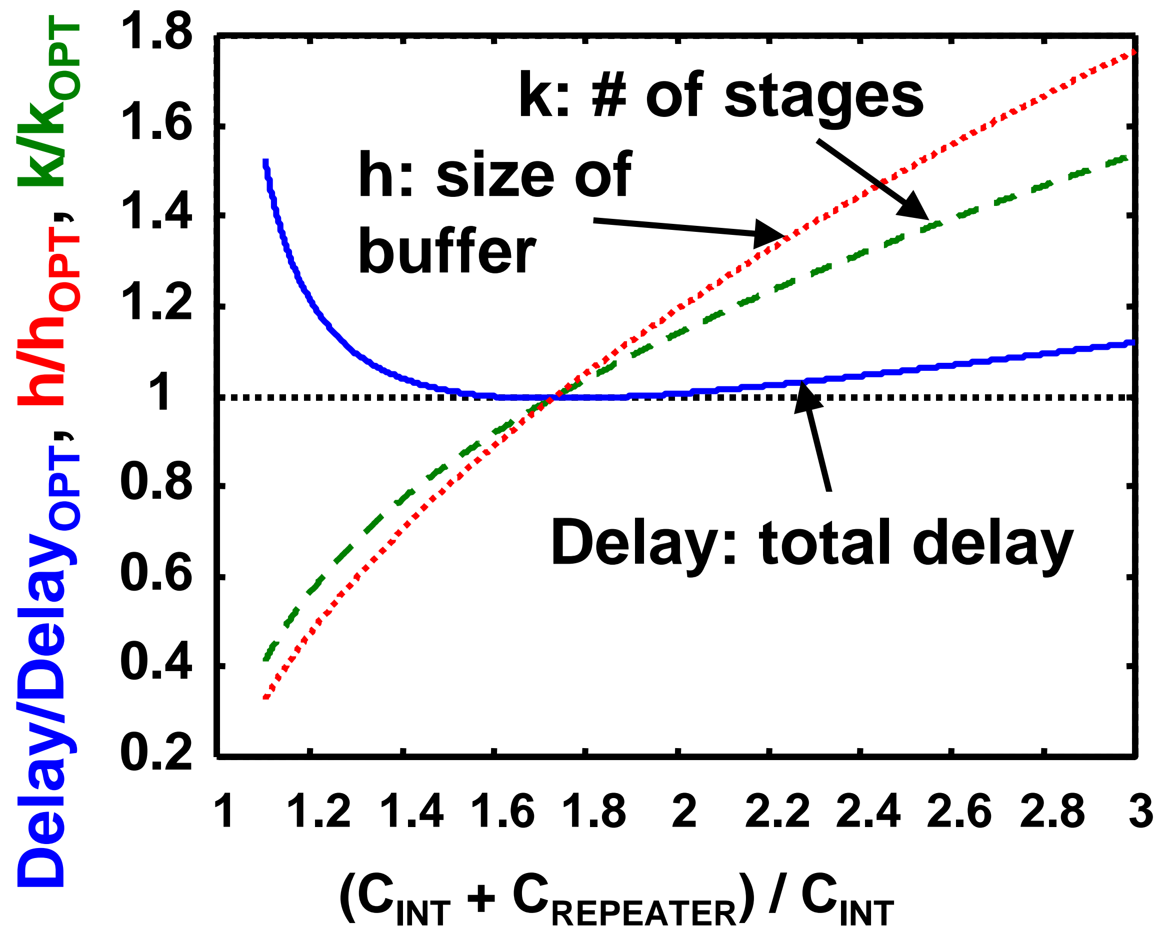
# Power increases with buffer insertion




a) Without repeaters



b) With repeaters

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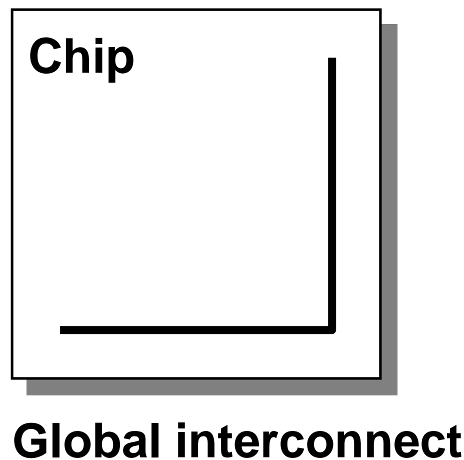
# Superconnect may decrease RC delay without power increase




Minimum cross-section interconnect

18mm x 18mm

30mm x 30mm

Clock period

6μm x 2μm cross-section interconnect

Delay (sec): $10^{-6}$, $10^{-7}$, $10^{-8}$, $10^{-9}$, $10^{-10}$

Year: 1998, 2002, 2006, 2010, 2014

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# Summary

- LSI technology should meet the challenge of three crises: Power, Interconnect and Complexity crises.
- SoC based on IP's solves the complexity crisis but issues remain.
- As complement to SoC, new system level integration called superconnect is pursued.
- Superconnect will help solve LSI design issues .

# Assembly & Packaging

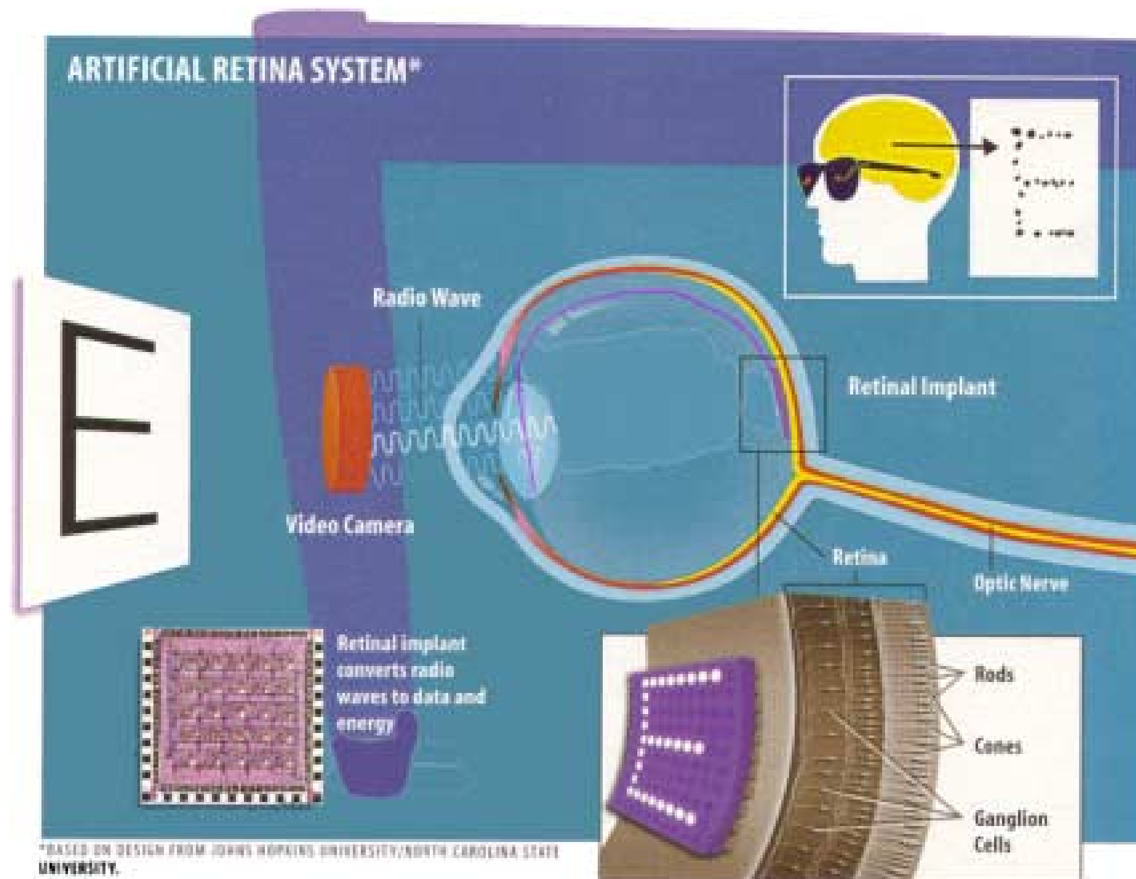
**"There is an increased awareness in the industry that assembly and packaging is becoming a differentiator in product development."**

**Excerpt from "International Technology Roadmap for Semiconductors, ITRS'99 p.213"**

# Bio-medical application needs new assembly technology

NC STATE UNIVERSITY

Retinal Prosthesis




Courtesy: Prof. Wentai Liu (North Carolina Univ.)
http://www.ece.ncsu.edu/erl/faculty/wtl_data/retina.html