ISSCC'02 Feb. 5 Evening Panel

Low-Voltage Design or the End of CMOS Scaling?

Organizer: Akira Matsuzawa (Matsushita)
Kunihiro Iizuka (Sharp)

Moderator: Takayasu Sakurai (Univ. of Tokyo)

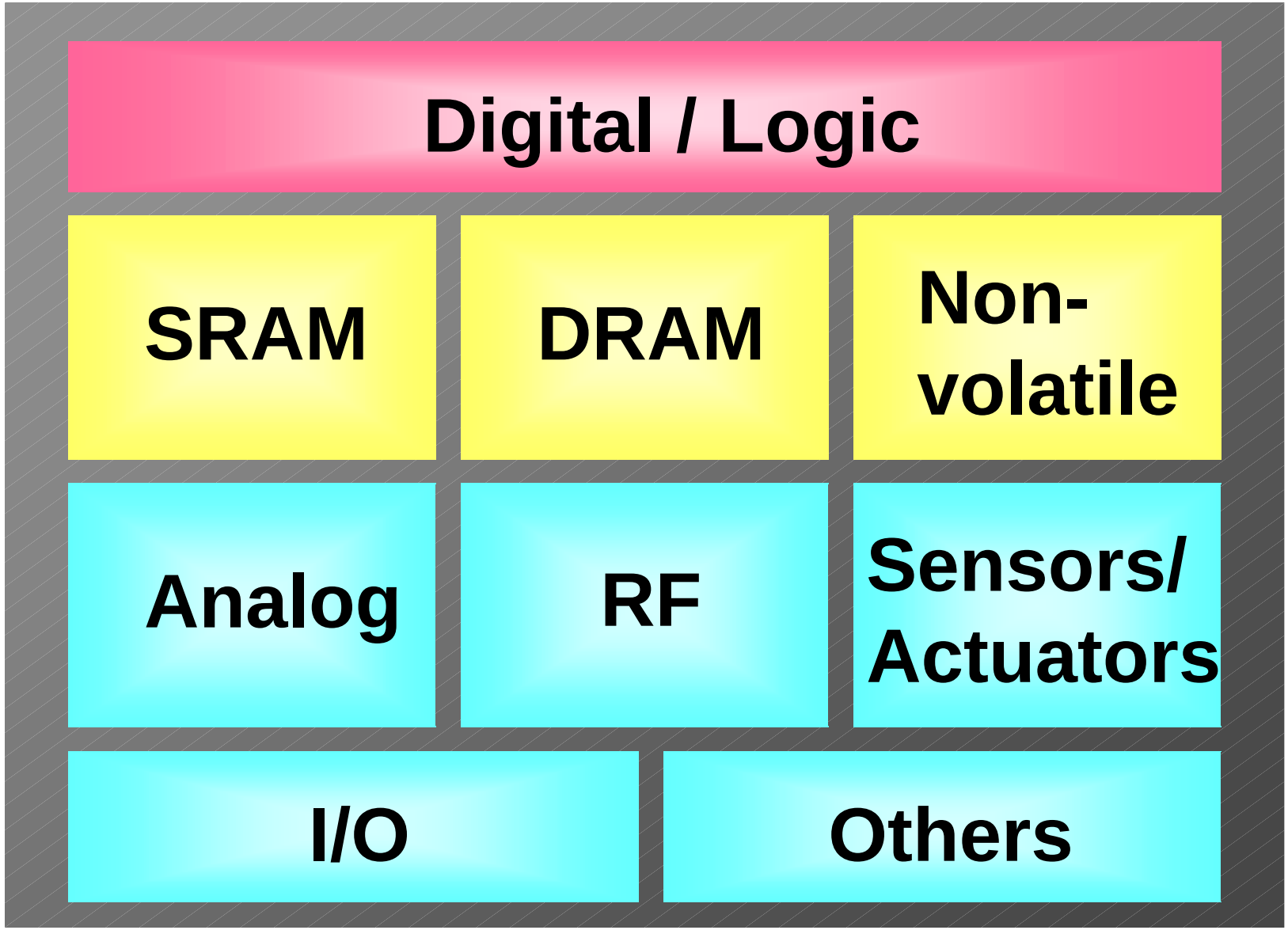
Panelists:

Asad Abidi	U.C.L.A	Analog/RF
Daniel Senderowicz	SynchroDesign	Analog/SW cap.
Akira Matsuzawa	Matsushita	Analog/DAC, DAC
Alex Shubat	Virage Logic	Memory/SRAM
Junichi Miyamoto	Toshiba	Memory/Non-vol.
Shekhar Borker	Intel	Digital/µP

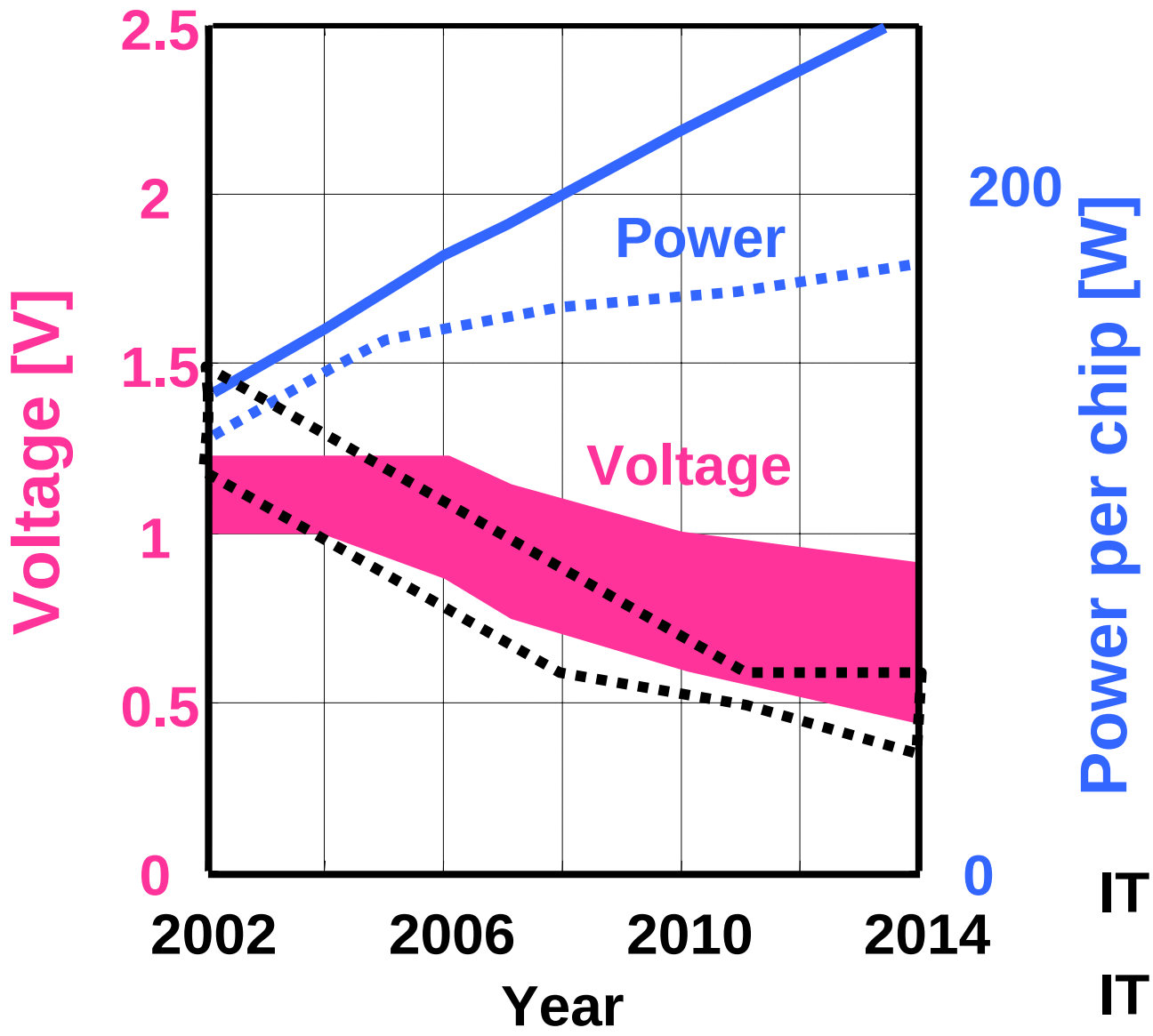
Low-voltage design or the end of CMOS scaling?

1. Is there minimum V_{DD}? Why?
2. After the V_{DD},min is reached, how can we improve the cost-performance w/o scaling?
3. What implications to the SoC design?

System on a Chip (SoC) in 2010



V_{DD} and power estimate from ITRS



ITRS 1999 (dotted lines)

ITRS 2001 (solid lines)

How low can we go?

Name	Area	VDD,min (V)	Limitting factor
Asad	Analog	2.5~1V	Dynamic range imposed by physical world
Daniel	Analog	~1.5V	Dynamic Range, DEVICE LIMITATIONS
Matsuzawa	Analog	0.8~1.8V	Amplifior scheme→Headroom Dynamic range
Alex	Memory	Will Scale	I_k/I_L, NM, Prpcess V
Miyamoto	Memory	follow logics	prpcess complexity
Shekhar	Digital	<200mv	Micro-Architectures to comprehend effec

How to improve cost-perf. w/o scaling

Name	Area	Mainly Technology or Circuit?	Possible cost-perf. improvement senario
Asad	Analog	Both	Better, more compact passives
Daniel	Analog	Both	Operate at the highest possible VDD and enjoy the high-performance devices with clever design techniques.
Matsuzawa	Analog	Technology and CKT	・FD-SOI for switch ・Hi-accurale passive ・Small analog, big digital
Alex	Memory	Both T(1/3) C(3/3)	・Optimization at small block Lennel ・More options T+C
Miyamoto	Memory	Both	miniaturization-(Muliti-bit)-Newmaterial -stack(3D)
Shekhar	Digital	Both.Technology&circuit to support	Tech.will provide integration capatit, circuib will exploib it to obtain higher performance

T.Sakurai

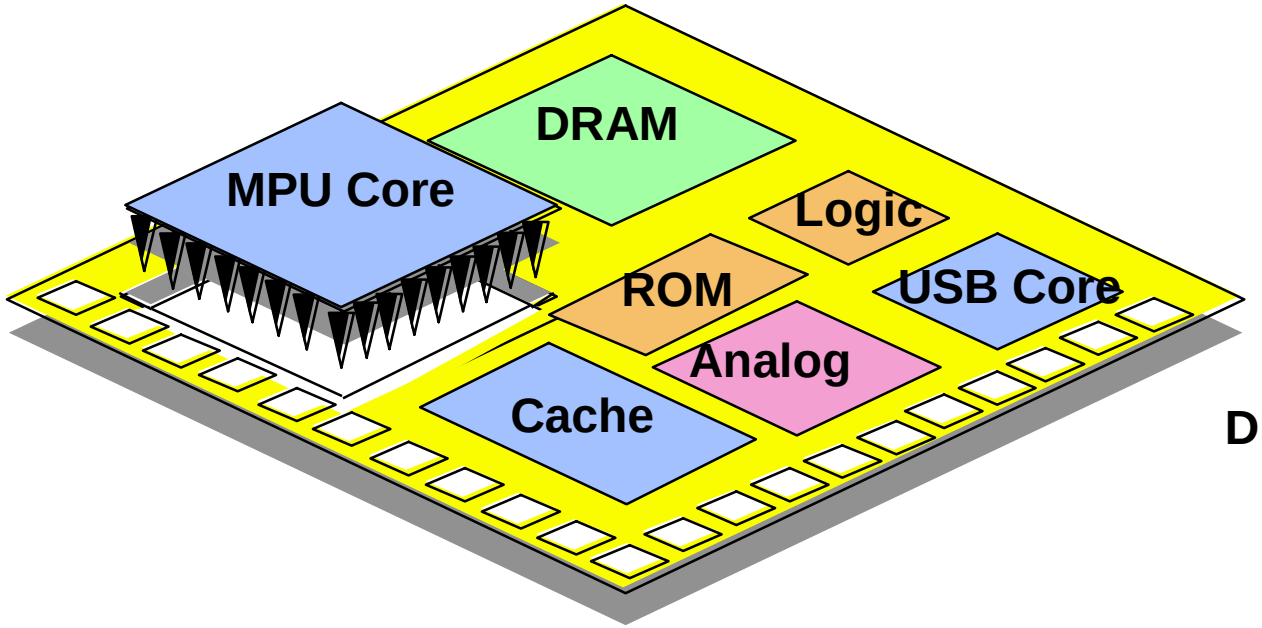
Implications to SoC in 2010

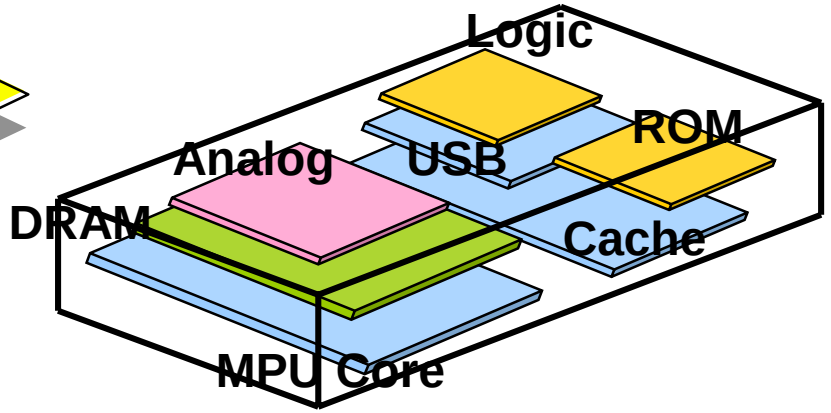
Name	Area	# of VDD's	# of tr. Option	Vary VDD in time?	Vary VTH in time?	SoC/SiP MOC
Asad	Analog	2	4	No	No	MOC
Daniel	Analog	2	4	No	No	NO
Matsuzawa	Analog	3	5	YES	YES	50%SoC 50%SiP
Alex	Memory	.....	.....	YES	Yes (BACK B, Reast)	Soc=#
Miyamoto	Memory	2(1 for I/O 1 for V_{DD})	at least 4	No	YES	depending on the system
Shekhar	Digital	>3	2-3 2-Digital	YES	YES	NO

Basic PMOS-high Thick.tox

Basic NMOS high Thick.tox

No SoC, please





System on a Chip

System in a Package

- Voltage optimized process for each die (Analog, DRAM, MEMS…)
- Good voltage isolation