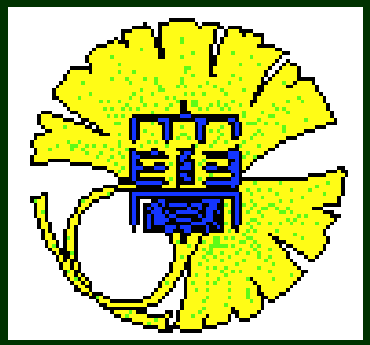
VTCMOS characteristics and its optimum conditions predicted by a compact analytical model

Hyunsik Im, T. Inukai, H. Gomyo, T. Hiramoto, and T. Sakurai



Low Power Group

Institute of Industrial Science, University of Tokyo

OBJECTIVE

- √ To develop a compact analytical model of VTCMOS
- √ To demonstrate the low power operation of VTCMOS
- √ To investigate the short channel effect on VTCMOS
- √ To find optimum device conditions

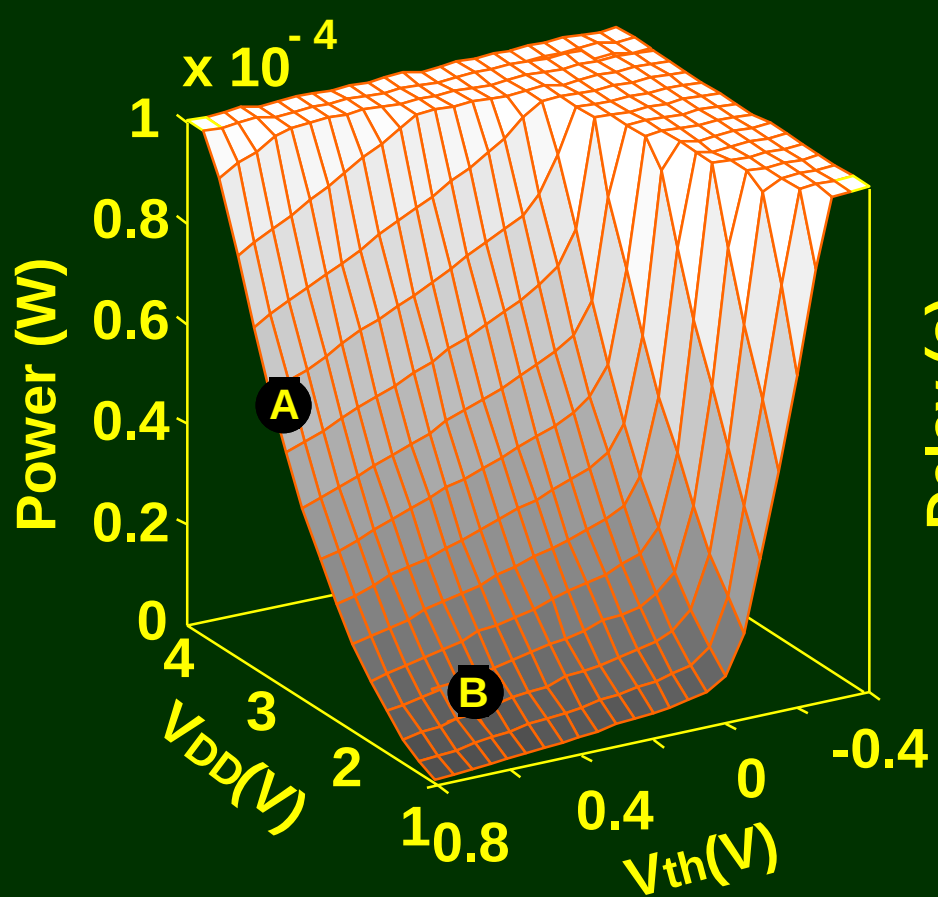
Contents

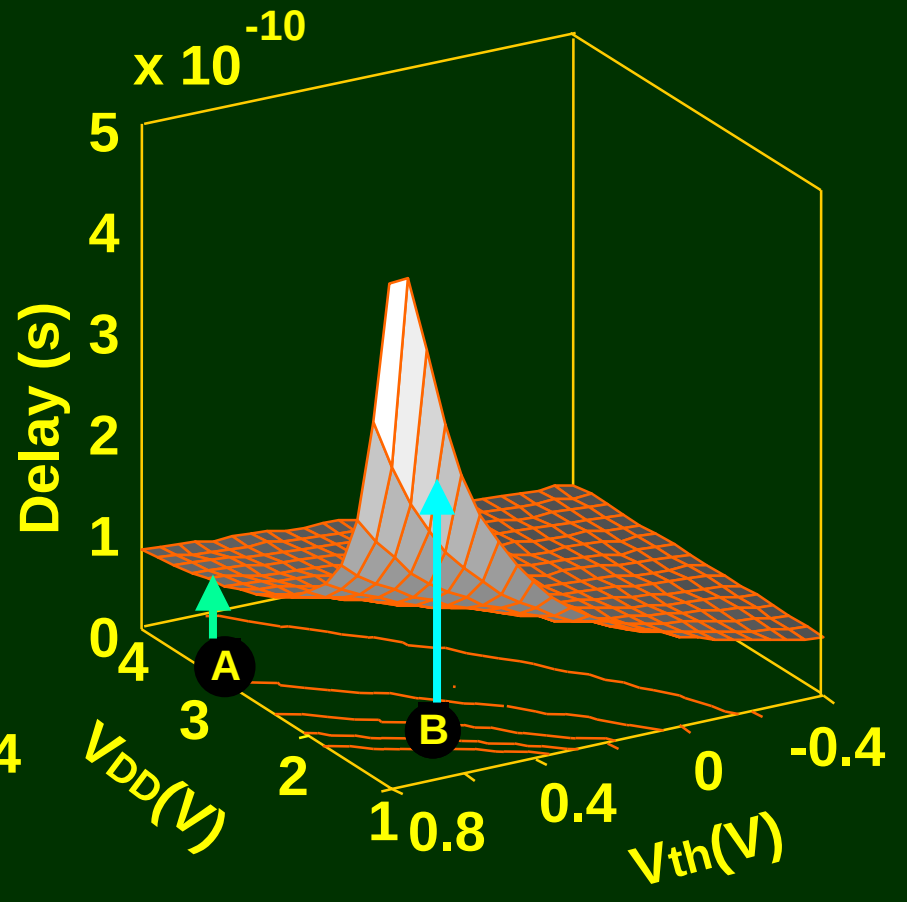
- √ **Introductory part**
  - **Necessity of low power MOSFET technology**
  - **Variable Threshold-Voltage CMOS (VTCMOS)**
- √ **Previous work: Numerical simulations of VTCMOS**
- √ **Analytical model of VTCMOS**
- √ **Short Channel Effect on VTCMOS**
- √ **Optimum conditions of VTCMOS**
- √ **Conclusions**

Introduction

Circuits' speed and power dissipation

$$P_{total} = P_{active} + P_{static} = f\, C_{load} V_{dd}^{\,2} + I_o\, 10^{-\frac{Vth}{S}} V_{dd}, \quad t_{pd} \approx \frac{C_{load} V_{dd}}{I_{on}} \propto \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

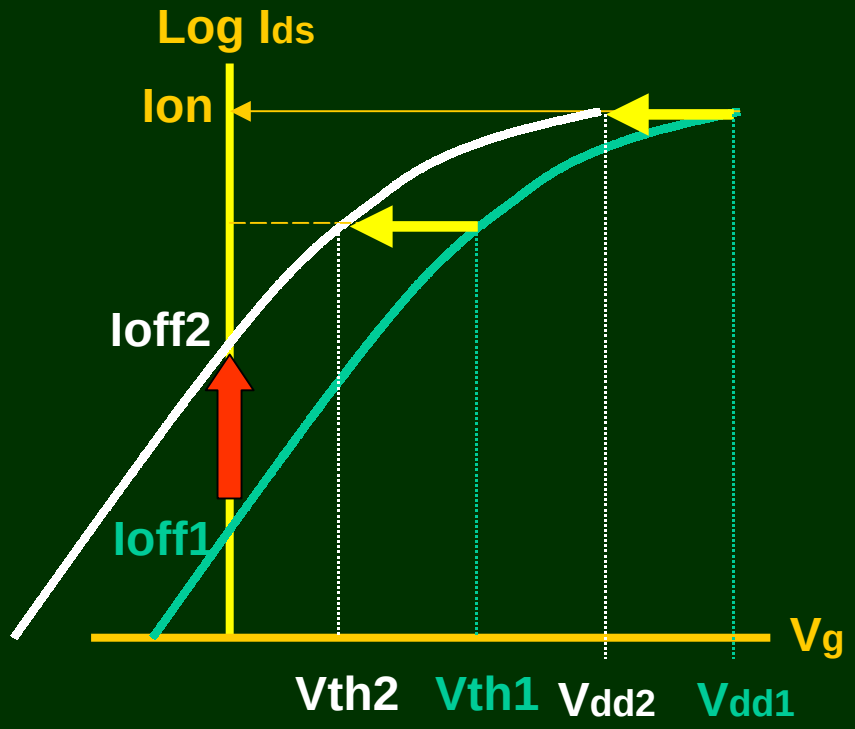




Introduction

Tradeoffs in Low Power Devices

$$P_{total} = P_{active} + P_{static} = f C_{load} V_{dd} + I_{leak} V_{dd}$$



$$t_{pd} = \frac{C_{load} V_{dd}}{I_{drive}} \propto \frac{V_{dd}}{(V_{dd} - V_{th})^{1.5}}$$

Low V_{dd} for low ac power

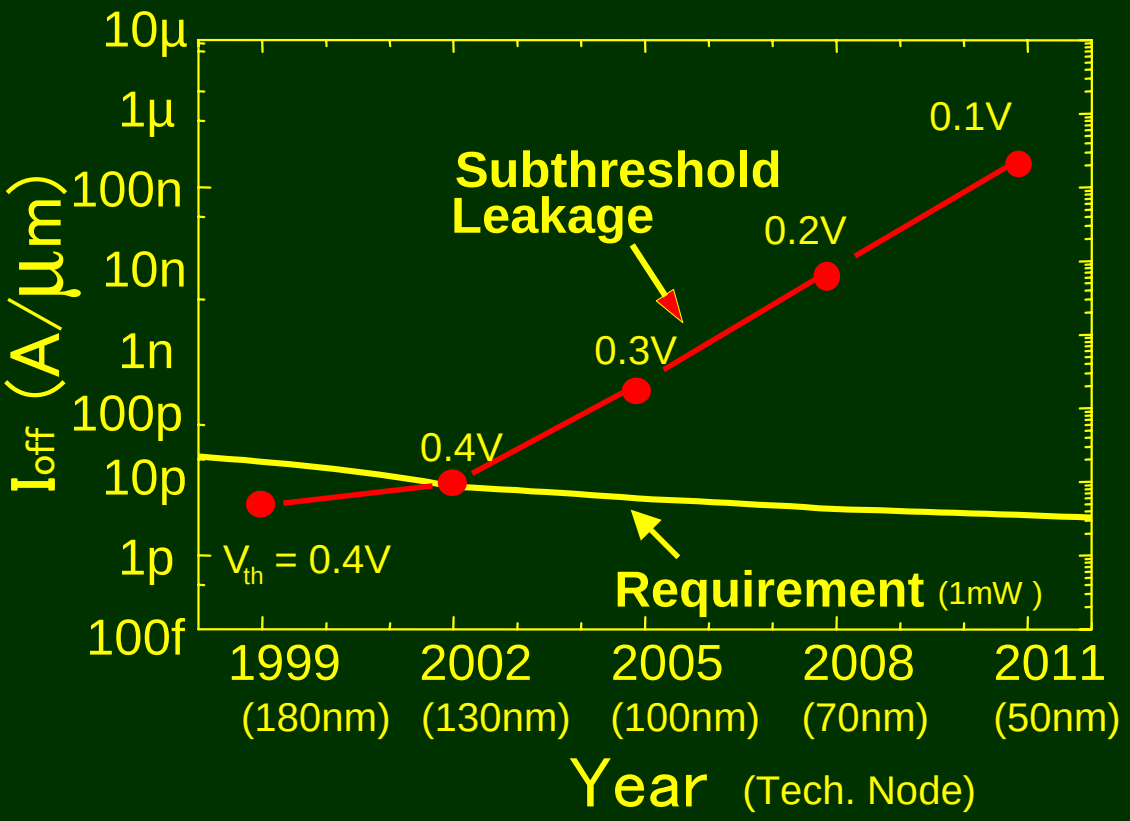
Low V_{th} for high speed

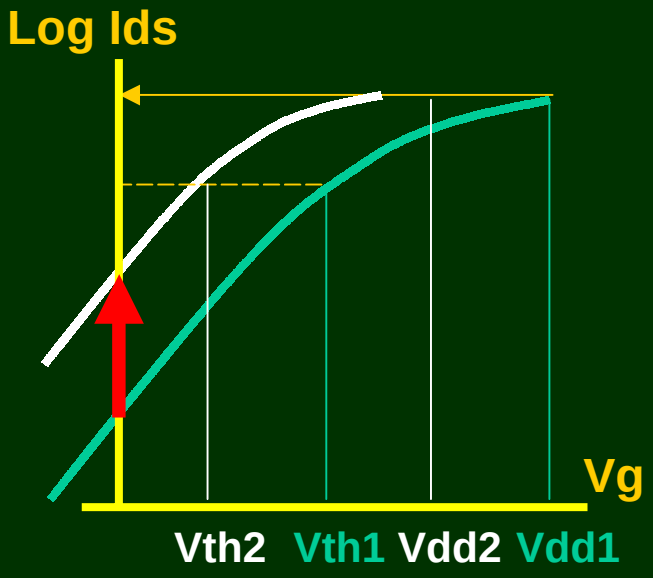
Explosion of stand-by power

Strong demand for ultra-low power VLSI

Introduction

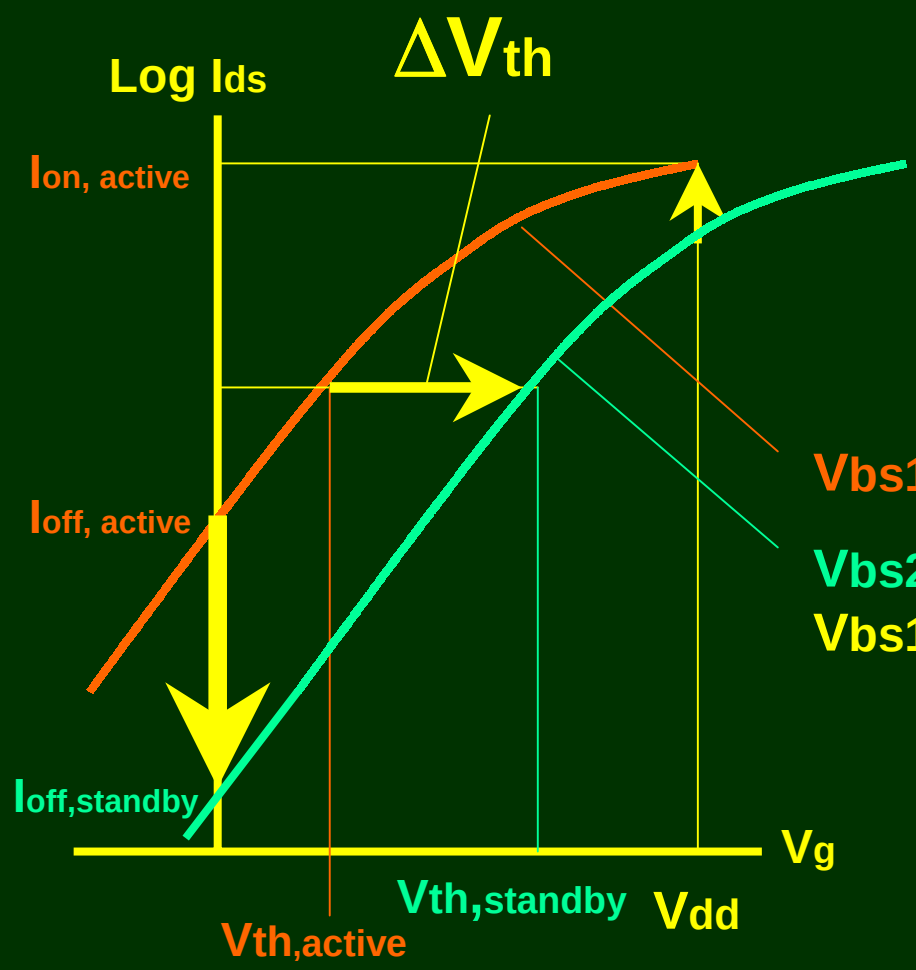
Explosion of Stand-by Power

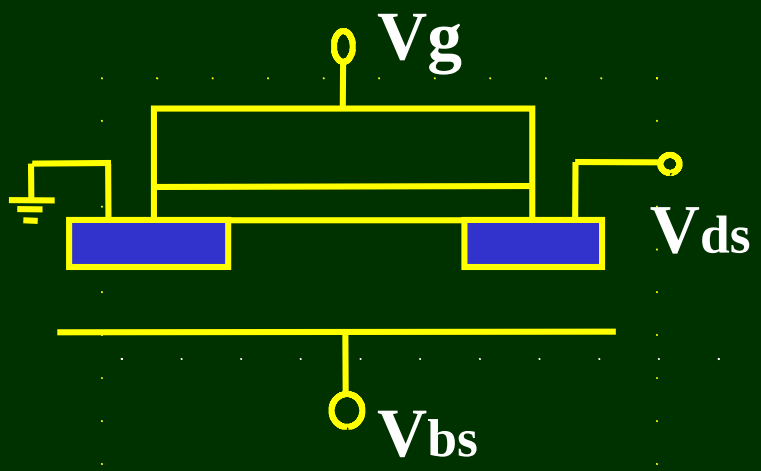




Necessity of low power VLSI technology ➡ **VTCMOS**

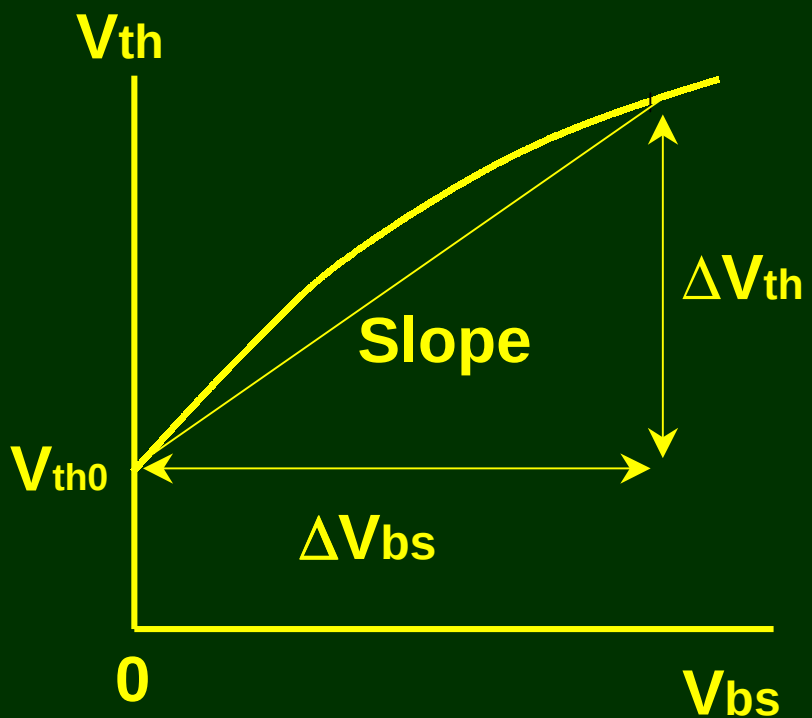
Variable Threshold-Voltage CMOS (VTCMOS)





What determines ΔVth?

Body effect factor γ



$$\gamma \equiv \frac{|\Delta V_{th}|}{|\Delta V_{bs}|}$$

Then $\Delta Vth = \gamma \times |\Delta Vbs|$

$\gamma \propto C_D / C_{OX}$ C_D: Depletion layer cap. C_{OX}: Gate oxide cap.

(irrespective of device structure)

- Directly related to ΔV_{th}
- Applicable to any devices (including SOI devices)
- Also related to SCE

γ ranges from 0.1 to 0.2 in advanced MOSFET's

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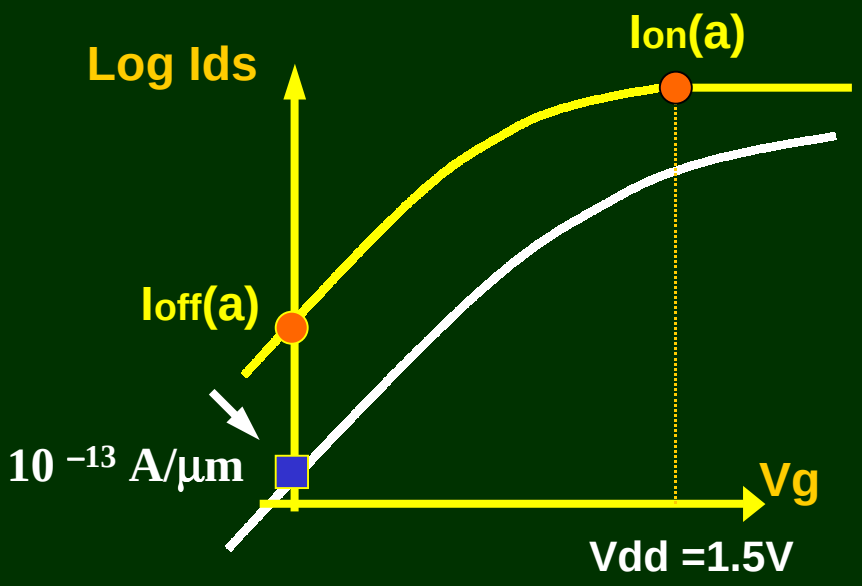
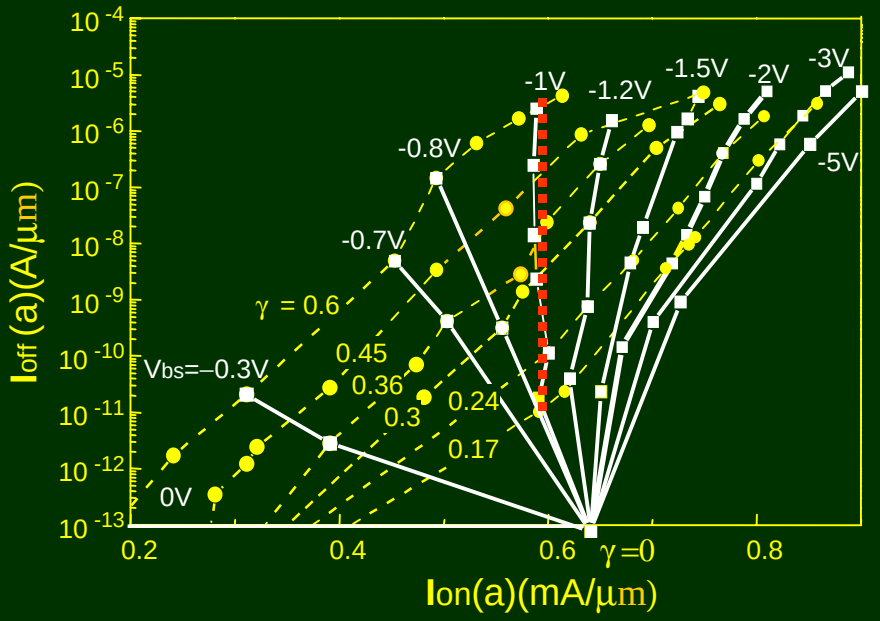
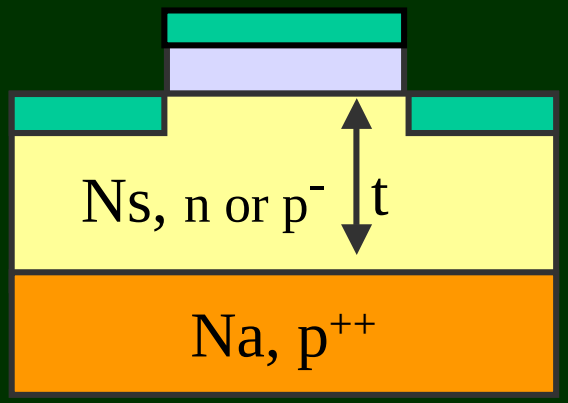
Numerical simulations of VTCMOS

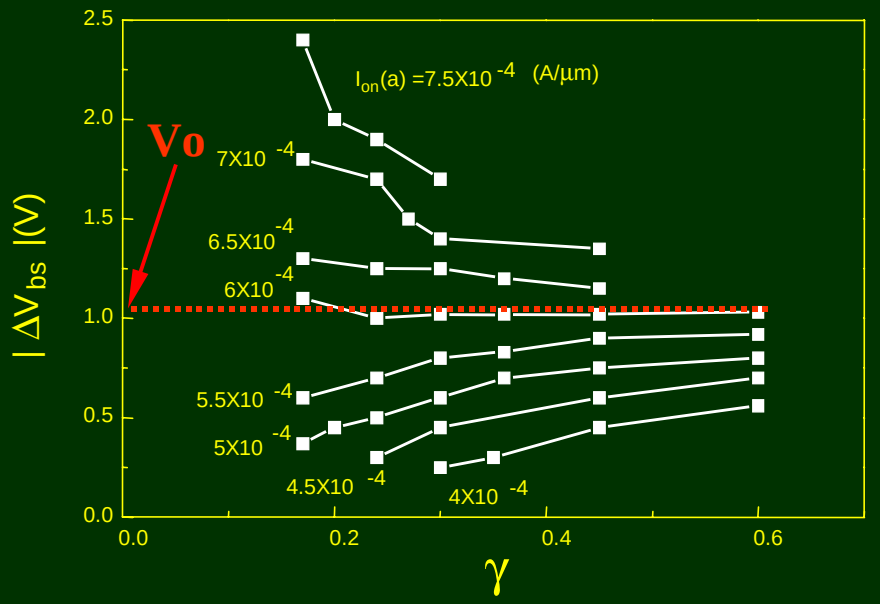
Koura et al, JJAP pp.2312 (2000)







Simulation procedure



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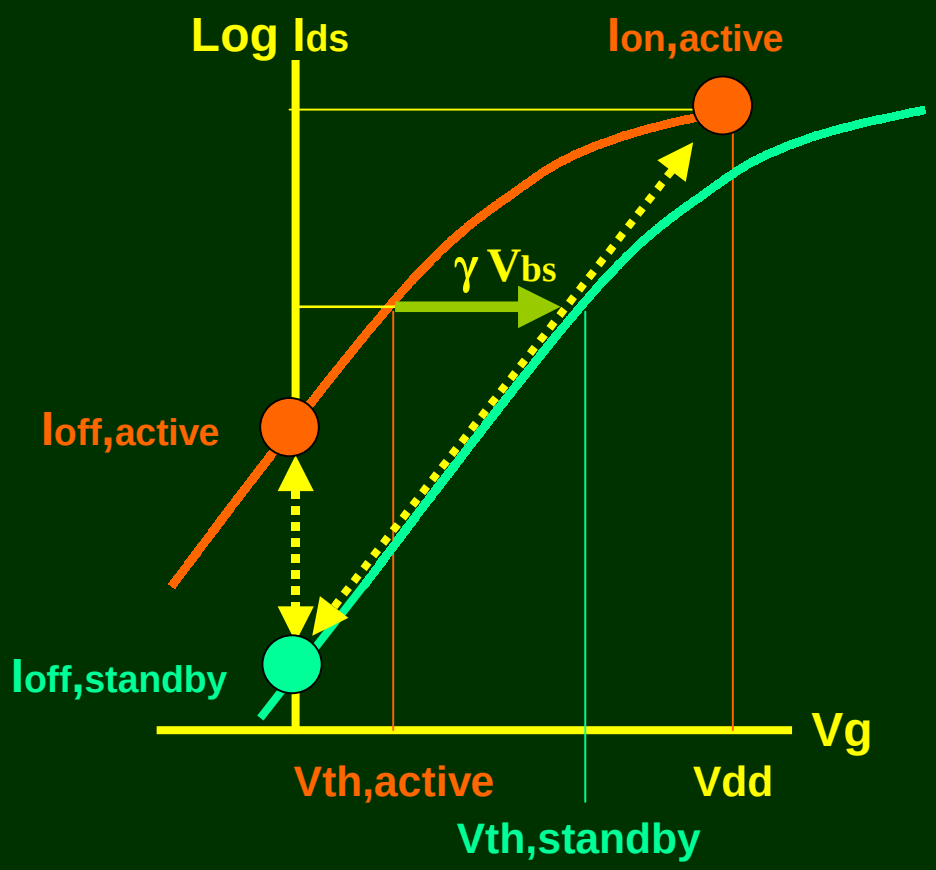
Purpose of Analytical VTCMOS Model



In terms of γ, *S* and V_{bs},

Find the following relations:

$I_{OFF}(S)$

$I_{ON}(a)$ $I_{OFF}(a)$

√ **Compact and practical only includes γ, *S*, and Vbs**

√ **Applicable to any devices including short channel VTCMOSs**

Analytical VTCMOS Model ($I_{off,\ active}$)

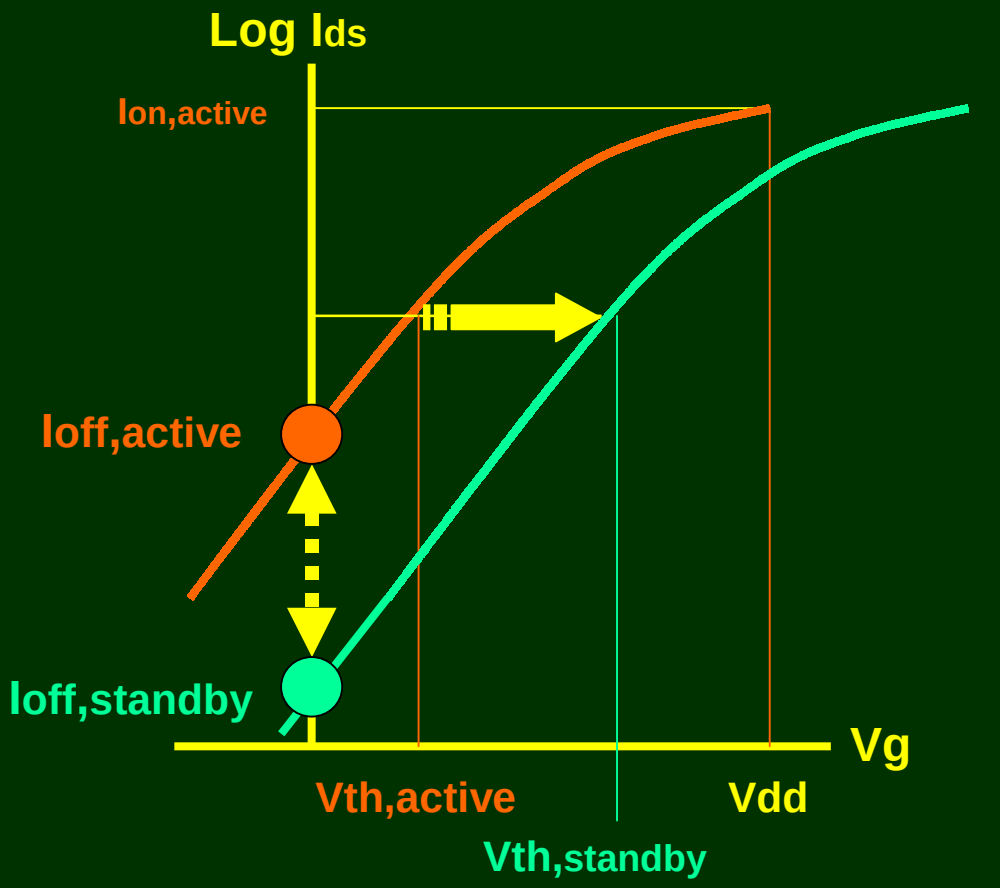
$I_{OFF}(a) \Leftrightarrow I_{OFF}(s)$

Using the definitions of sub-threshold slope (S) and threshold voltage (V_{th}):

$$S \cong \left(\frac{\Delta \log_{10} I_{ds}}{\Delta V_g}\right)^{-1}$$

$$V_{th} = V_g \text{ when } I_{ds} = \frac{W_g}{L_g} 10^{-7} (\text{A})$$

$$r \equiv \frac{I_{off}(a)}{I_{off}(s)} \cong 10^{\frac{V_{th}' - V_{th}}{S}} = 10^{\frac{\gamma |V_{bs}|}{S}}$$



Analytical VTCMOS Model ($I_{on,\ active}$)

$I_{ON}(a) \Leftrightarrow I_{OFF}(s)$

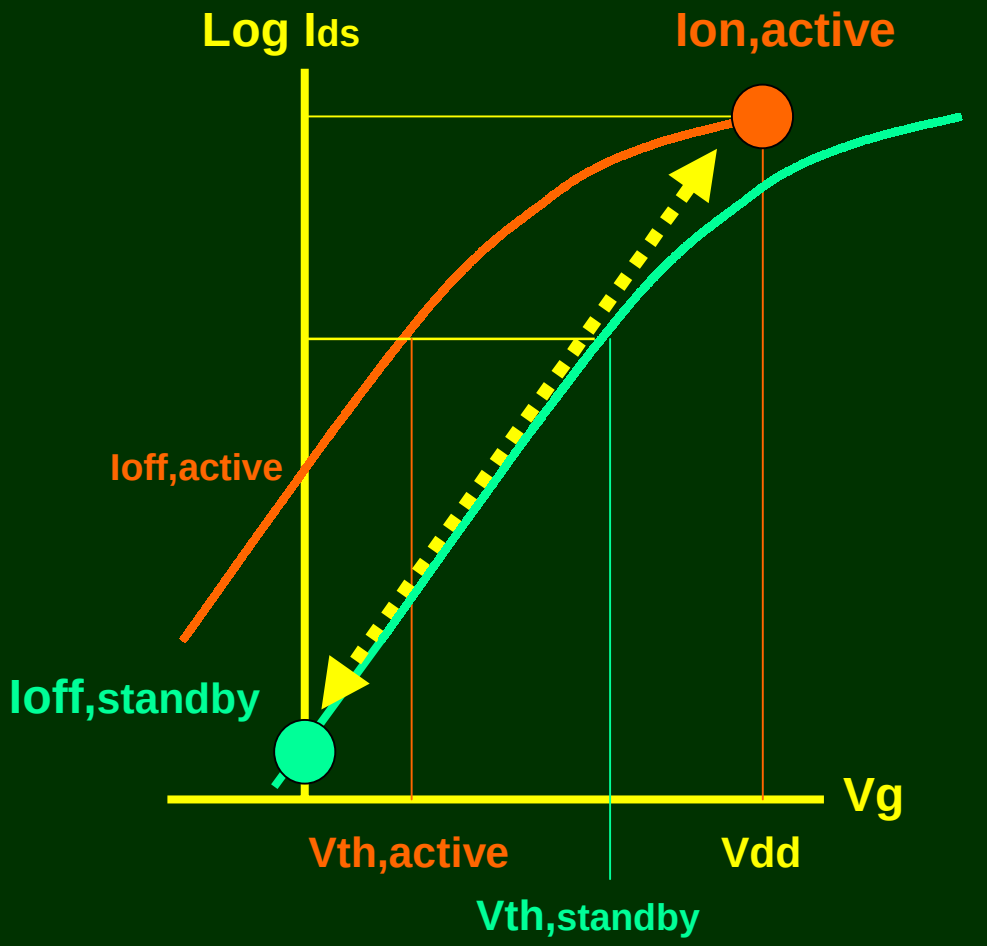
Using the α-power law model:

$$I_{on}(a) = B\,(V_{dd} - V_{TH})^{\alpha}$$

$$V_{TH} = V_{th,active} + \Theta \qquad (\Theta \leq 5kT/e)$$

$$\Rightarrow [S(\log_{10}(I_{off}(s)) - \Omega') - \gamma\,|V_{bs}|]$$

$$B \propto \frac{1}{1 + \frac{C_{dm}}{C_{ox}}} \propto \frac{1}{1+\gamma}$$



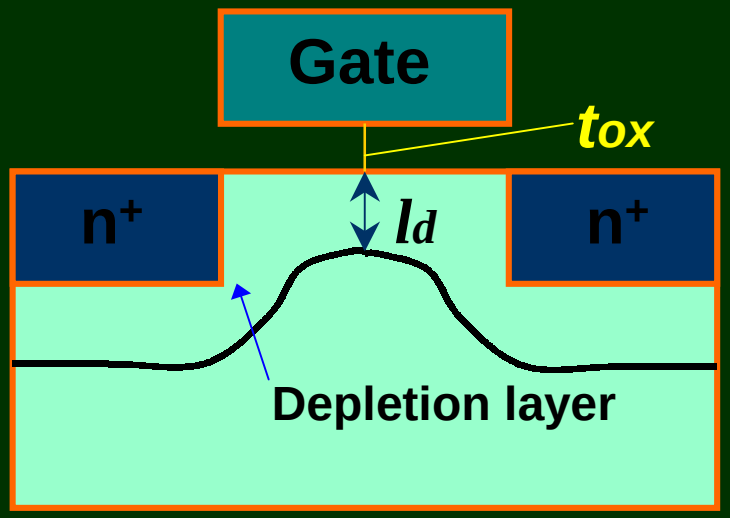
Relation between *S* factor and γ

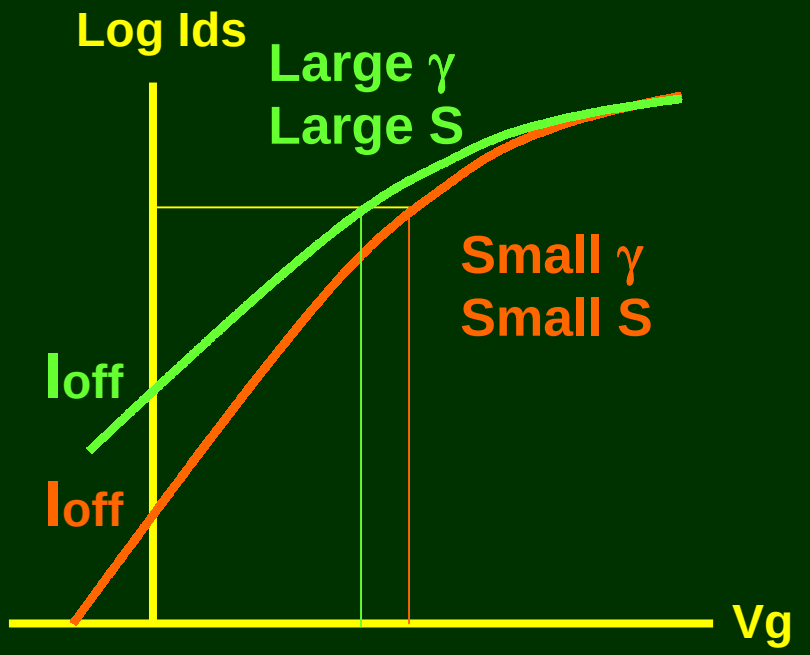
$$S = 60\left(1 + \frac{C_D}{C_{ox}}\right)$$

$$\gamma \equiv \frac{|\Delta Vth|}{|\Delta Vbs|} \propto \frac{C_D}{C_{OX}} \quad (\cong \frac{3t_{OX}}{l_D})$$

Long channel ⇒ $S \cong dS/d\gamma\,(1+\gamma)$ [mV/decade]

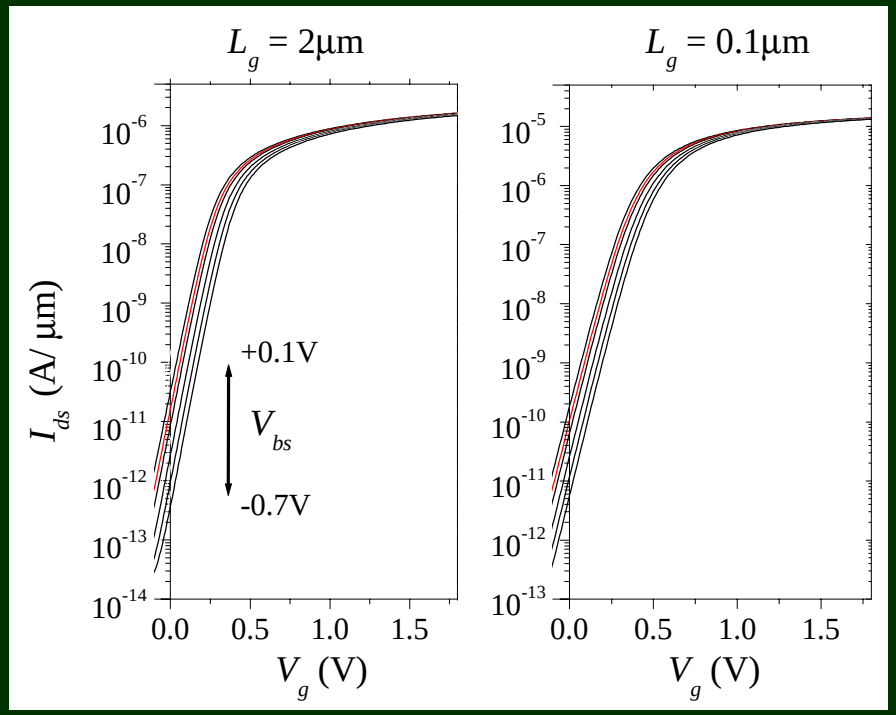
$dS/d\gamma \geq 60$

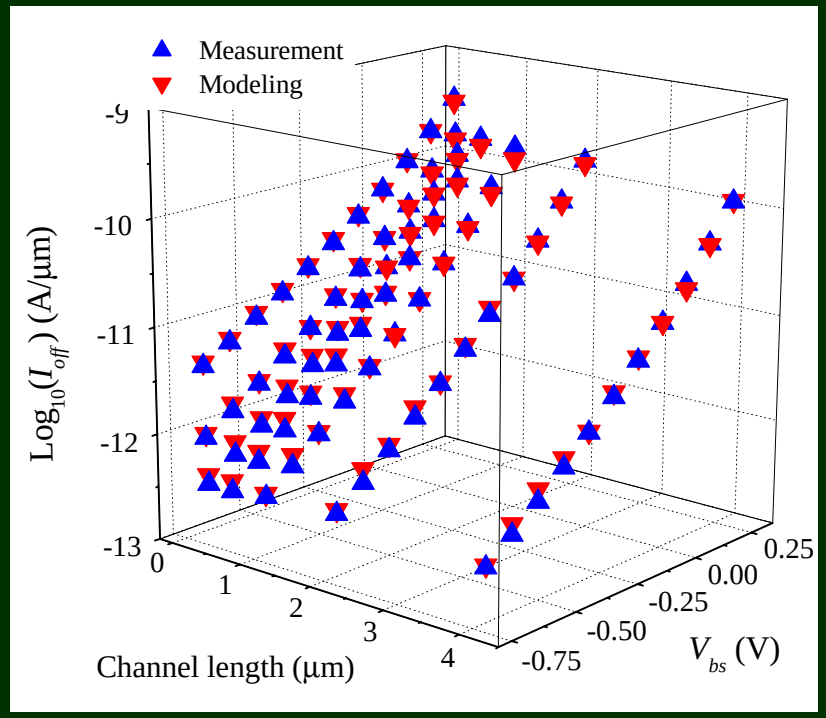




If the SCE occurs ⇒ *New* γ - *S* relation

Comparison of measured and modeled I_{off} (s)





Ids -Vg curves as a function of Vbs

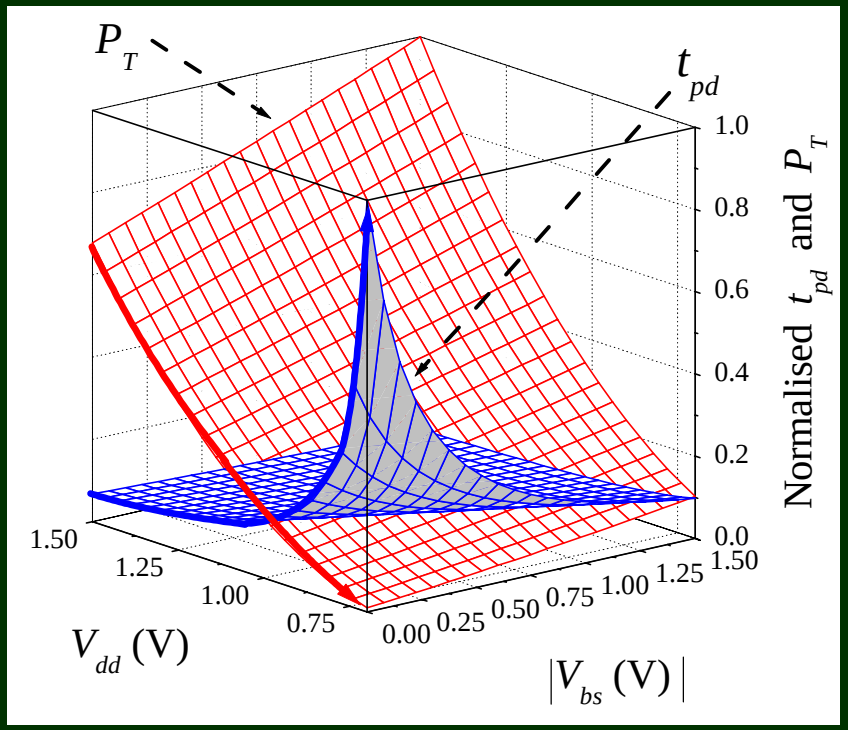
Verify

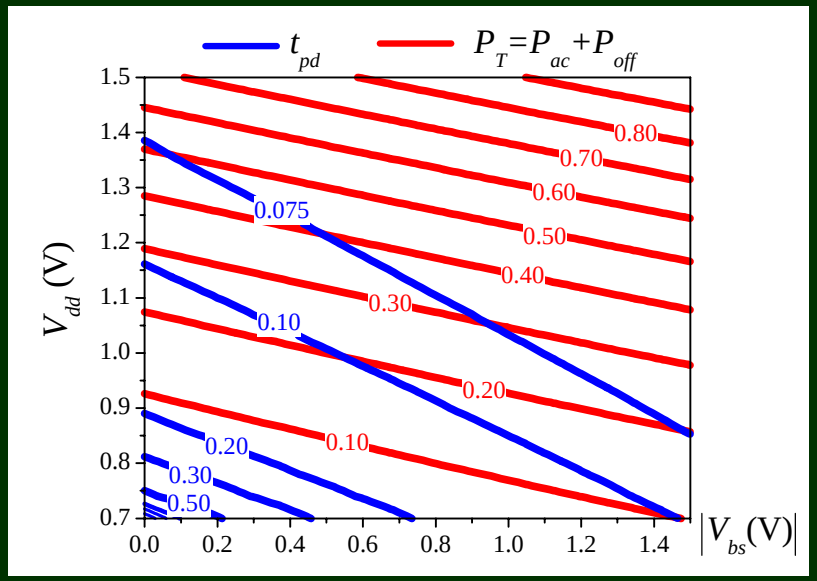
$$r = \frac{I_{off}(a)}{I_{off}(s)} \cong 10^{\frac{\gamma|Vbs|}{S}}$$

Relation between power and speed in VTCMOS

POWER **Trade-off in a normal MOSFET** **SPEED**

$$P_{total} = P_{active} + P_{static} = f\, C_{load} V_{dd}^{\,2} + I_o\, 10^{\frac{-Vth}{S}} V_{dd} \quad \Leftrightarrow \quad t_{pd} \approx \frac{C_{load} V_{dd}}{I_{on}} \propto \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

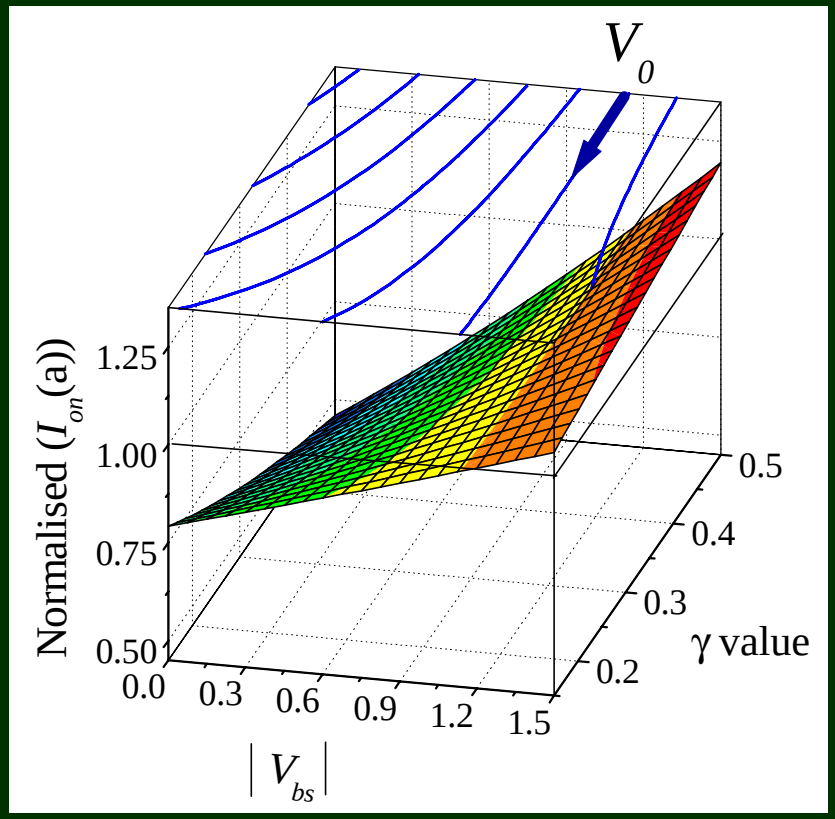


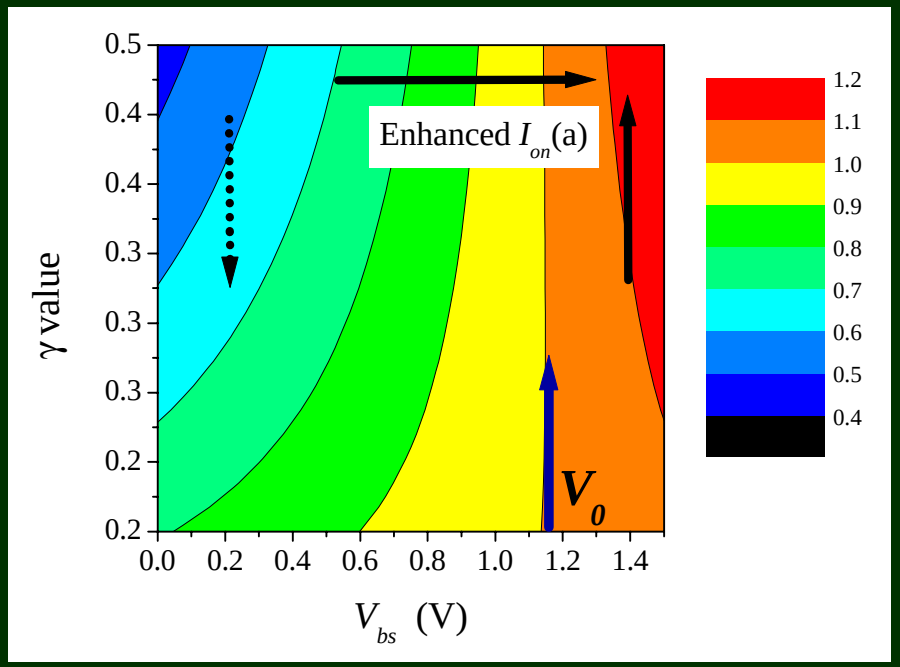


BUT, VTCMOS ⟹ **Low power and high speed**

Modeling of $I_{on}(a)$ characteristics

(I_{off} (s) = 10^{-13} A/μm and Vdd = 1.5V)



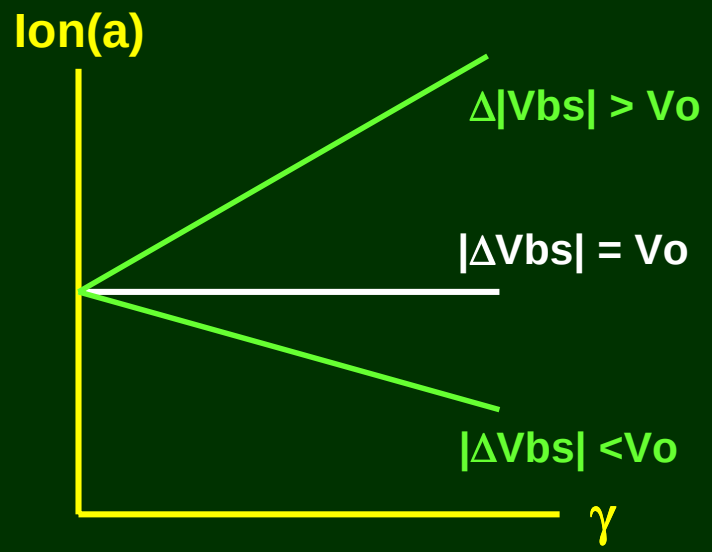


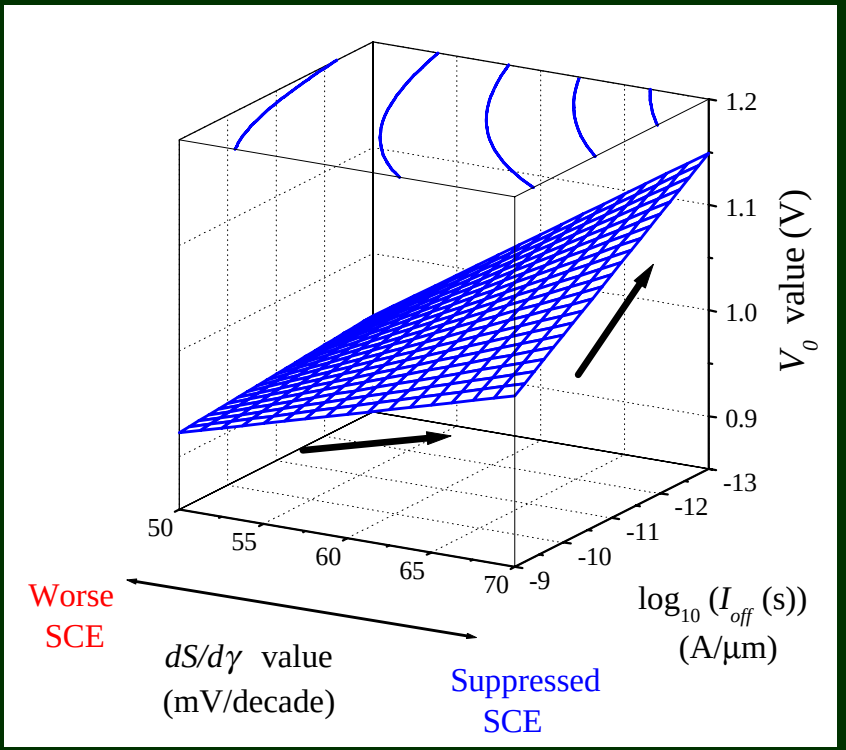
- √ **Characteristic Vbs (=Vo) exists.**
- √ **Ion(a) increases with increasing Vbs.**
- √ **If Vbs < Vo, smaller γ should be exploited.**

Interpretation of V_0

Definition of Vo: Vbs where Ion(a) is given by a constant

$$\frac{d\,\mathrm{Ion(a)}}{d\,\gamma} = 0 \Longrightarrow |Vo| = \frac{V_{dd} + (\log_{10}(I_{off}(s)^{-1}) - \Omega')[(1+\gamma)\,\alpha\, dS/d\gamma - S]}{(1+\gamma)\times\alpha - \gamma}$$





(Vdd=1.5V)

- rarely dependent on γ
- Scalability with Vdd
- Related with the SCE

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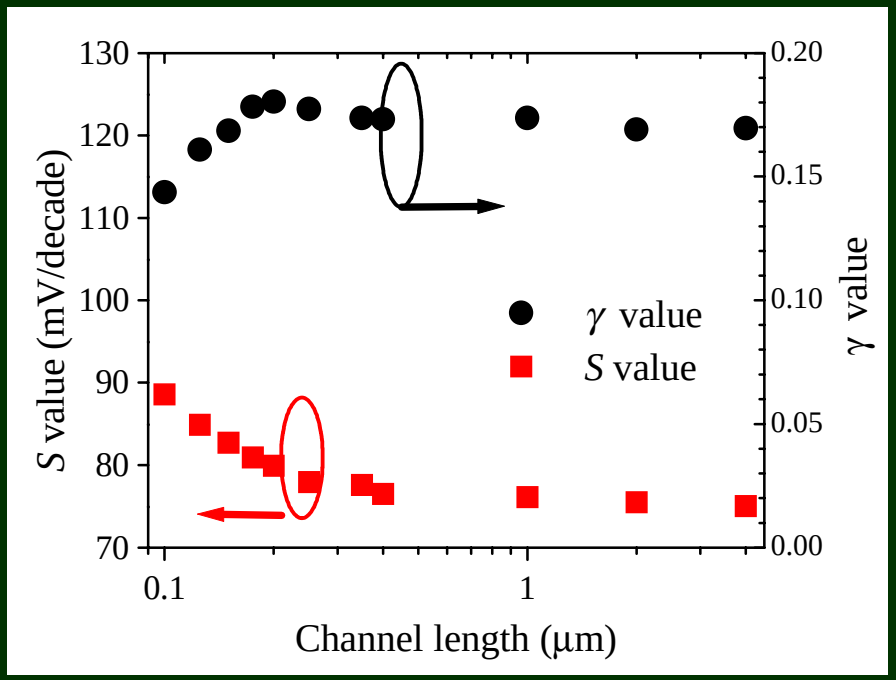
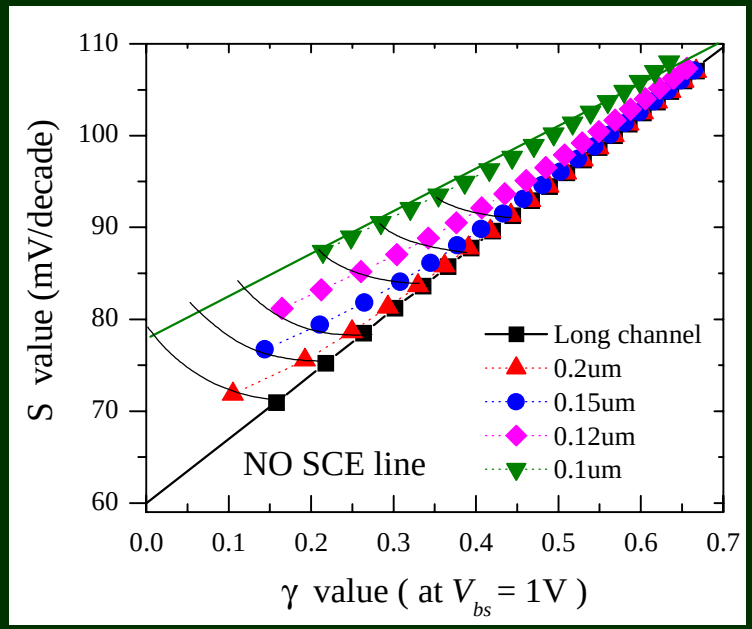
Short Channel Effect on the performance of VTCMOS

Short Channel Effect, γ decreases and *S* increases.

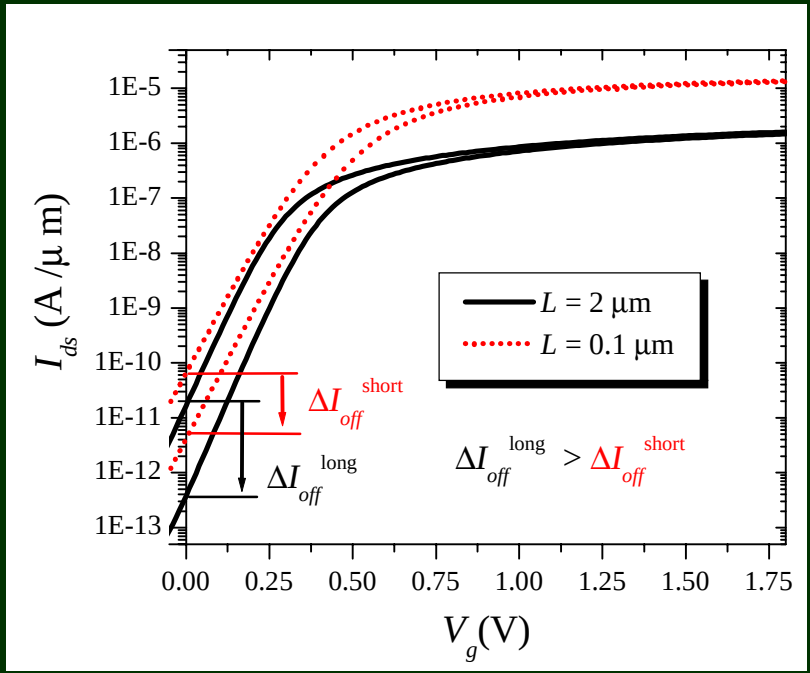
New γ - S relation

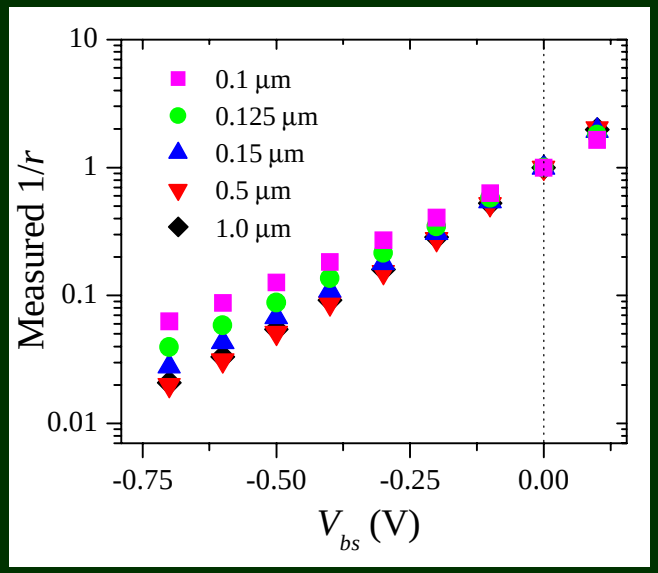




$$S = \frac{dS}{d\gamma}(\gamma - 0.8) + 115 \quad \text{(mV/decade)}$$

Short Channel Effect - Standby off current, Ioff(s)



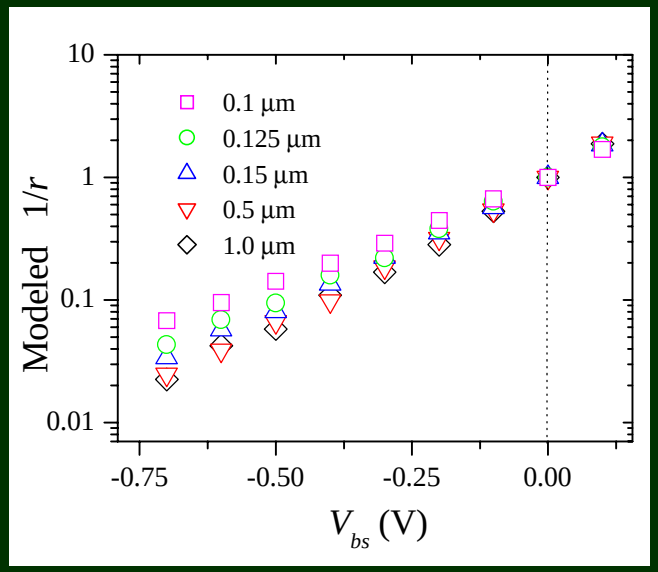


$$r = \frac{I_{off}(a)}{I_{off}(s)} \cong 10^{\frac{\gamma |Vbs|}{S}}$$

SCE ➡ Degradation of $\gamma\downarrow$ and $S\uparrow$

⬇

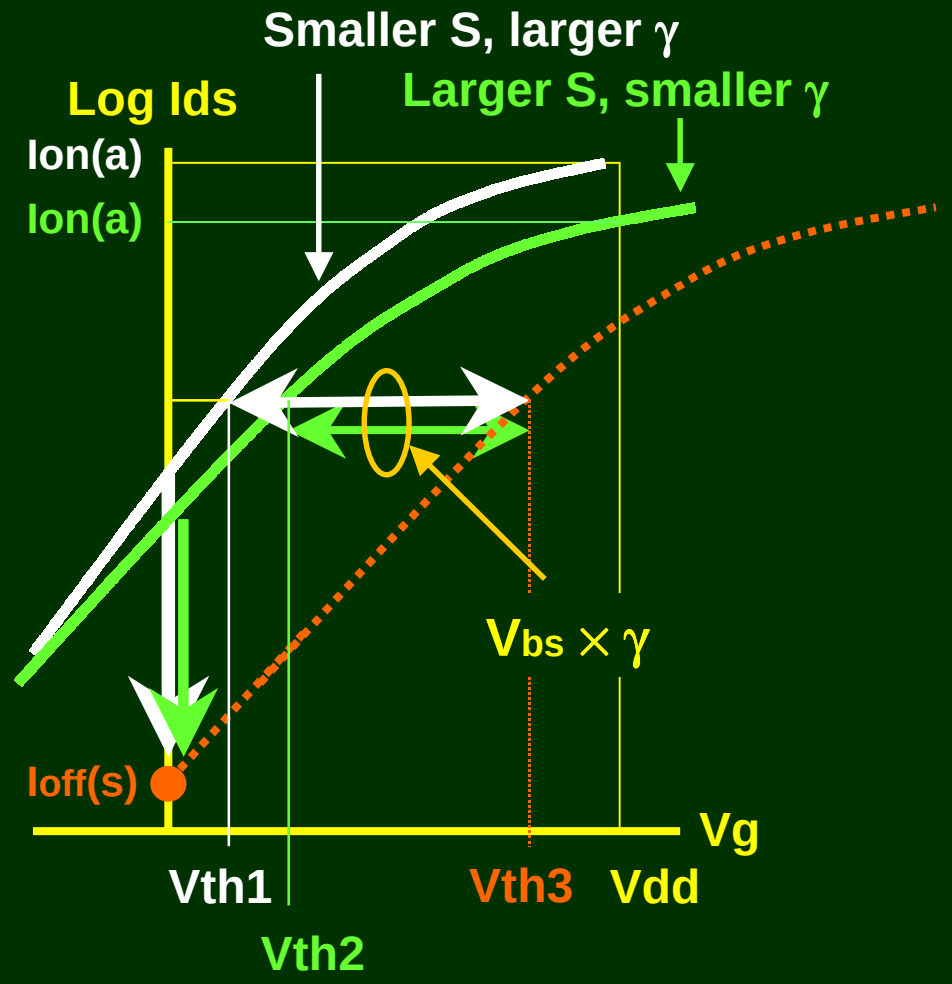
Larger 1/r (*or* Smaller Ioff(s))



Short Channel Effect – Active on current, $I_{on}(a)$

Smaller SCE

Larger SCE



$$S = \frac{dS}{d\gamma}(\gamma - 0.8) + 115 \quad \text{(mV/decade)}$$

SCE ➡ dS/dγ decreases

($\gamma^{\downarrow}$, $S^{\uparrow}$)

$$V_{TH} = [S(\log_{10}(I_{off(s)}) - \Omega') - \gamma |V_{bs}|]$$

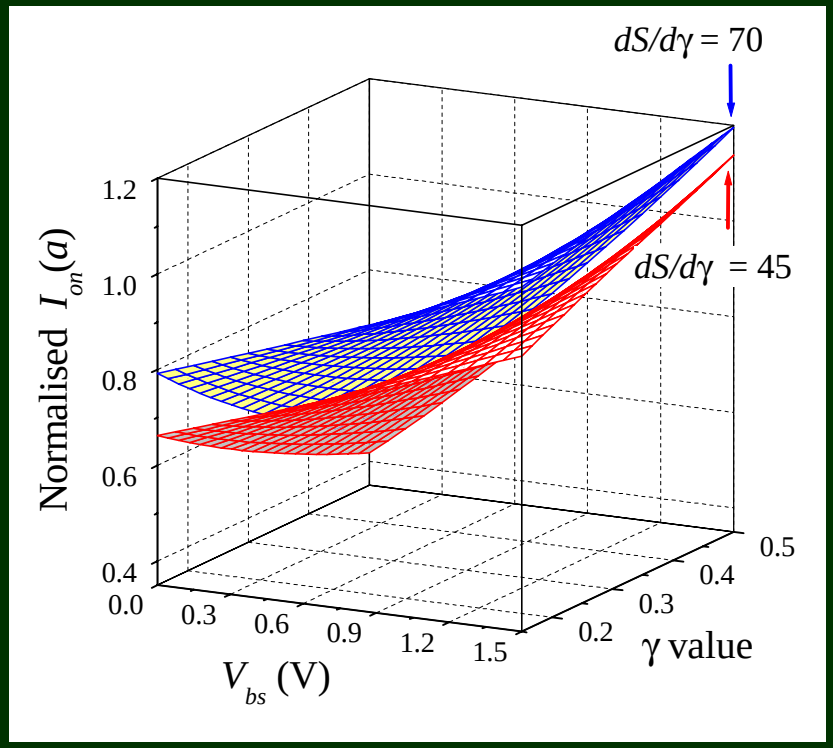
Increasing V_{TH}

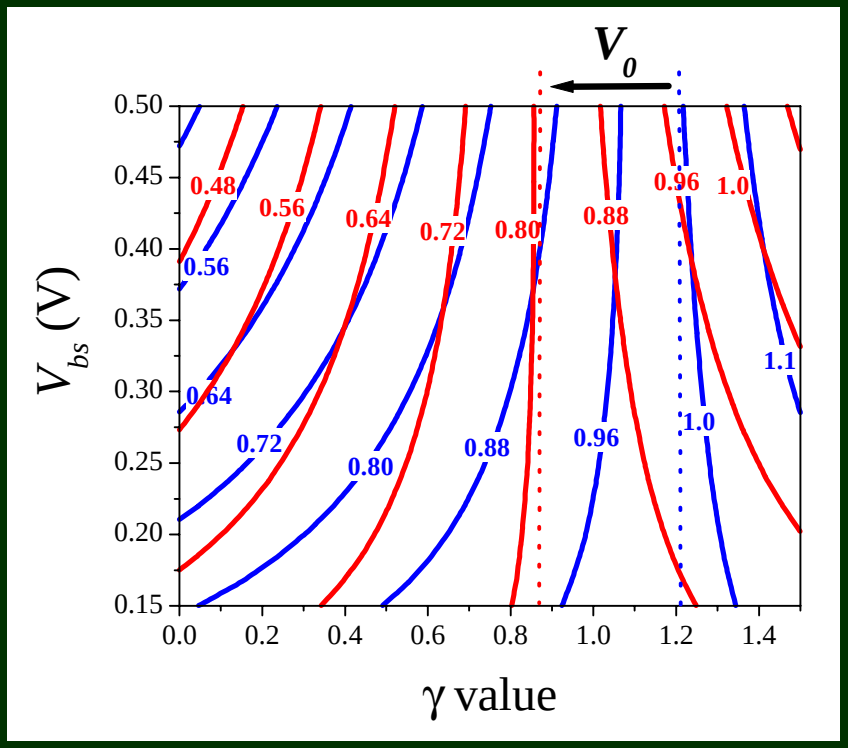
$$I_{on(a)} = B\,(V_{dd} - V_{TH})^{\alpha}$$

Decreasing $I_{on(a)}$

Short Channel Effect – Ion(a) Modeling

At $I_{off}(s)=10^{-13}$ A/μm





SCE

(γ↓, S↑)

1. To make Ion(a) Smaller.

2. To shift Vo to a lower value.

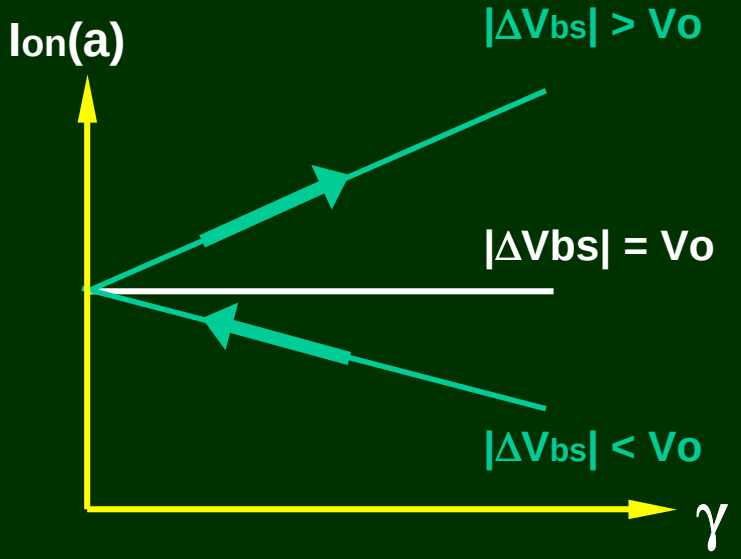
Optimum condition

(1) $|\Delta V_{bs}|$ should be set as large as the junction leakage permits.

(2) Appropriate selection of Vdd and Vbs must be made to satisfy both low $I_{off}(s)$ and high $I_{on}(a)$.

(3) When the values of γ and Vth can be designed at a fixed $|\Delta V_{bs}|$, the optimum γ depends on Vo.

- γ should be large ($|\Delta V_{bs}| > Vo$)
- γ should be small ($|\Delta V_{bs}| < Vo$)



(4) To design a VTCMOS of high performance, The following *parameters* must be larger. (suppressed SCE).

$E_{off} \equiv \Delta\gamma / \gamma - \Delta S / S$ and $E_{on} \equiv \Delta\gamma \cdot Vbs - \Delta S \cdot (I_{off}(s) - \Omega')$

Conclusions

- √ A very compact analytical VTCMOS model has been developed.
- √ VTCMOS can attain lower power than a normal CMOS at the same speed.
- √ Short Channel Effect degrades the VTCMOS' performance. SCE should be suppressed.
- √ Optimum device conditions for VTCMOS are discussed.