# Variable Threshold Voltage CMOS (VTCMOS) in Series Connected Circuits

Takashi Inukai<sup>1</sup>, Toshiro Hiramoto<sup>1,2</sup> and Takayasu Sakurai<sup>1,3</sup>

<sup>1</sup> Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan Phone: +81-3-5452-6264, Fax: +81-3-5452-6265, E-mail: inukai@nano.iis.u-tokyo.ac.jp

> <sup>2</sup> VLSI Design and Education Center, University of Tokyo <sup>3</sup> Center for Collaborative Research, University of Tokyo

# ABSTRACT

Characteristics of variable threshold voltage CMOS (VTCMOS) in the series connected circuits are investigated by means of device simulation. It is newly found that the performance degradation due to the body effect in series connected circuit is suppressed by utilizing VTCMOS. Lowering the threshold voltage ( $V_{th}$ ) enhances the drive current and alleviates the degradation due to the series connected configuration. Therefore, larger body effect factor ( $\gamma$ ) results in lower  $V_{th}$  and higher *on*-current even in the series connected circuits. These characteristics are attributed to the velocity saturation phenomenon which reduces the drain saturation voltage ( $V_{dsat}$ ).

#### **Keywords**

variable threshold voltage CMOS, series connected circuits, degradation factor, body effect factor, substrate bias, velocity saturation

#### 1. Introduction

Variable threshold voltage CMOS (VTCMOS) has recently attracted much attention for ultra-low power LSI applications at low supply voltage ( $V_{dd}$ ) [1-3]. Utilizing the body effect, the threshold voltage ( $V_{th}$ ) can be controlled by the substrate bias ( $V_{bs}$ ), which makes it possible to obtain high  $V_{th}$  in the stand-by mode and low  $V_{th}$  in the active mode in the same devices. Therefore, while *off*-current in the stand-by mode is fixed to extremely low level, *on*-current can be enhanced in the active mode, as shown in Fig. 1(a). In this study, the body effect factor ( $\gamma$ ) is defined by [4]

$$\gamma = \frac{\left|\Delta V_{th}\right|}{\left|\Delta V_{bs}\right|},\tag{1}$$

where  $\Delta V_{th}$  is the threshold voltage shift and  $\Delta V_{bs}$  is the difference of substrate bias between the active mode and standby mode. Then, threshold voltage shift ( $\Delta V_{th}$ ) is directly determined by  $\gamma$  and  $|\Delta V_{bs}|$  as expressed by

$$\Delta V_{th} = \gamma |\Delta V_{bs}| \,. \tag{2}$$

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

*ISPLED '01*, August 6-7, 2001, Huntington Beach, California, USA. Copyright 2001 ACM 1-58113-371-5/01/0008...\$5.00.



Fig. 1 (a) Schematics of VTCMOS characteristics. Utilizing the body effect, *on*-current in the active mode ( $I_{on,active}$ ) can be enhanced, while *off*-current in the stand-by mode ( $I_{off,standby}$ ) is fixed. (b)  $\gamma$  dependence of  $I_{on,active}$  with the fixed  $I_{off,standby}$ . When  $|\Delta V_{bs}|$  is larger  $V_{o}$ , lager  $\gamma$  results in higher *on*-current.

It is generally recognized that  $\gamma$  should be suppressed to obtain high *on*-current. We have found that, contrary to the general guideline, larger  $\gamma$  can attain higher *on*-current in VTCMOS when  $|\Delta V_{bs}|$  is larger than a critical substrate bias (V<sub>o</sub>), as shown in Fig. 1(b) [4]. When  $|\Delta V_{bs}|$  is small (including 0V), the device with larger  $\gamma$  has smaller *on*-current because of worse subthreshold characteristics and lower transconductance [5]. When  $|\Delta V_{bs}|$  is larger than the certain substrate bias (V<sub>o</sub>), larger  $\gamma$  results in larger *on*-current because of larger  $\Delta V_{th}$ . Therefore, when substrate bias can be applied to some extent,  $\gamma$  should be large in term of *on*current in VTCMOS.

Ref. [4] dealt with the  $\gamma$  dependence only in the single VTCMOS device. It is well known that the body effect deteriorates the circuit performance in the series connected circuits such as NAND, NOR and more complex gates. Therefore, the advantage of large  $\gamma$  in VTCMOS might be cancelled out in series connected VTCMOS. In this paper, we investigate the optimum design of  $\gamma$  by considering not only the single devices but also the series connected circuits.

This paper is organized as follows. Section 2 describes the analytical background of the performance of the series connected circuit, where important parameters that affect the *on*-current in the series connected devices are clarified. Sections 3 and 4 describe the simulation procedure and results, respectively, where larger  $\gamma$  can attain higher *on*-current even in the series connected circuits. In Sections 5, it is shown that lowering V<sub>th</sub> is very effective to enhance *on*-current in the series connected circuits. It is also found that this current enhancement in VTCMOS with low V<sub>th</sub> originates from the velocity saturation effect. Finally, Section 6 gives some conclusions.

# 2. Series Connected MOSFET Circuits

A series connected MOSFET structure (SCMS) appears in NAND, NOR and more complex gates. In this structure, some source nodes of n-MOSFETs (p-MOSFET) are not connected to the GND (VDD) lines but floating. Therefore, negative substrate bias occurs even in the active mode and deteriorates the circuit performance. Sakurai et al. have analyzed the performance of SCMS in terms of its *on*-current and derived an analytical form of reduction ratio of *on*-current in the case of  $V_{bs} = 0V$  [6]. A degradation factor (F<sub>d</sub>), which is defined as the reduction ratio of *on*-currents between the single device and the series connected circuits, is expressed analytically by

$$F_{d} \equiv \frac{I_{on}}{I_{onN}}$$

$$= 1 + \frac{1 - 1/\sqrt{2}}{1 - 1/\sqrt{2}} \frac{V_{dsat}}{V_{dd} - V_{th}} (1 + \gamma)(1 + \lambda V_{dd})(N - 1)$$

$$\approx 1 + \frac{1}{2} \alpha \frac{V_{dsat}}{V_{dd} - V_{th}} (1 + \gamma)(1 + \lambda V_{dd})(N - 1), \qquad (3)$$

where  $I_{on,N}$  is the *on*-current of the series connected circuit,  $\gamma$  is the body effect factor,  $V_{dsat}$  is the drain saturation voltage when  $V_{gs} = V_{dd}$ ,  $\alpha$  is a fitting parameter in the  $\alpha$ -power law [7],  $\lambda$  is a widely used channel-length modulation parameter which is related to the finite drain conductance in the saturated region and N is the number of series connected MOSFETs. As shown in eq.(3), larger  $\gamma$  results in larger reduction ratio and smaller *on*-currents in the series connected devices at  $V_{bs} = 0V$ . However,  $V_{th}$  is changed utilizing VTCMOS. In addition, the degradation factor has other components than the body effect and they are expected to be complicatedly related to  $\gamma$ . Therefore, the situation should be more complicated and detailed investigation is required in VTCMOS.

### 3. Simulation Procedure

# **3.1 Device structure**

The dependence of VTCMOS characteristics on the body effect factor is investigated by means of two-dimensional device simulation with a circuit analysis module [8]. Figure 2 shows schematics of the assumed device structure. Assuming an ideal step-like channel profile and changing depth and impurity concentration of the upper layer, depletion width ( $t_d$ ) and threshold voltage are independently changed [4]. The body effect factor is directly related to the depletion width and analytically expressed by

$$\gamma_{analytial} = \frac{C_d}{C_{ox}} \approx 3 \frac{t_{ox}}{t_d}, \tag{4}$$

where  $C_d$  is the depletion capacitance,  $C_{ox}$  is the oxide capacitance and  $t_{ox}$  is the gate oxide thickness. In the assumed ideal channel profile, since  $t_d$  is determined by the depth of the upper layer irrespective of  $V_{bs}$ ,  $\gamma$  becomes almost constant and  $V_{th}$  linearly changes with  $V_{bs}$  which includes positive biases as well as negative biases. Therefore, this analytical  $\gamma$  is in good agreement with the practical  $\gamma$  defined by eq.(1).

# **3.2** *On-* and *Off-*currents in the series connected circuits

In order to investigate the performance of the series connected circuits, the *on*-currents of the series connected circuits are evaluated. In this study, the *on*-current of the series connected circuit is defined as the current that flows when all the gate nodes are biased to  $V_{dd}$ . On the other hand, the *off*-current depends on the combination of all the gate voltages because of the body effect. Since the body effect always reduces the *off*-current by an increase of  $V_{th}$ , the *off*-current has its maximum value when the gate nearest to the GND lines is in the OFF state and the others are in the ON state. In this case, the *off*-current of the series connected circuits is equal to that of single devices. Therefore, the stand-by *off*-current of the single devices can be used as that of the series connected circuits.



Fig. 2 A device structure assumed in the device simulations. (a) A schematic of the structure and (b) a profile of channel. Assuming an ideal step-shape profile, the depletion width is controlled by the depth of the second layer and  $V_{\rm th}$  is controlled by the concentration and the type of dopant. A non-doped layer with 5nm thick ( $N_a = 10^{15} {\rm cm}^{-3}$ ) is inserted in order to avoid the inaccuracy of model for the dependence of mobility on the impurity concentration. Other technology parameters are as follows: gate length ( $L_g$ ) is 0.14µm, gate oxide thickness ( $t_{ox}$ ) is 3nm, source/drain junction depth ( $x_j$ ) is 50nm, and supply voltage ( $V_{dd}$ ) is 1.8V.



Fig. 3 Schematics of the series connected circuits and the definitions of (a) *on*-current and (b) *off*-current.

#### 4. Simulation Results

#### 4.1 Single devices

Figure 4 shows the dependence of *on*-current in the active mode on the body effect factor at fixed  $I_{off,standby}$  of  $10^{-13}$  A/µm. As shown in Fig. 4(a), the optimum  $\gamma$  depends on the applied substrate bias ( $|\Delta V_{bs}|$ ) in the single devices. When  $|\Delta V_{bs}|$  is smaller than a certain value  $V_o$  (~0.9V), larger  $\gamma$  results in the lower  $I_{on,active}$ . This is due to the degraded subthreshold

characteristics, which results in higher threshold voltage, and the degraded transconductance. On the other hand, when  $|\Delta V_{bs}|$  is larger than  $V_o$ , larger  $\gamma$  can make the threshold voltage much lower in the active mode, which results in higher  $I_{on,active}$ , while keeping the  $I_{off,standby}$  constant.



Fig. 4 The dependence of the active *on*-currents on the body effect factor in VTCMOS. (a) Single device (N = 1) and (b) series connected circuit (N = 3). In each case, the threshold voltage is adjusted so that the stand-by *off*-current is fixed to  $10^{-13}$ A/µm with given  $|\Delta V_{\rm bs}|$ .

#### 4.2 Series connected circuits

Although the critical voltage  $V_o$  becomes a little high (~1.0V), the series connected circuits have the same tendency as the single devices, which is shown in Fig. 4(b). Therefore, even in the case of the series connected circuits,  $\gamma$  should be large in terms of active *on*-current, when  $|\Delta V_{bs}|$  is large enough. It is surprising that the larger body effect is useful in the series connected circuit because the body effect has been believed to deteriorate its performance. Therefore, as mentioned in Section 2, other effects that enhance the performance by VTCMOS are expected in the series connected circuits. In the following section, the characteristic of the series connected circuits and the effect of VTCMOS are revisited in detail.

# 5. Discussion

#### 5.1 Effects of the series connected configuration

Figure 5 shows the dependence of the active on-current on the number of the series connected MOSFETs (N). When  $|\Delta V_{bs}|$  is 0V or small (Fig. 5(a) and (b)), the on-current is lower with larger  $\gamma$  irrespective of N. On the other hand, when  $|\Delta V_{bs}|$  is large enough (Fig. 5(c)), the on-current is higher with larger  $\gamma$ irrespective of N. In addition, the difference of on-currents varies with N and  $|\Delta V_{hs}|$ . Figure 6 shows the dependence of the degradation factor on N. As expected from eq.(3), the degradation factor linearly increases with N and its slope depends on the  $\gamma$  and  $|\Delta V_{hs}|$ . It is interesting to notice that the degradation factor has the similar dependence on  $\gamma$  to the *on*-current of the single devices. When  $|\Delta V_{bs}|$  is small, larger  $\gamma$  results in larger degradation. On the other hand, when  $|\Delta V_{bs}|$  is large enough, larger  $\gamma$  results in smaller degradation. Figure 7 shows the dependence of the slope of the degradation factor on  $\gamma$ . As  $|\Delta V_{bs}|$ increases, the slope decreases in each  $\gamma$  value. In addition, there is another critical substrate voltage  $V_0^*$  (~1.2V). When  $|\Delta V_{bs}|$  is smaller than  $V_o^*$ , larger  $\gamma$  results in larger degradation. On the other hand,  $|\Delta V_{bs}|$  is larger than  $V_o^*$ , larger  $\gamma$  results in smaller degradation. Since  $V_0^*$  is higher than  $V_0$  of the single devices,  $V_0$ becomes higher in the case of the series connected circuits.



Fig. 5 The dependence of the active *on*-current on the number of the series connected MOSFETs. (a)  $|\Delta V_{bs}| = 0V$  (normal MOSFET), (b)  $|\Delta V_{bs}| = 0.7V$  and (c)  $|\Delta V_{bs}| = 1.5V$ .



Fig. 6 The dependence of the degradation factor on the number of the series connected MOSFETs. (a)  $|\Delta V_{bs}| = 0V$  (normal MOSFET), (b)  $|\Delta V_{bs}| = 0.7V$  and (c)  $|\Delta V_{bs}| = 1.5V$ .



Fig. 7 The dependence of the slope of the degradation factor  $(\mathbf{f}_d)$  on the body effect factor.

# 5.2 Effect of lowering threshold voltage

Since one of the most importance features of the VTCMOS is the threshold voltage shift, the above-mentioned characteristic of the degradation factor is expected to be related to threshold voltage. Therefore, in order to investigate the effect of the threshold voltage shift, the dependence of the degradation factor on the threshold voltage is evaluated, which is shown in Fig. 8. As the threshold voltage decreases, the degradation factor decreases irrespectively of  $\gamma$  value. Therefore, the decrease of the threshold voltage utilizing VTCMOS is effective in terms of not only an enhancement of on-current of single devices but also the reduction of the degradation factor. As y increases, threshold voltage in the active mode ( $V_{\text{th,active}})$  decreases and when the  $|\Delta V_{\text{bs}}|$ is large, lager  $\gamma$  results in lower V<sub>th,active</sub>, as shown in Fig. 9. This is the reason why the degradation factor is smaller with larger  $\gamma$ value when  $|\Delta V_{bs}|$  is large. Figure 10 shows the dependence of the degradation factor on the body effect factor with the contour lines of the threshold voltage. It is clearly found that larger  $\gamma$  results in lower  $V_{\text{th,active}}$  and smaller degradation.



Fig. 8 The dependence of the slope of the degradation factor on the threshold voltage. In each  $\gamma$  value, as the threshold voltage decreases, the slope decreases.



Fig. 9 The dependence of the threshold voltage in the active mode  $(V_{th,active})$  on the body effect factor. When  $|\Delta V_{bs}|$  is large, larger  $\gamma$  results in lower  $V_{th,active}$ .



Fig. 10 The dependence of the slope of the degradation factor on the body effect factor. Contour lines of the threshold voltage are also shown.

#### 5.3 Effect of velocity saturation

In order to analyze the reduction of the degradation factor, characteristics of the single devices are revisited. Figure 11 shows the  $I_d\mbox{-}V_{ds}$  characteristics in devices with various  $V_{th}\mbox{'s}$  but the same  $\gamma$  value. It is found that  $I_d$  has relatively small drain saturation voltage (V\_{dsat}) and V\_{dsat} increases only slightly as  $V_{th}$ decreases, which is shown in Fig. 12. On the other hand, since lowering  $V_{th}$  results in an increase of gate drive ( $V_{dd}$ - $V_{th}$ ), the ratio of  $V_{dsat}$  to  $V_{dd}$ - $V_{th}$ , which appears in eq.(3), decreases as  $V_{th}$ decreases. And it is also found that this reduction corresponds to the reduction of the slope in Fig. 8. It is due to well-known velocity saturation phenomenon. In longer channel devices, the saturation voltage is determined by the pinch-off of the channel and changes roughly proportionally to the gate drive. However, as the gate length becomes smaller, the velocity saturation would determine the drain saturation voltage and the dependency of  $\boldsymbol{V}_{\text{dsat}}$ on  $V_{\text{th}}$  weakens, resulting in the alleviation of the degradation factor. This channel length dependence is clearly shown in Figs. 13 and 14 and corresponding tendencies of the degradation factor are obtained for each gate length, as shown in Fig. 15. Therefore, the reduction of the degradation factor in the series connected circuits with reduced  $V_{th}$  is attributed to weak dependency of  $V_{dsat}$ on V<sub>th</sub> because of the velocity saturation phenomenon.



Fig. 11  $I_d$ - $V_{ds}$  characteristics of devices with various  $V_{th}$ 's and the same  $\gamma$  value ( $\gamma = 0.15$ ).  $V_{dsat}$  in each device is shown by a dot.



Fig. 12 The  $V_{th}$  dependence of the saturation voltage  $(V_{dsat})$  and ratio of  $V_{dsat}$  to gate drive  $(V_{dd}\text{-}V_{th})$ . As  $V_{th}$  decreases,  $V_{dsat}$  increases only slightly, resulting in reduction of the ratio.



Fig. 13 The dependence of  $V_{dsat}$  on  $V_{th}$  for devices with various gate lengths. Comparison with an analytical form for the long channel devices is also shown.  $V_{dsat}$  varied linearly with  $V_{th}$  in long channel devices. On the other hand,  $V_{dsat}$  remains almost constant in short channel devices due to velocity saturation.



Fig. 14 The dependence of the ratio of  $V_{dsat}$  to  $V_{dd}$ - $V_{th}$  for devices with various gate lengths. Comparison with an analytical form for the long channel devices is also shown. The ratio rapidly decreases with  $V_{th}$  in short channel devices compared with long channel devices.



Fig. 15 The dependence of the slope of the degradation factor on  $V_{th}$  for devices with various gate lengths.

#### 6. Conclusions

We have investigated the characteristics of VTCMOS in the series connected circuits in terms of the body effect factor and the *on*current. Even in the case of the series connected circuits, large  $\gamma$ results in larger *on*-current if the substrate bias can be applied to some extent. This is because lower threshold voltage results in not only enhanced *on*-current of the single devices but also reduced degradation factor. This threshold voltage dependence of the degradation factor is attributed to the velocity saturation phenomenon, which determines the drain saturation voltage. Unlike long channel devices, the drain saturation voltage becomes less sensitive to the threshold voltage. Consequently, VTCMOS is effective for improving the performance of the series connected circuits.

#### Acknowledgements

This work was partly supported by the Japan Society for the Promotion of Science (JSPS) Research for the Future Program and by the Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology. The device simulator (Medici<sup>TM</sup>) has been supplied through VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Avant! Corporation.

#### References

- [1] T. Kuroda, T. Fujita, S. Mita, T. Nagamatsu, S. Yoshioka, K. Suzuki, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu and T. Sakurai: "A 0.9V, 150-MHz, 10-mW, 4 mm<sup>2</sup>, 2-D discrete cosine transform core processor with variable threshold- voltage (VT) scheme", *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1770-1779, 1996.
- [2] Y. Oowaki, M. Noguchi, S. Takagi, D. Takashima, M. Ono, Y. Matsunaga, K. Sunouchi, H. Kawaguchiya, S. Matsuda, M. Kamoshida, T. Fuse, S. Watanabe, A. Toriumi, S. Manabe and A. Hojo: "A sub-1µm circuit design with substrate-overbiasing", *ISSCC Digest of Technical Papers*, pp. 88-89, 1998.
- [3] H. Mizuno, K. Ishibashi, T. Shimura, T. Hattori, S. Narita, K. Shiozawa, S. Ikeda and K. Uchiyama: "A 18µA-Standby-Current 1.8V 200MHz Microprocessor with Self Substrate-Biased Data-Retention Mode", *ISSCC Digest of Technical Papers*, pp. 280-281, 1999.

- [4] H. Koura, M. Takamiya and T. Hiramoto: "Optimum Conditions of Body Effect Factor and Substrate Bias in Variable Threshold Voltage MOSFETs", *Jpn. J. Appl. Phys.*, vol. 39, pp. 2312-2317. 2000.
- [5] T. Hiramoto and M. Takamiya: "Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias", *IEICE Trans. Electron.*, vol. E83-C, pp. 161-169, 2000.
- [6] T. Sakurai and A. R. Newton: "Delay Analysis of Series-Connected MOSFET Circuits", *IEEE Journal of Solid-State Circuits*, vol. 26, pp. 122-131, 1991.
- [7] T. Sakurai and A. R. Newton: "Alpha-Power Law MOSFET Model and its Application to CMOS Inverter Delay and Other Formulas", *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 584-594, 1990.
- [8] Medici Ver.4.1, Avant! Corp., 1998.