Transmission Line Models and Overshoots of On-chip Interconnects

ダナルドノ　ドゥイ　アントノ　　**桜井貴康**
Danardono Dwi Antono　　Takayasu Sakurai

東京大学　生産技術研究所
Institute of Industrial Science,　The University of Tokyo

1. Introduction

Similar to the resistance and capacitance of interconnect line, the inductance is distributed over the wire. A distributed *RLC* model of a wire, known as transmission line model, becomes the most accurate approximation of the actual behavior of interconnect. In this paper, we discuss about transmission line models for doing simulation with circuit simulator and overshoots of on-chip interconnects, as one phenomena caused by inductance effect of interconnects.

2. Transmission line models and overshoots

To simulate the behavior of transmission line with circuit simulator, usually a distributed *R(L)C* interconnect is represented by connecting numbers of lumped *R(L)C* elements. Various lumped elements could be used here, however, π ladder circuit, as shown in Fig.1, is known to be a good approximation. Also, to get the better approximation, one single line should be divided into more sections. However, sometimes it results in unnecessary simulation time and accuracy.

A distributed *RLC* line should be calculated/evaluated by using telegrapher's equations instead of transfer function of *n*-lumped *RLC* elements. *HSPICE* circuit simulator provides the *real* transmission line model, called as *W* model. *W* model interconnects could be determined by inserting resistance, inductance, capacitance per unit length, and the length of interconnects. Fundamentally, higher-*n*-lumped-*RLC*-elements approximates the *W* model better. However, there is possibility that the former one causes spurious ringing, which cannot be neglected as shown in Fig.2.

Overshoot is important to examine, due to its possibility to threaten the reliability of circuit. In the following sub-sections, first, it is discussed overshoots on optimized buffered *RLC* interconnects. Then, a brief discussion of overshoots on general circuits is summarized.

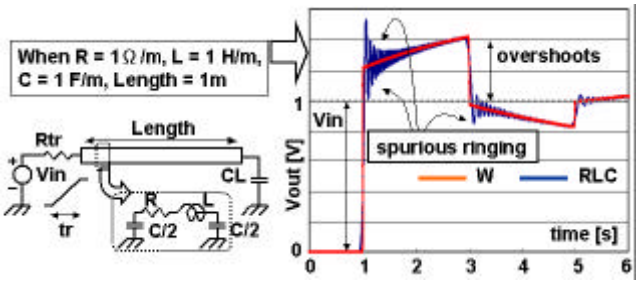

Fig.1. Distributed *RLC* int.　　Fig.2 Overshoots and ringing

2.1. *RLC* optimized buffered interconnects

In the previous work [2], it was discussed that for such a long line, inserting buffers results in decreasing of time propagation delay of distributed *RLC* line. For local lines, the difference of total propagation delay (*%Incr*) between buffered distributed *RLC* line and buffered distributed *RC* line is less than 1.5 when W < 10Wo. Where *W*, and *Wo* are interconnect width, and the minimum one, respectively. For semiglobal and global lines, *%Incr*<10 (when *W*<10*Wo*), and *%Incr*<10 (*W*<3*Wo*), respectively.

Applying the same data used in [2], transient response simulations of optimized *RLC* on-chip interconnects are employed using *HSPICE* circuit simulator. Note that no overshoot observed for optimized buffered *RLC* local interconnects, while some results for the global ones are listed as followings.

Table 1: Vin + Overshoot [V], global, tech. node (TN) [nm], Vin=V,W=aWo,Wo=425nm,Rtr=Ro/b, Ro=26kΩ, min CL (right)

Optimized buffered RLC					TN:130,a=20, length [mm]			
TN	a=2	a=4	a=10	a=20	b	0.2	1	5
130	1.03	1.12	1.15	1.20	800	1.49	1.43	1.38
90	1.01	1.07	1.12	1.18	600	1.35	1.31	1.28
60	1.00	1.02	1.07	1.14	400	1.13	1.12	1.11
40	1.00	1.01	1.03	1.07	200	1.00	1.00	1.00

2.2. General circuits

Transient response of a single distributed *RLC* interconnect depends on the values of driver resistance, interconnects and load capacitance. It is difficult to give such a rule of thumb whether overshoots occur for general circuits. However, overshoots becomes more difficult to occur, especially when 1) longer rise time (*tr*); 2) smaller driver (narrower transistor gate width, bigger driver resistance); 3) narrower interconnect width; are used. Note that global interconnect also suffers from overshoots more easily than local one, and as scaling of technology continues, by keeping *Vin* constant, overshoot becomes lower.

3. Summary

It is recommended to apply telegrapher's-equations-based transmission line model, instead of connecting lumped *RLC* elements for modeling transmission line, due to its advantages, such as exact analytical solution and no spurious ringing. Overshoots, which are affected by lots of points, however, occur more easily as faster switching speeds and wider interconnect are used. This work also shows that global interconnects suffers from overshoots (due to inductance effect) much more than local ones.

4. References

[1] Star-Hspice manual, chapter 17, Avant!, 1999.

[2] Danardono Dwi Antono, and Takayasu Sakurai, "Inductance Effect on VLSI Interconnections," **電子情報通信学会，基礎境界ソサイエティ大会講演論文集** P.61, Sept. 2001.