14th German-Japanese Forum on IT 2002/4/30
Working group program: Semiconductor

Low-power LSI
- Through cooperation among levels -

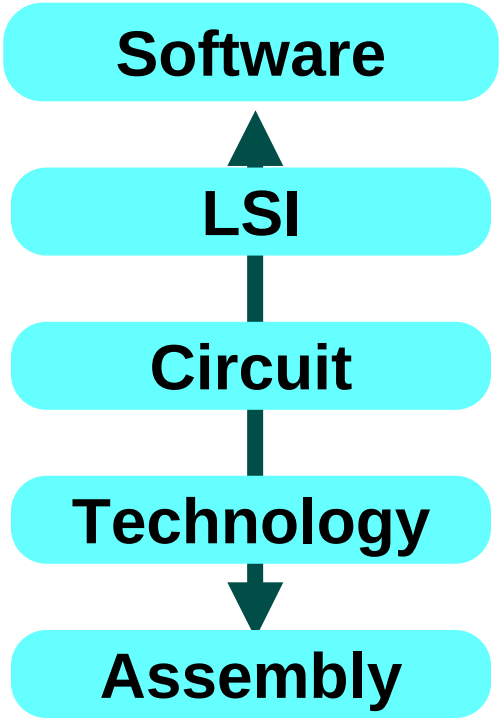
Prof. Takayasu Sakurai

**Center for Collaborative Research,
and Institute of Industrial Science,
University of Tokyo
E-mail: tsakurai@iis.u-tokyo.ac.jp
http://lowpower.iis.u-tokyo.ac.jp/**

Outline

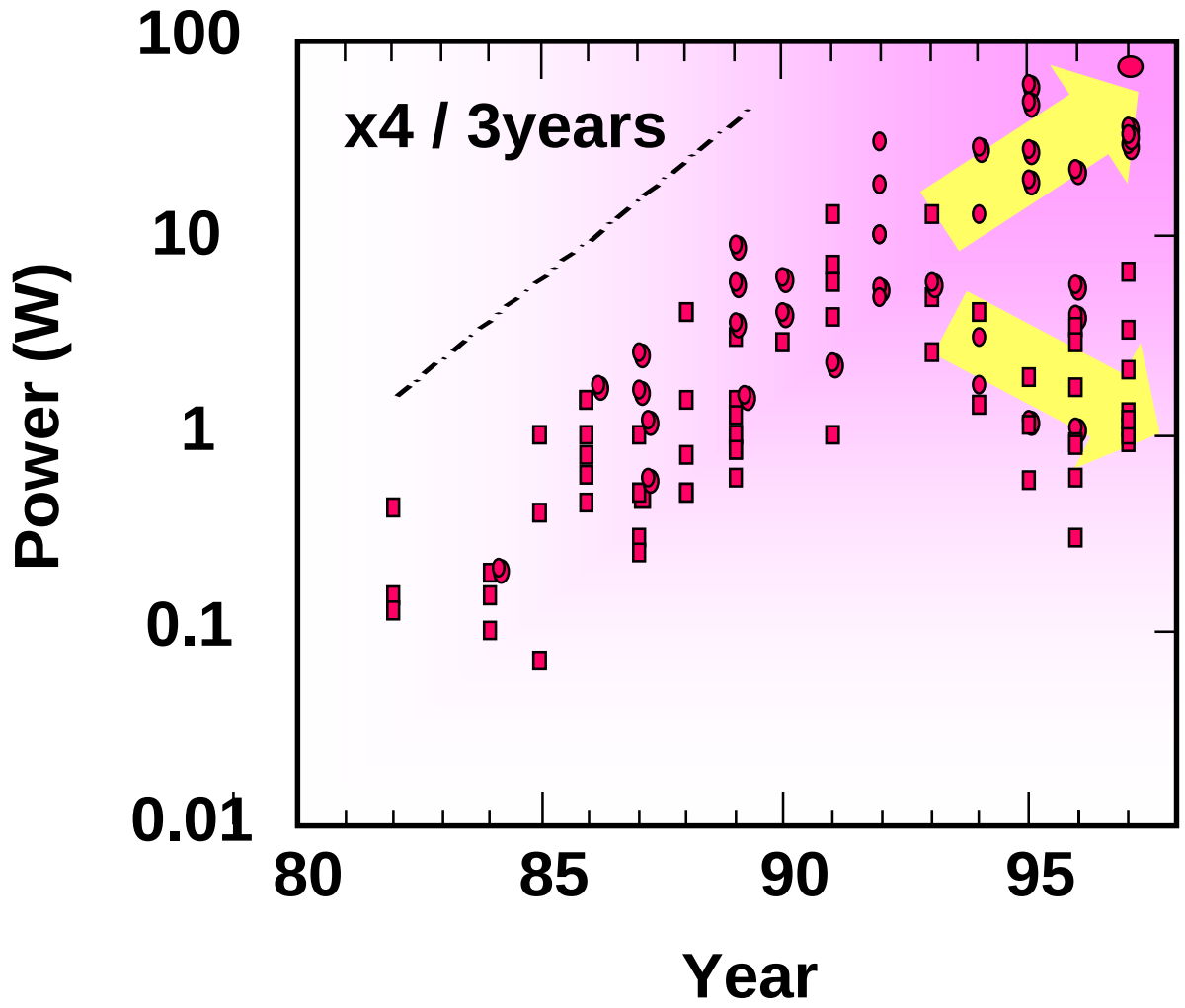
Low-power LSI - Through cooperation among levels -

- Introduction
- Technology - Circuit cooperation : Boosted Gate MOS (BGMOS)
- Software - LSI cooperation : VDD / VTH-hopping
- LSI – Assembly cooperation: Superconnect technology
- Summary

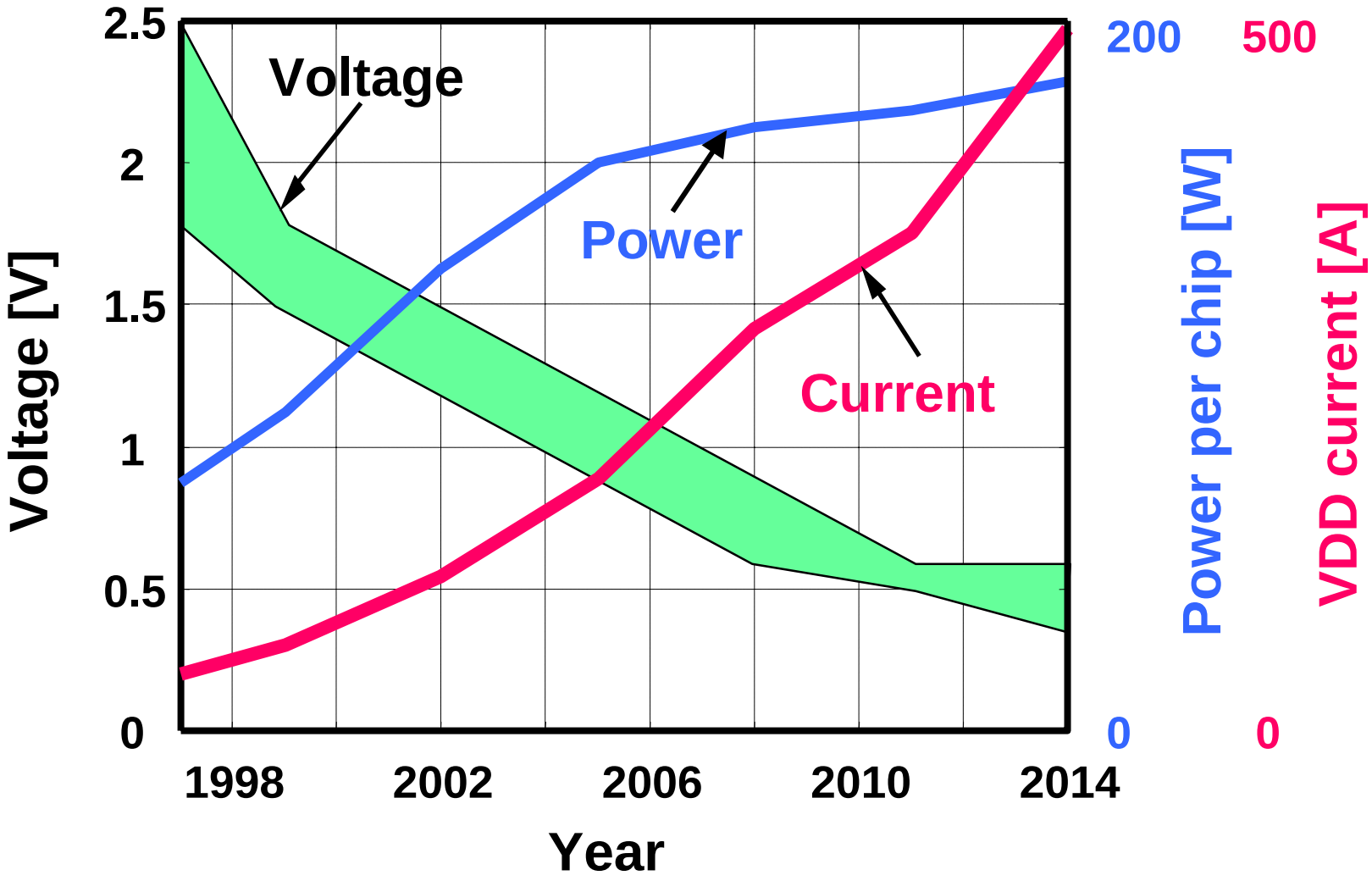


Ever increasing VLSI power

(Power consumption of processors published in ISSCC)



V_{DD}, power and current trend



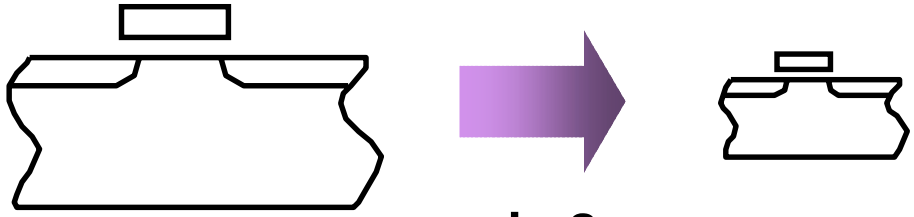
International Technology Roadmap for Semiconductors 1999 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA) , Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

T.Sakurai

Necessity for low-power design

Power range	Concerns	Typical applications (All need high-perf.)
< 0.1W	• Battery life	Portable • PDA • Communications
~ 1W	• Inexpensive package limit • System heat (10W / box)	Consumer • Set-Top-Box • Audio-Visual
> 10W	• Ceramic package limit • IR drop of power lines	Processor • High-end MPU's • Multimedia DSP's

Scaling law predicts power increase



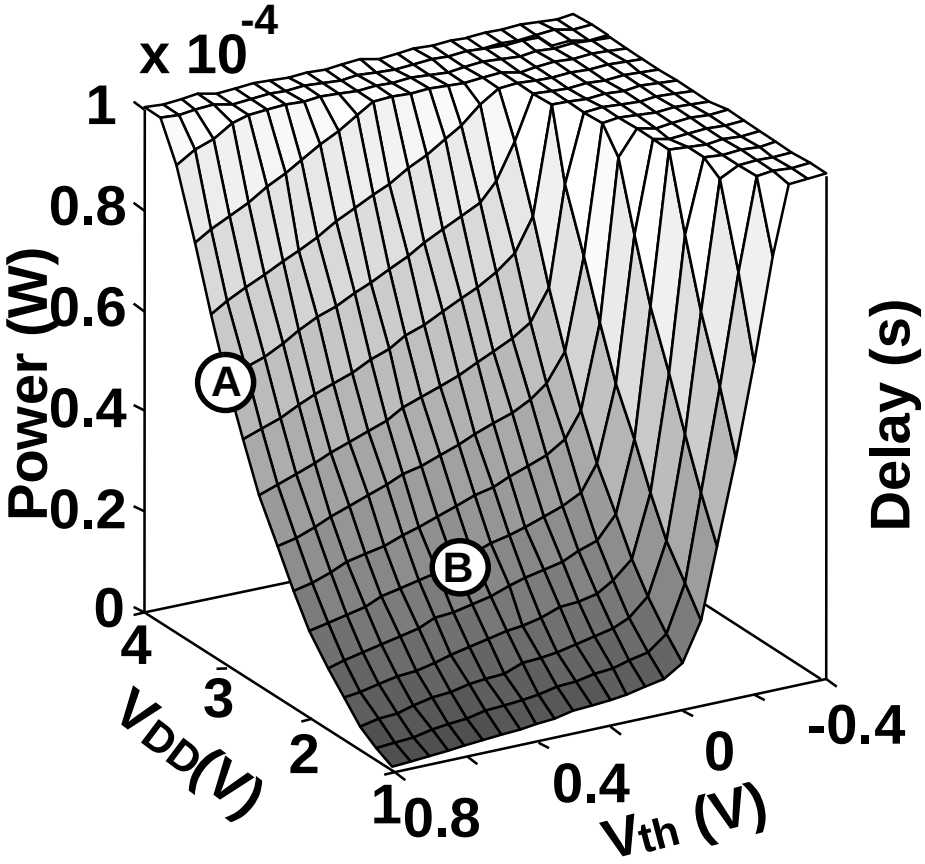
k=2

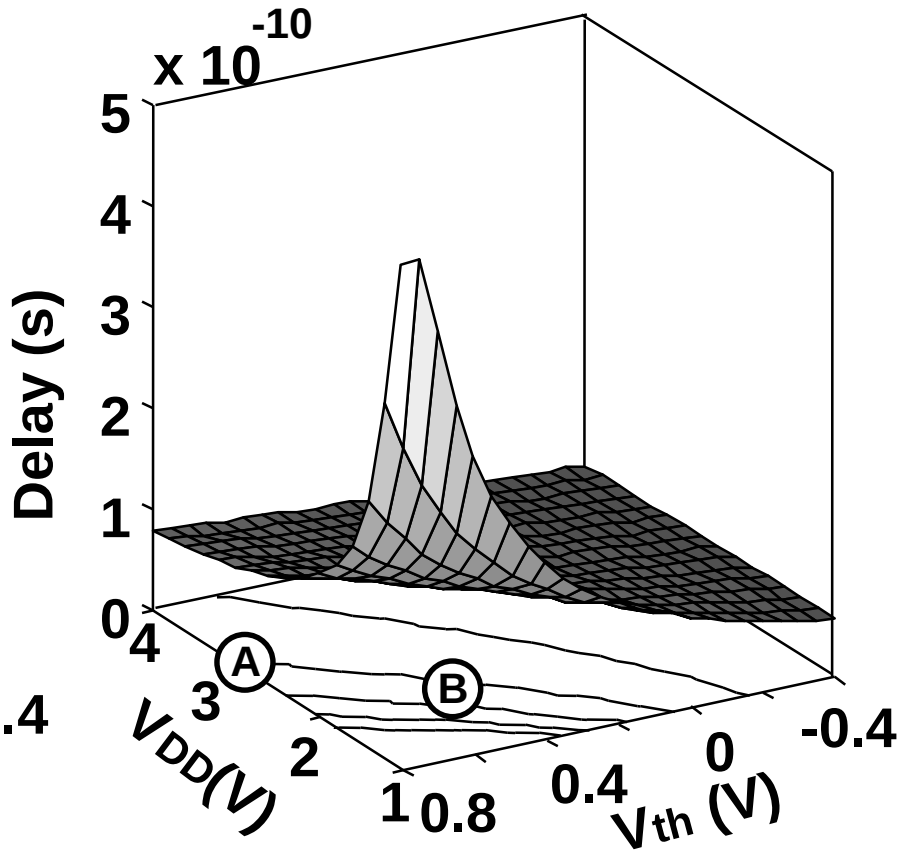
Transistors		Scaling coefficients
V_{DD}	[V]	1/k
Tr. dimensions	[x]	1/k
Tr. current	[I~1/x x/x V^1.3]	$1/k^{0.3}$
Tr. capacitance	[C~1/x xx]	1/k
Tr. delay	[d~CV/I]	$1/k^{1.7}$ (=0.3 when k=2)
Tr. power	[P~VI~CVV/d]	$1/k^{1.3}$
Power density	[p~P/x/x]	$k^{0.7}$ (=1.6 when k=2)

Power & delay dependence on V_{DD} & V_{TH}

Power : $P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{th}}{S}} \cdot V_{DD}$

Delay $= \frac{k \bullet Q}{I} = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{th})^{\alpha}}$ $(\alpha=1.3)$





Controlling V_{DD} and V_{TH} for low power

Low power → Low V_{DD} → Low speed → Low V_{TH} → High leakage → V_{DD}-V_{TH} control

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

Software-hardware cooperation

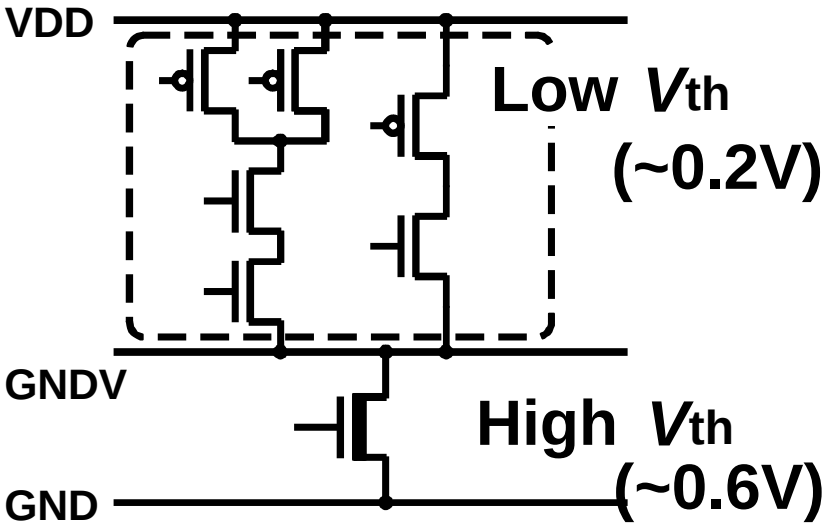
Technology-circuit cooperation

*) MTCMOS: Multi-Threshold CMOS

*) VTCMOS: Variable Threshold CMOS

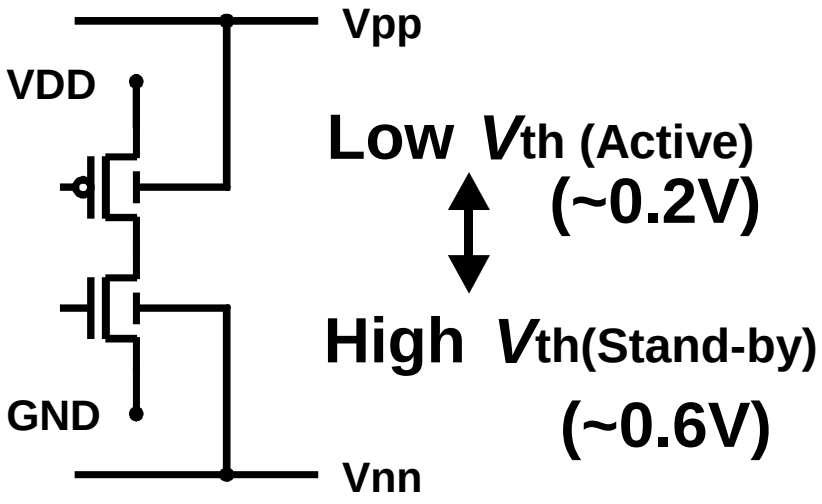
- Multiple : spatial assignment
- Variable : temporal assignment

Previous circuit schemes



MTCMOS [1]

- Tunneling leakage cannot be cut-off.
- Area penalty increases when VDD < 1V.

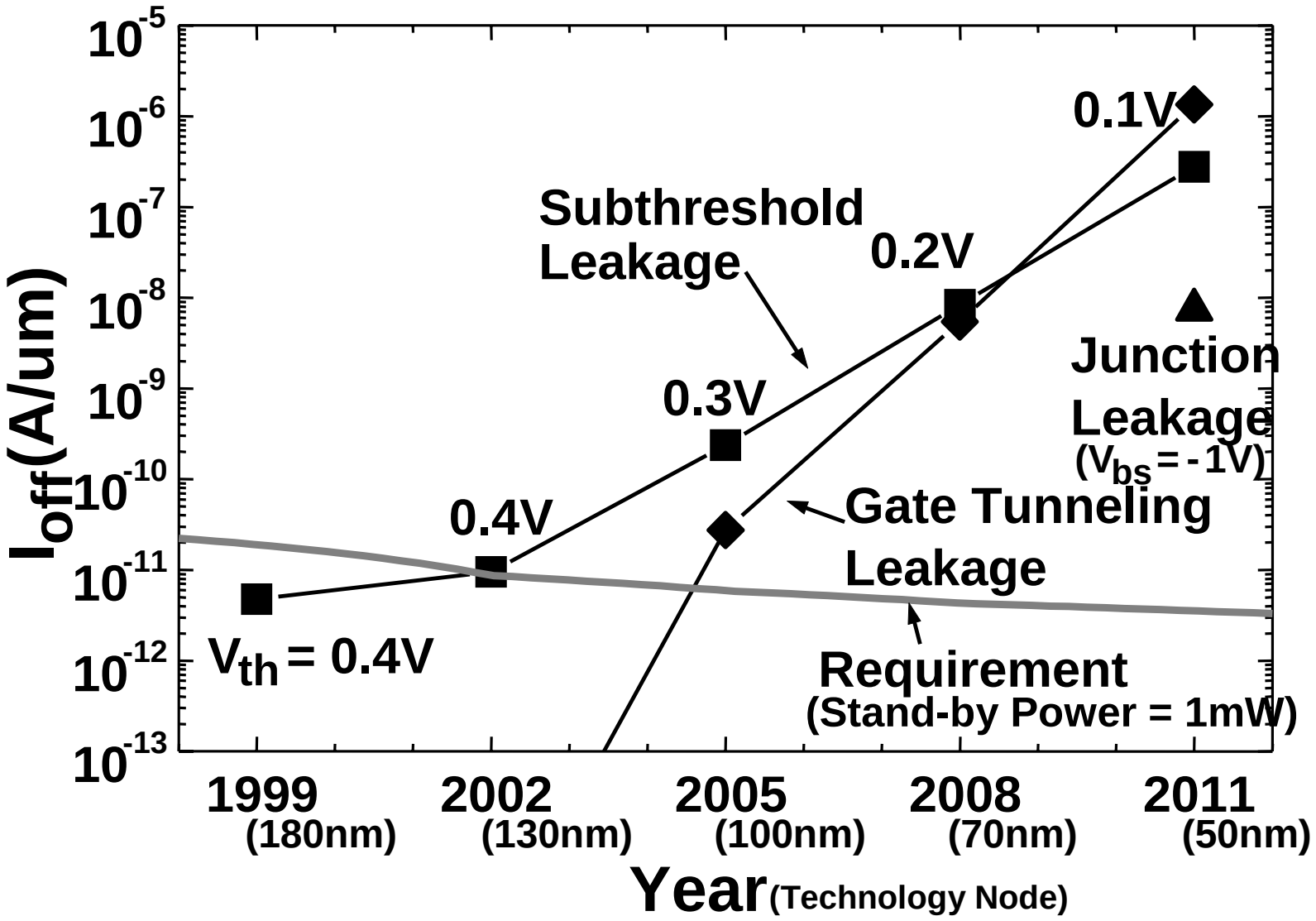


VTCMOS [2]

- Junction leakage increases due to band-to-band tunneling.
- Tunneling leakage is not suppressed.

[1] S.Mutoh *et al*. IEEE, JSSC, 1995. [2] T.Kuroda *et al*. IEEE, JSSC, 1996.

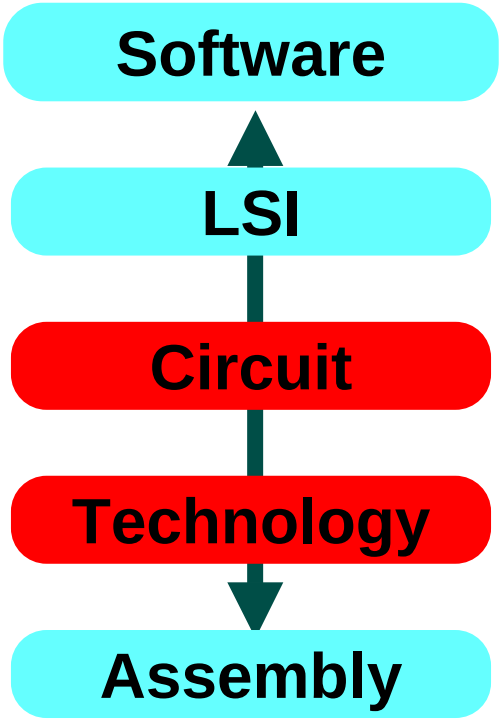
Transistors go leaky



Outline

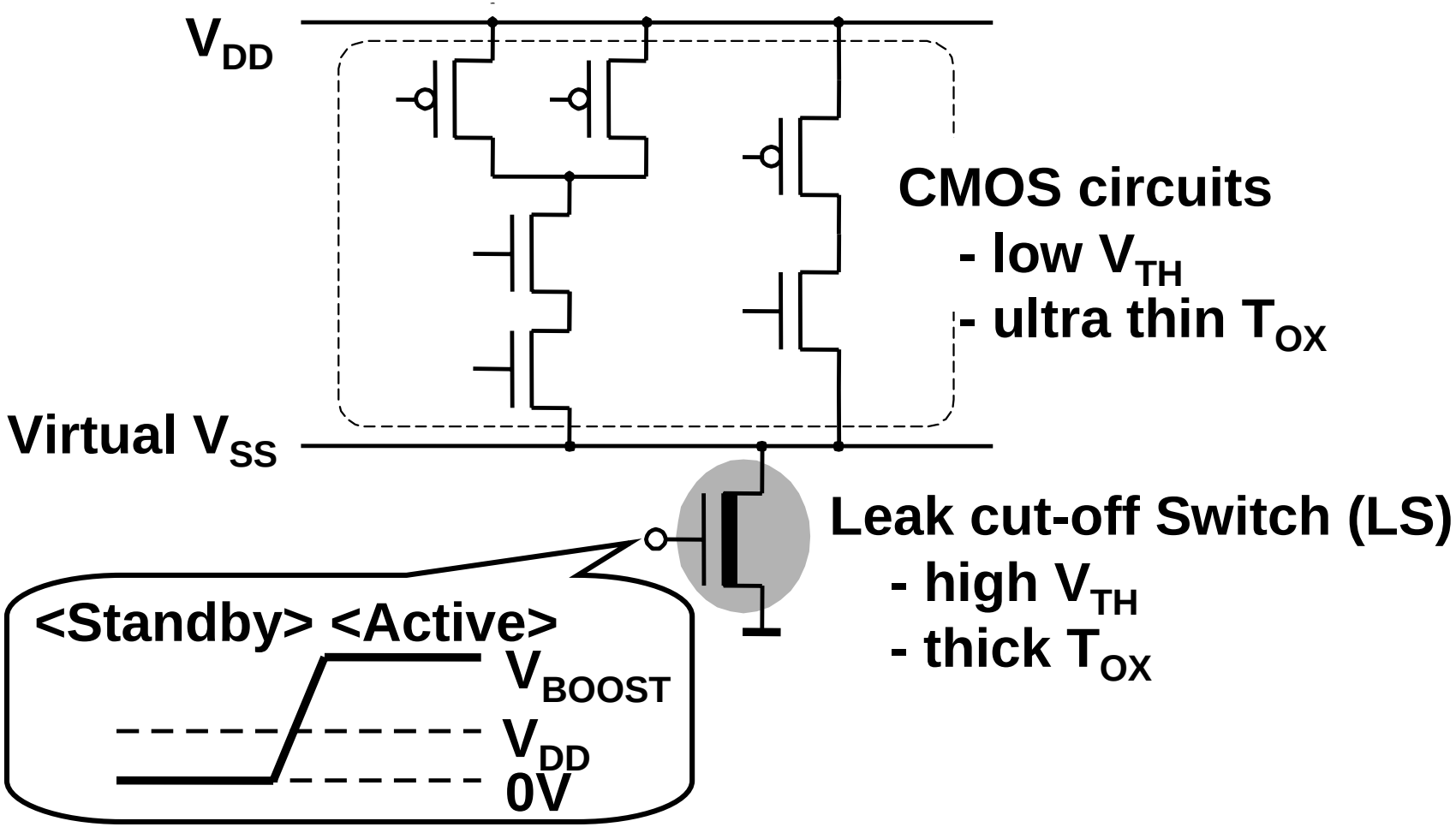
Low-power LSI - Through cooperation among levels -

- Introduction
- Technology - Circuit cooperation : Boosted Gate MOS (BGMOS)
- Software - LSI cooperation : VDD / VTH-hopping
- LSI – Assembly cooperation: Superconnect technology
- Summary



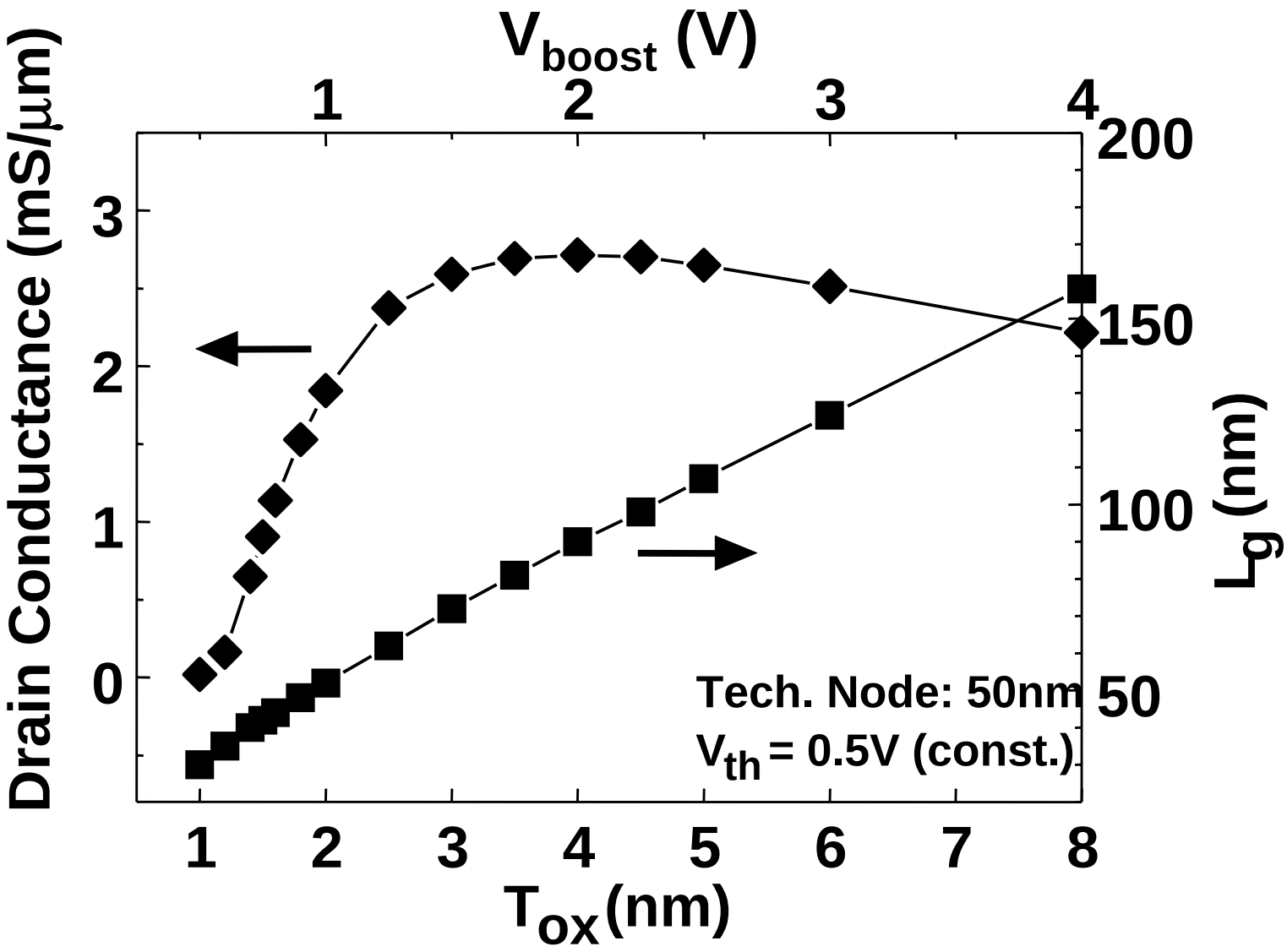
Boosted-Gate MOS (BGMOS)

Technology-Circuit cooperative approach

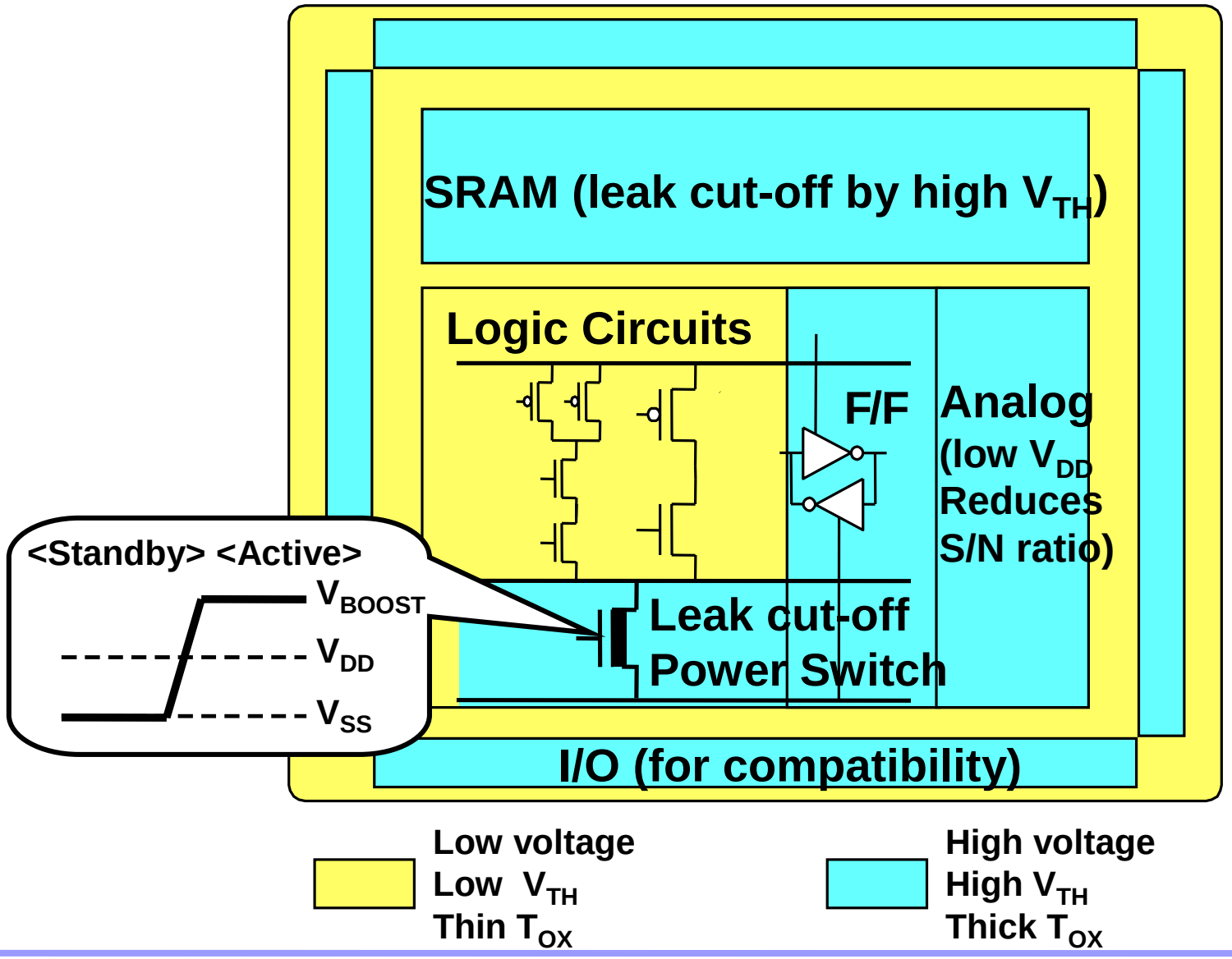


T.Inukai, M.Takamiya, K.Nose, H.Kawaguchi, T.Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC'00, p.409, May 2000.

Leak switch optimization



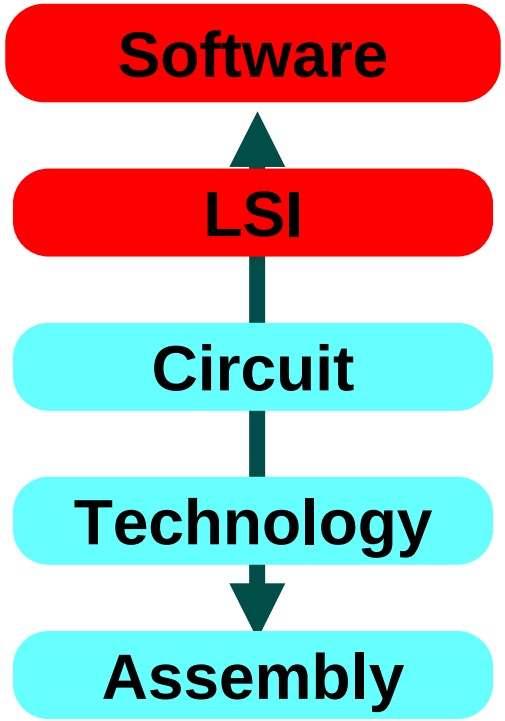
GSI's in deep-submicron era



Outline

Low-power LSI - Through cooperation among levels -

- Introduction
- Technology - Circuit cooperation : Boosted Gate MOS (BGMOS)
- Software - LSI cooperation : VDD / VTH-hopping
- LSI – Assembly cooperation: Superconnect technology
- Summary



Controlling V_{DD} and V_{TH} for low power

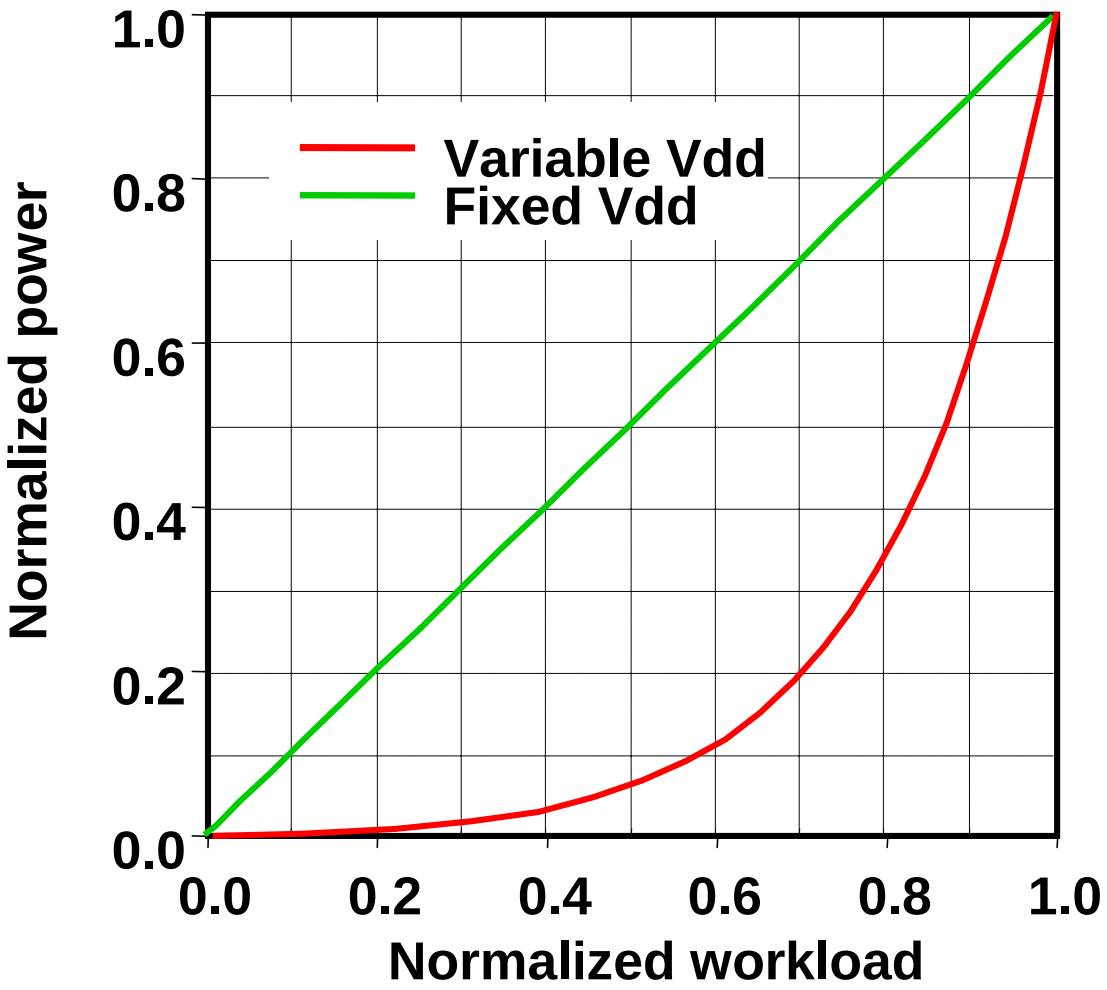
- Software-Hardware cooperation -

	Active	Stand-by
Multiple V_{TH}	Dual-V_{TH}	MTCMOS
Variable V_{TH}	V_{TH} hopping	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	Boosted gate MOS
Variable V_{DD}	V_{DD} hopping	

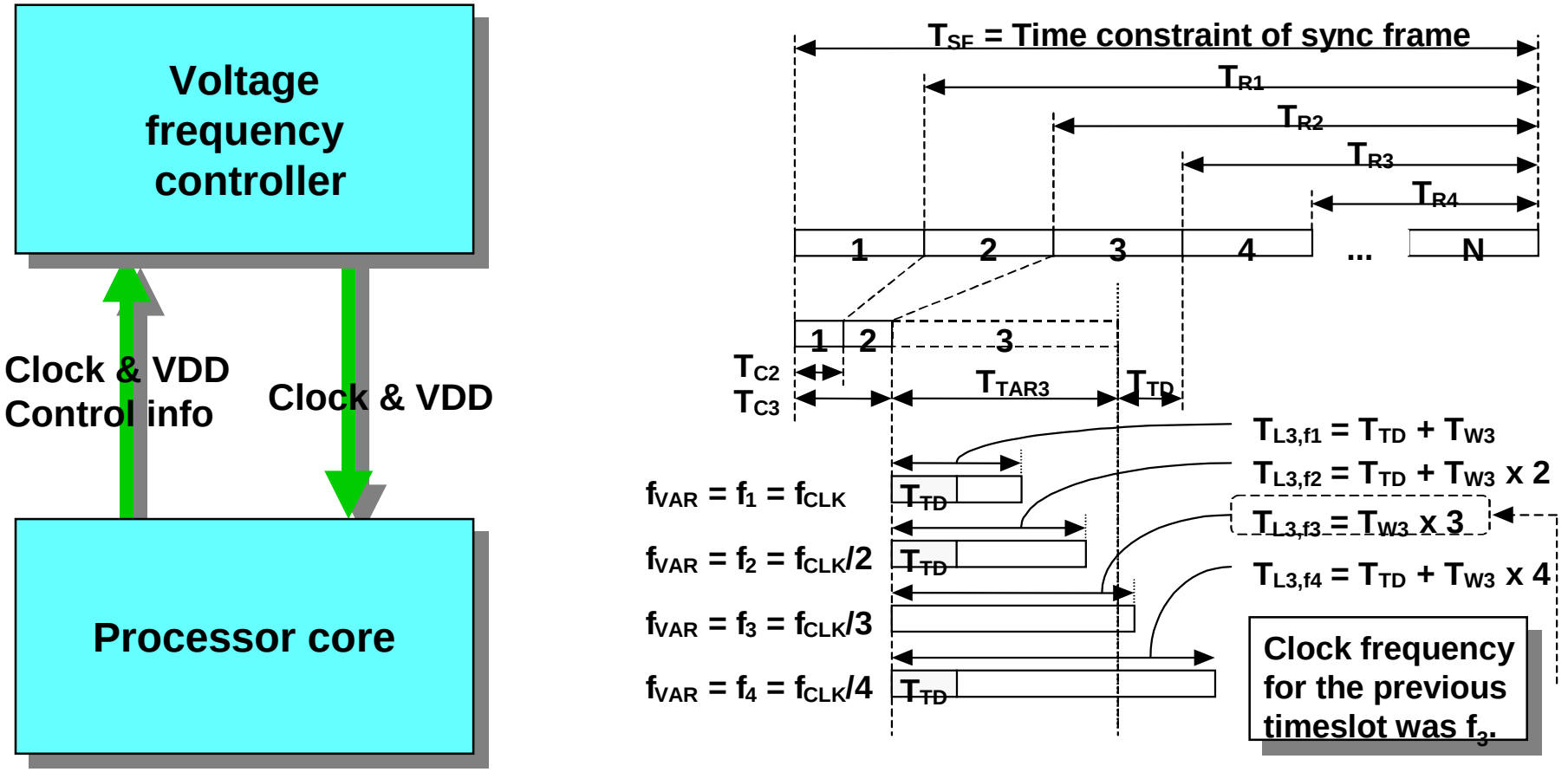
If you don't need to hussle, V_{DD} should be as low as possible

Energy consumption is proportional to the square of V_{DD}.

V_{DD} should be lowered to the minimum level which ensures the real-time operation.



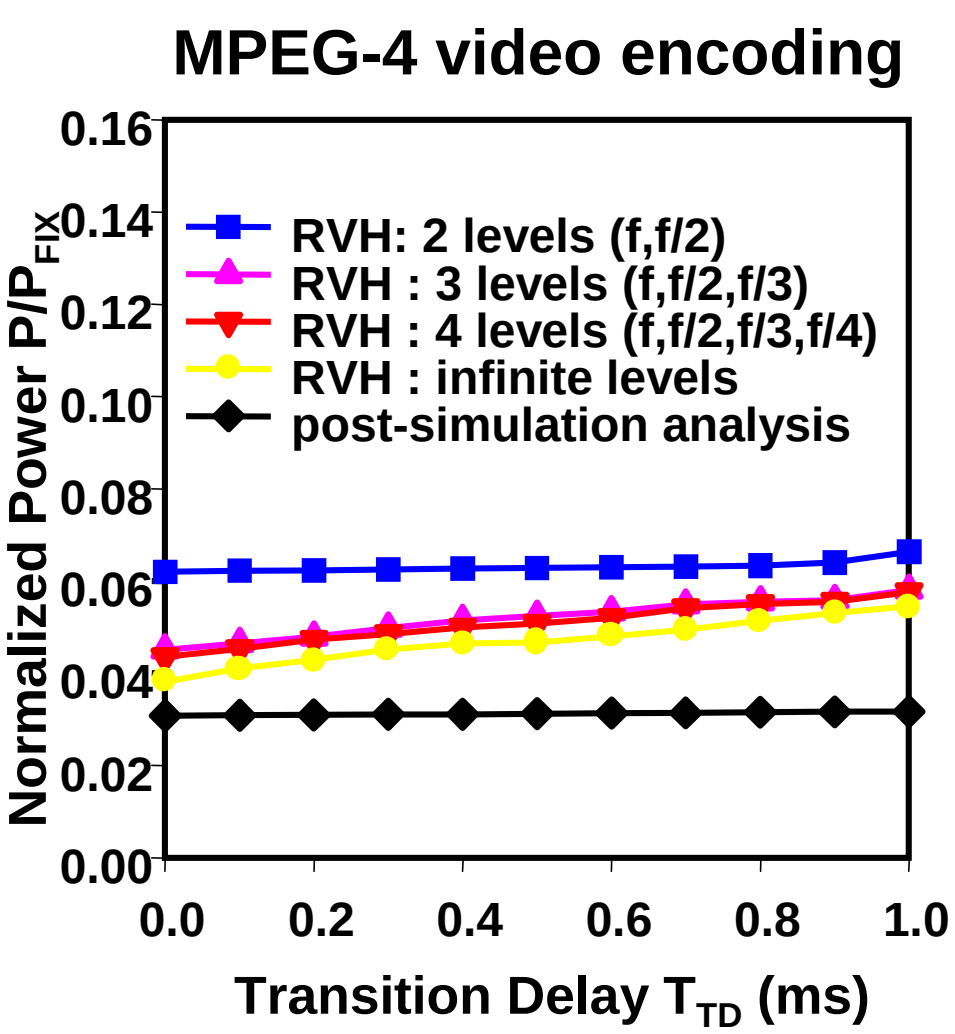
Application slicing and software feedback loop in Voltage Hopping

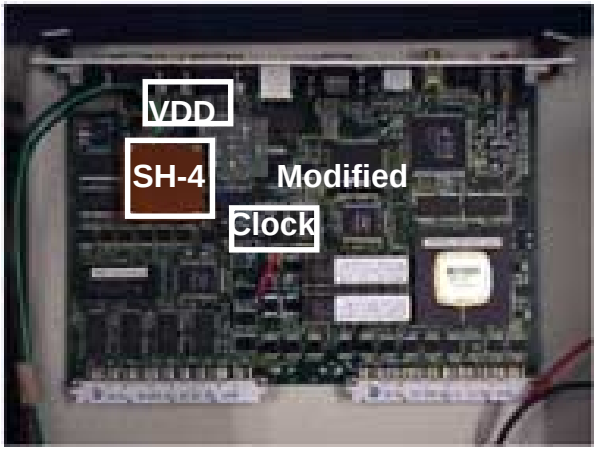


S.Lee and T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications,"ASPDAC'00, A5.2, pp.381~pp.386, Jan. 2000.

S.Lee and T.Sakurai, "Run-time Voltage Hopping for Low-power Real-time Systems," DAC'00, June 2000.

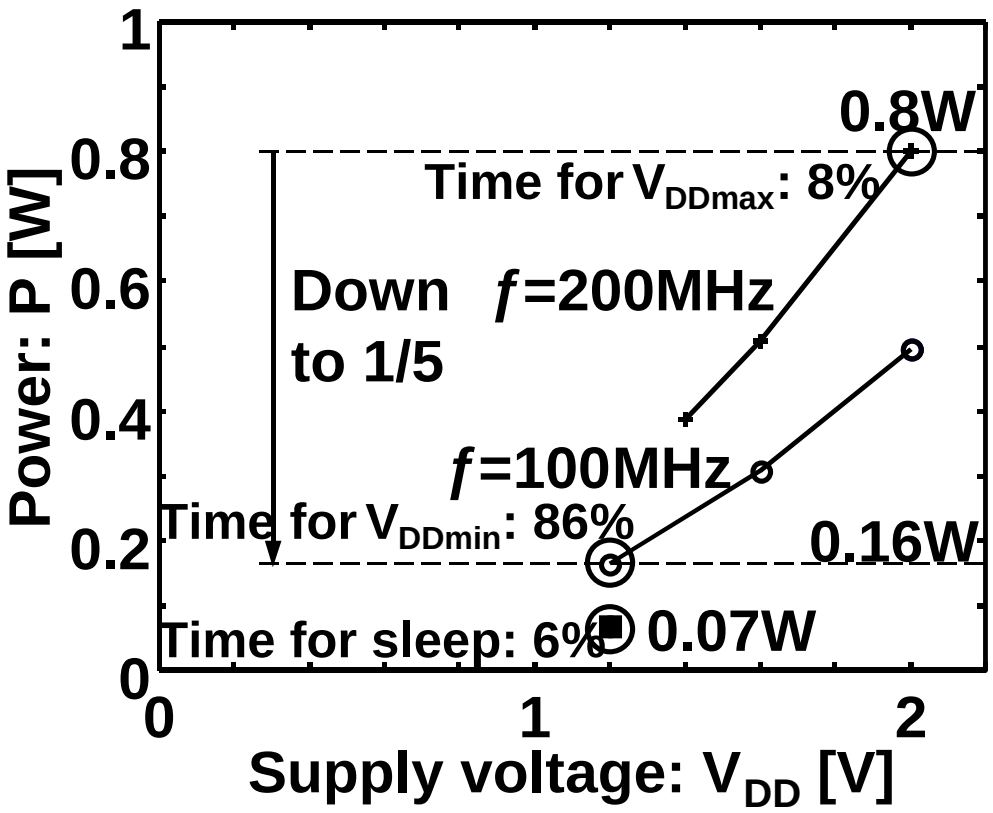
Voltage hopping achieves more than 70% power saving





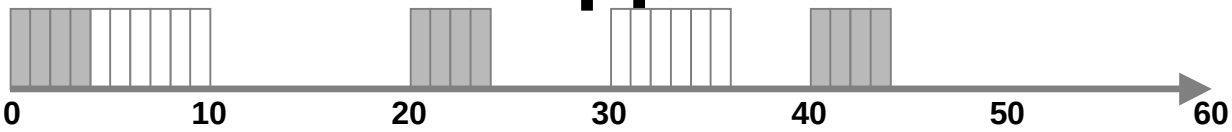
Measured power characteristics

Total power = 0.8 x 0.08 + 0.16 x 0.86 + 0.07 x 0.06 = 0.2W

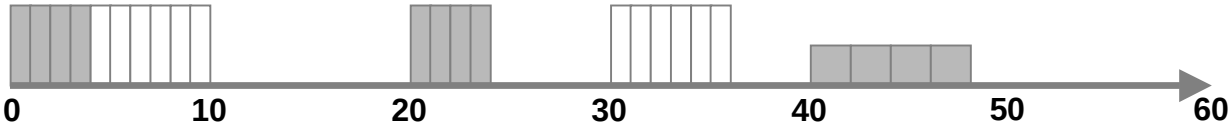


VDD hopping can cut down power consumption to 1/4

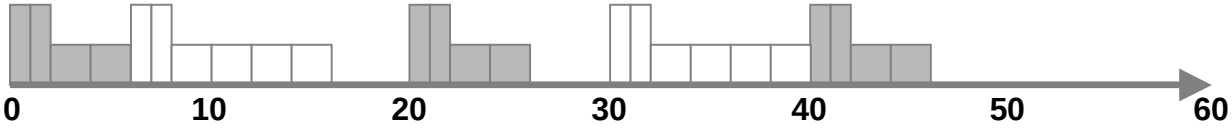
Cooperative Voltage Scaling (CVS) between OS and Applications



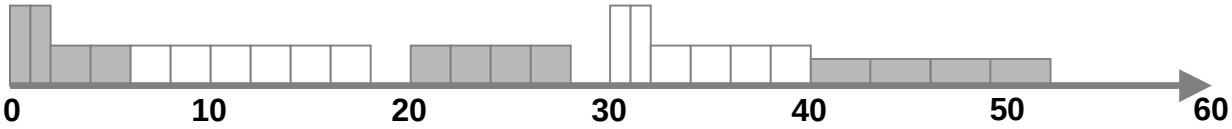
Conventional rate-monotonic scheduling (power consumption=1)



Speed control with power-conscious OS (power consumption=0.85)



Speed control within application slices (power consumption=0.47)

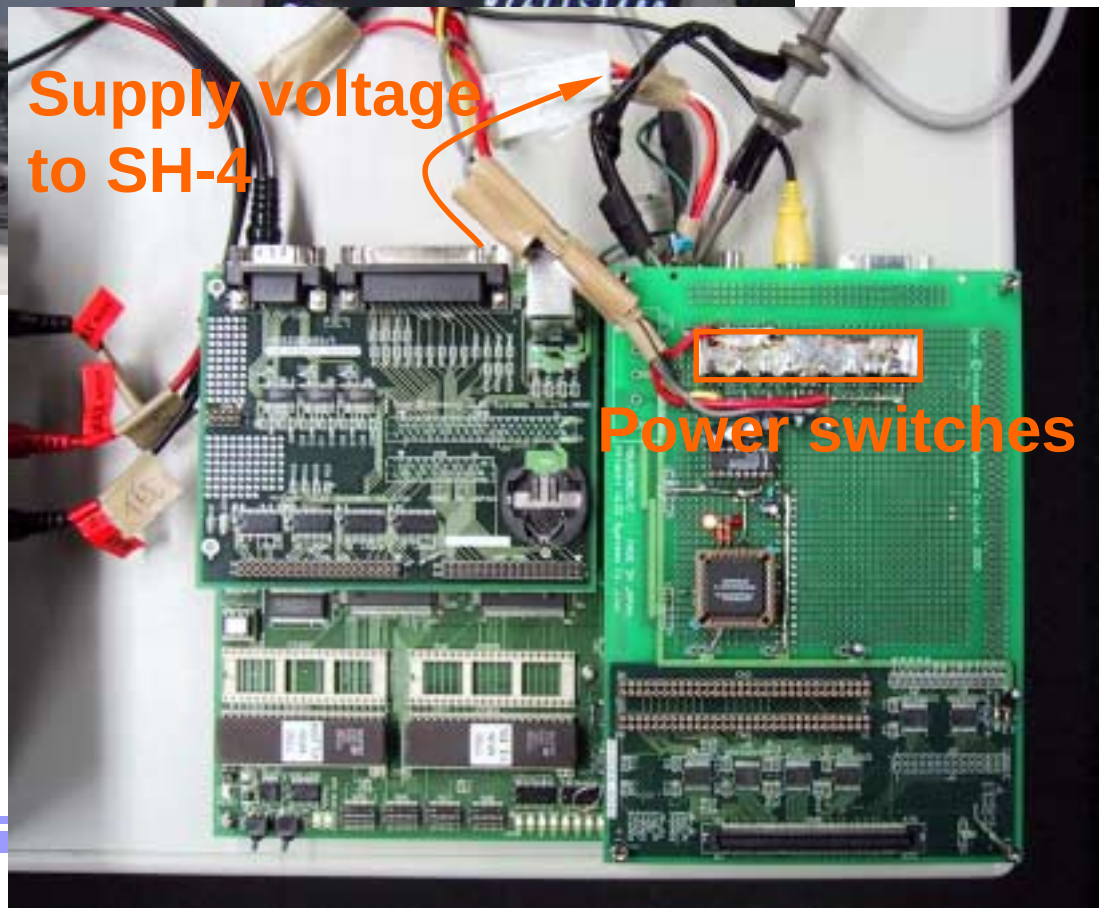


Proposed scheduling: cooperation of OS and applications (power consumption=0.24)

Y.S.Shin, H.Kawaguchi, T.Sakurai, "Cooperative Voltage Scaling (CVS) between OS and Applications for Low-Power Real-Time Systems," CICC'01, pp.553-556, May 2001.

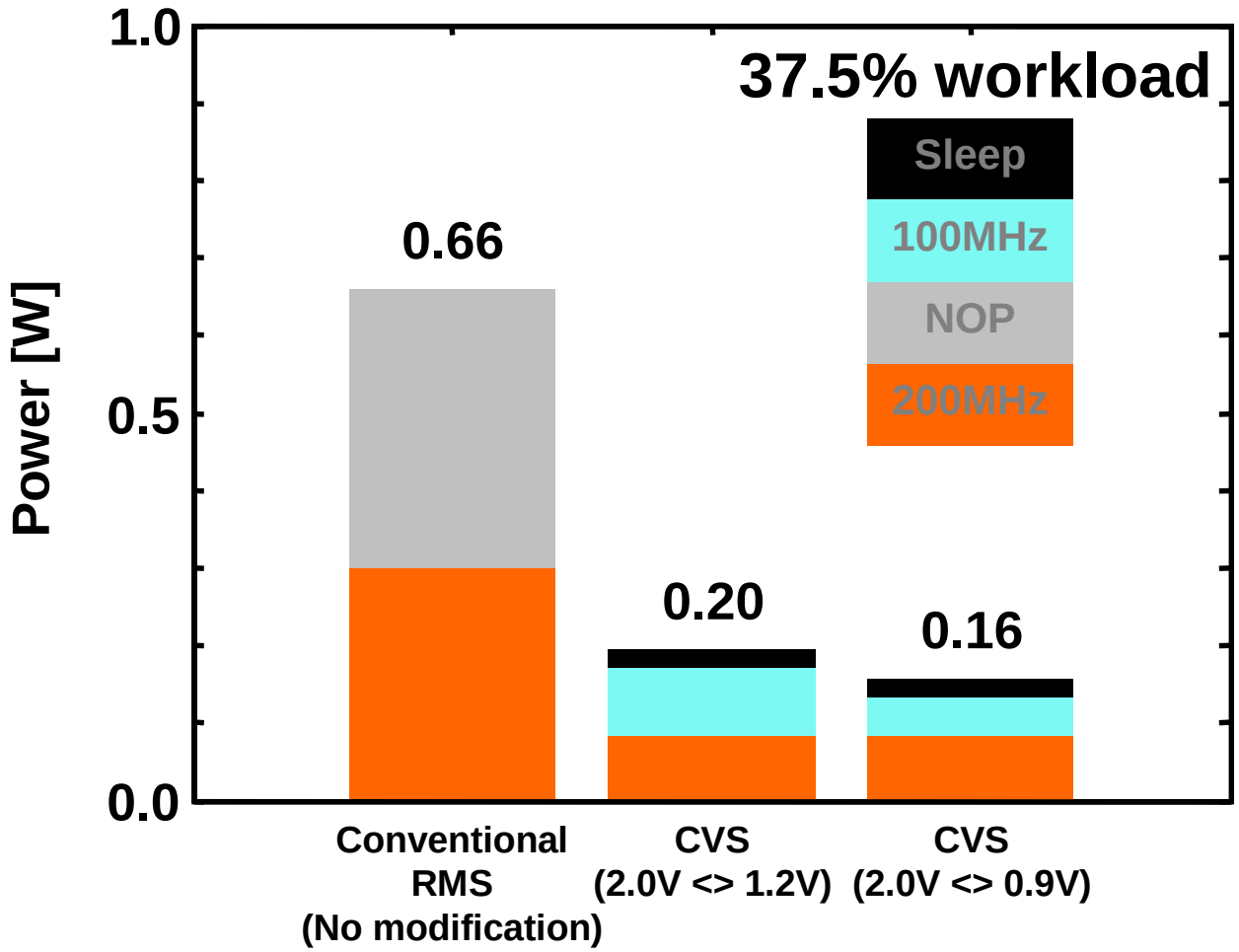
Hardware

(A) System



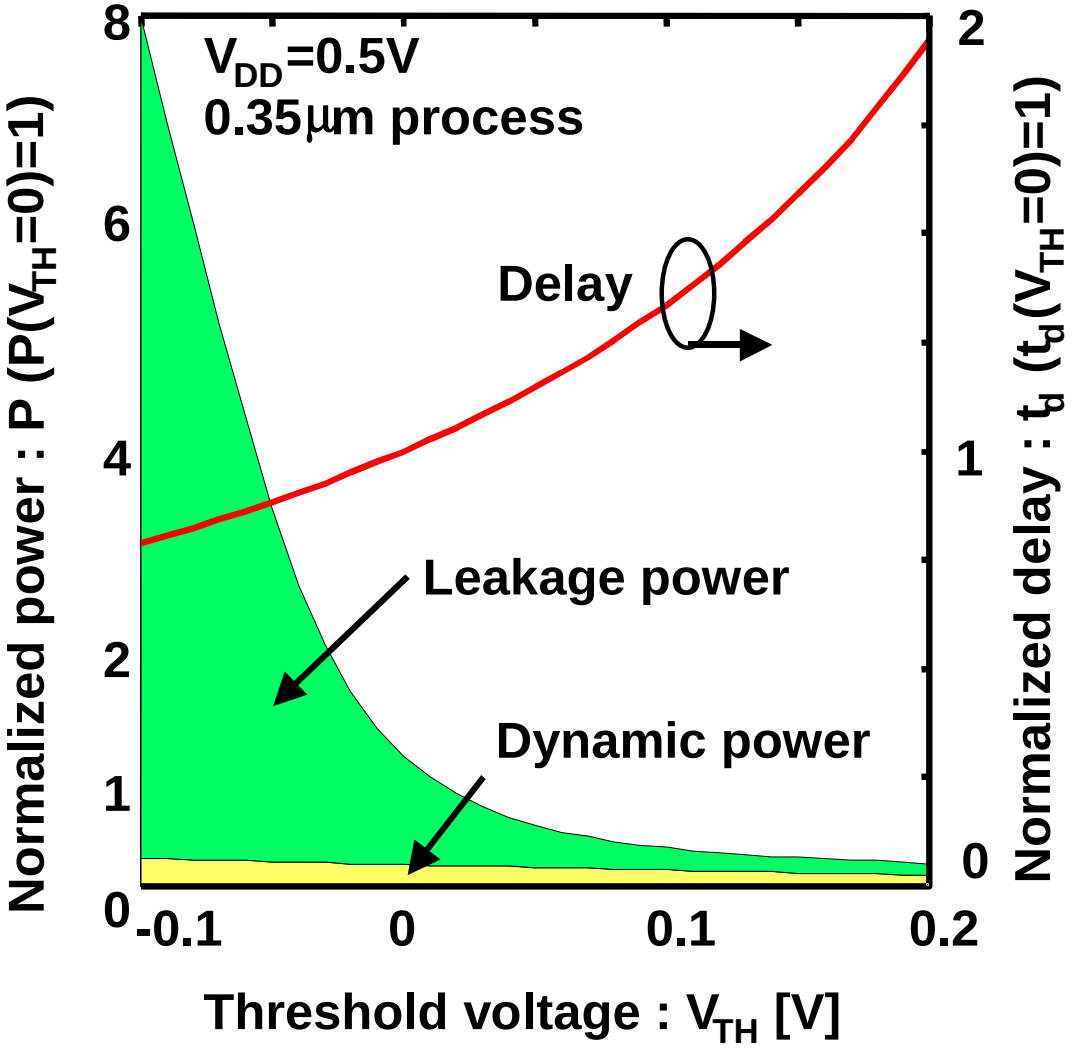
(B) SH-4 embedded board

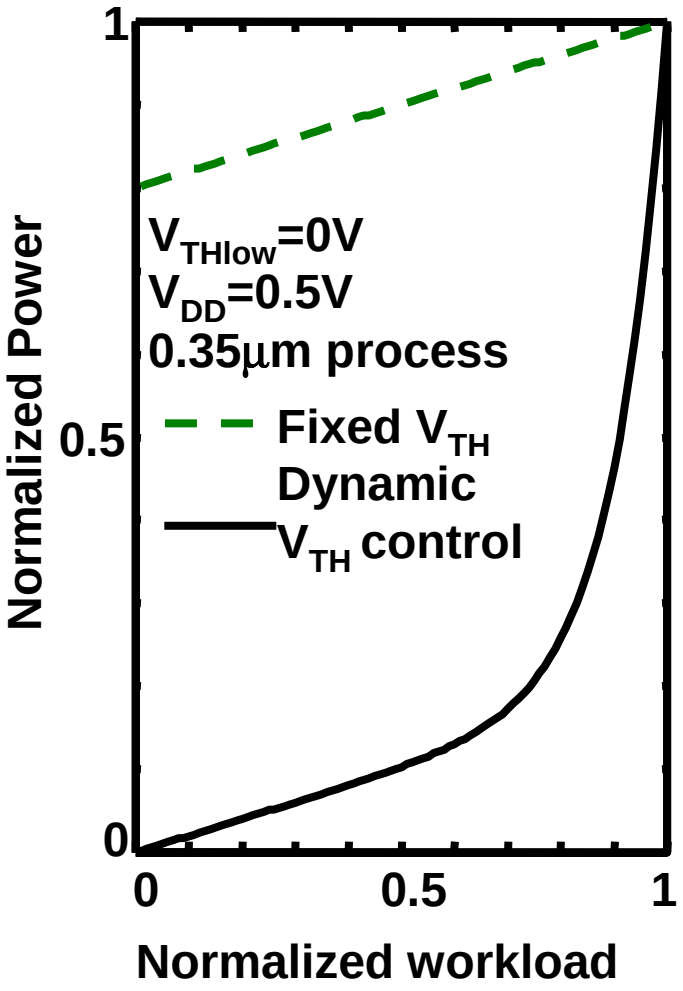
Power comparison to conventional RMS



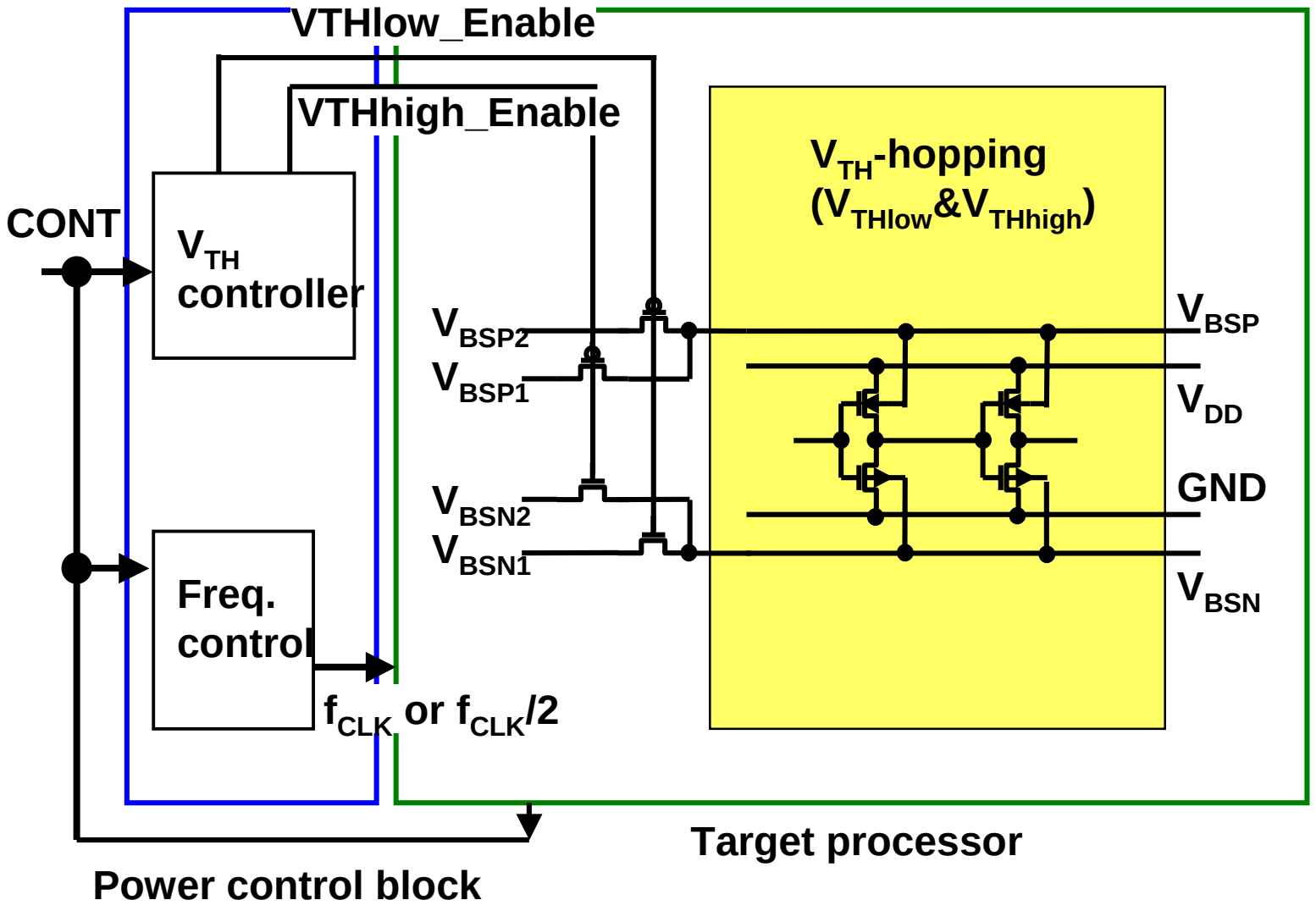
- CVS can reduce power to less than 1/4 of the conventional.

V_{TH}-hopping

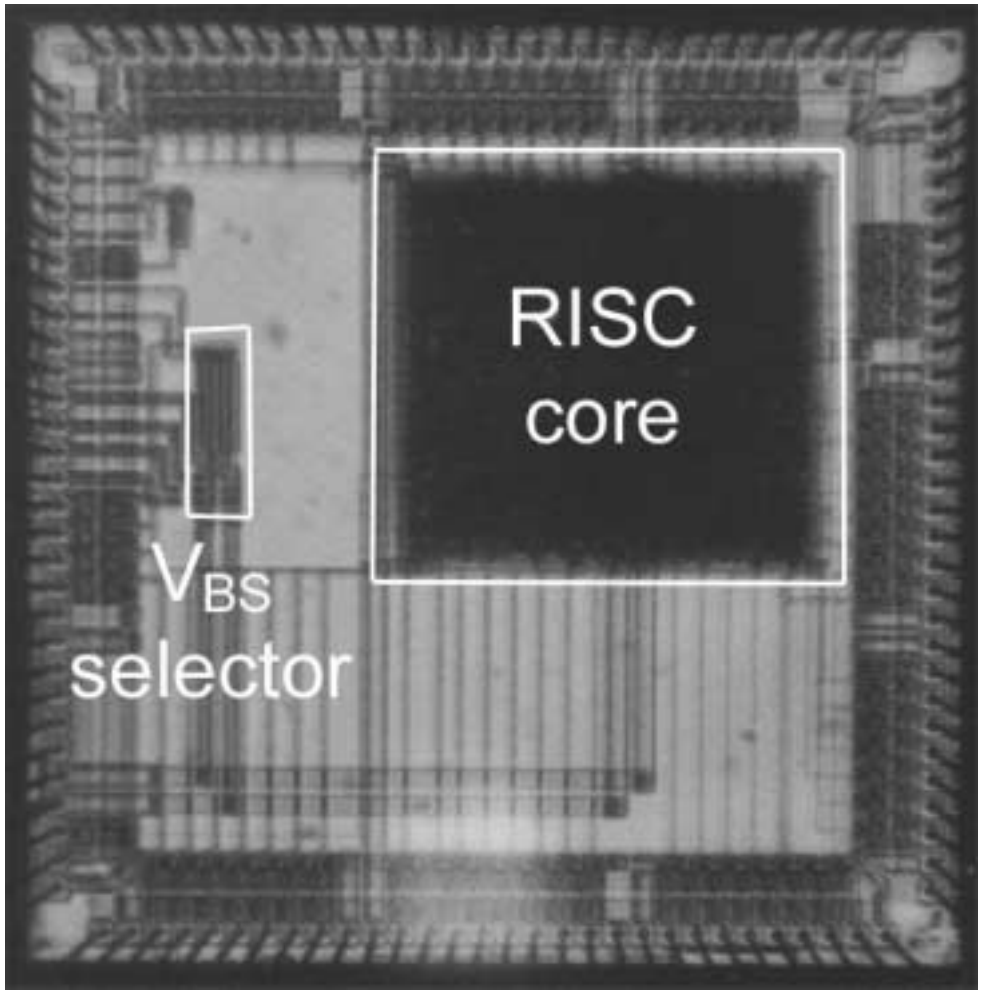

V_{DD}=0.5V
0.35μm process
Delay
Leakage power
Dynamic power
Normalized power : P (P(V_{TH}=0)=1)
Normalized delay : t_d (t_d(V_{TH}=0)=1)
Threshold voltage : V_{TH} [V]
8
6
4
2
1
0
-0.1
0
0.1
0.2
2
1
0


V_{THlow}=0V
V_{DD}=0.5V
0.35μm process
Fixed V_{TH}
Dynamic
V_{TH} control
Normalized Power
Normalized workload
1
0.5
0
0
0.5
1

Schematic of V_{TH}-hopping



Microphotograph of RISC processor

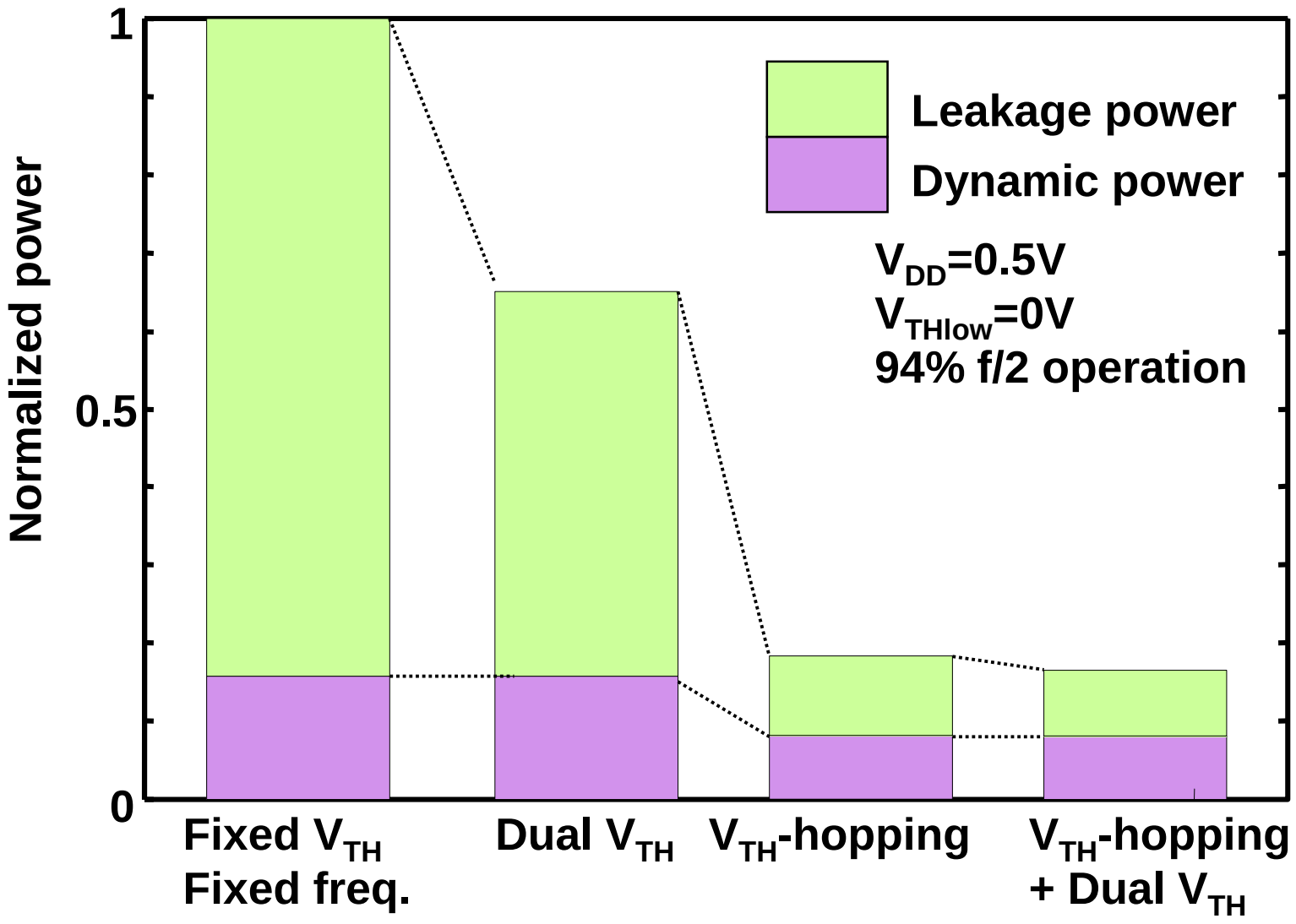


0.6μm process

Overhead of V_{TH}-hopping
= 14%

RISC core
= 2.1mm x 2.0mm
V_{BS} selector
= 0.2mm x 0.6mm

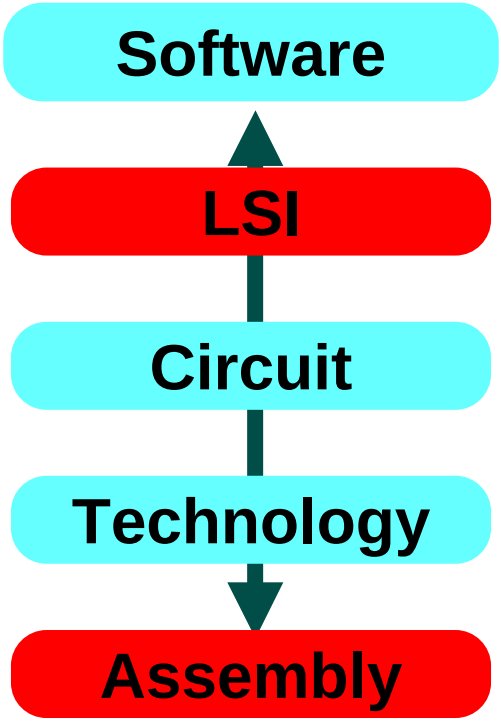
Power comparison



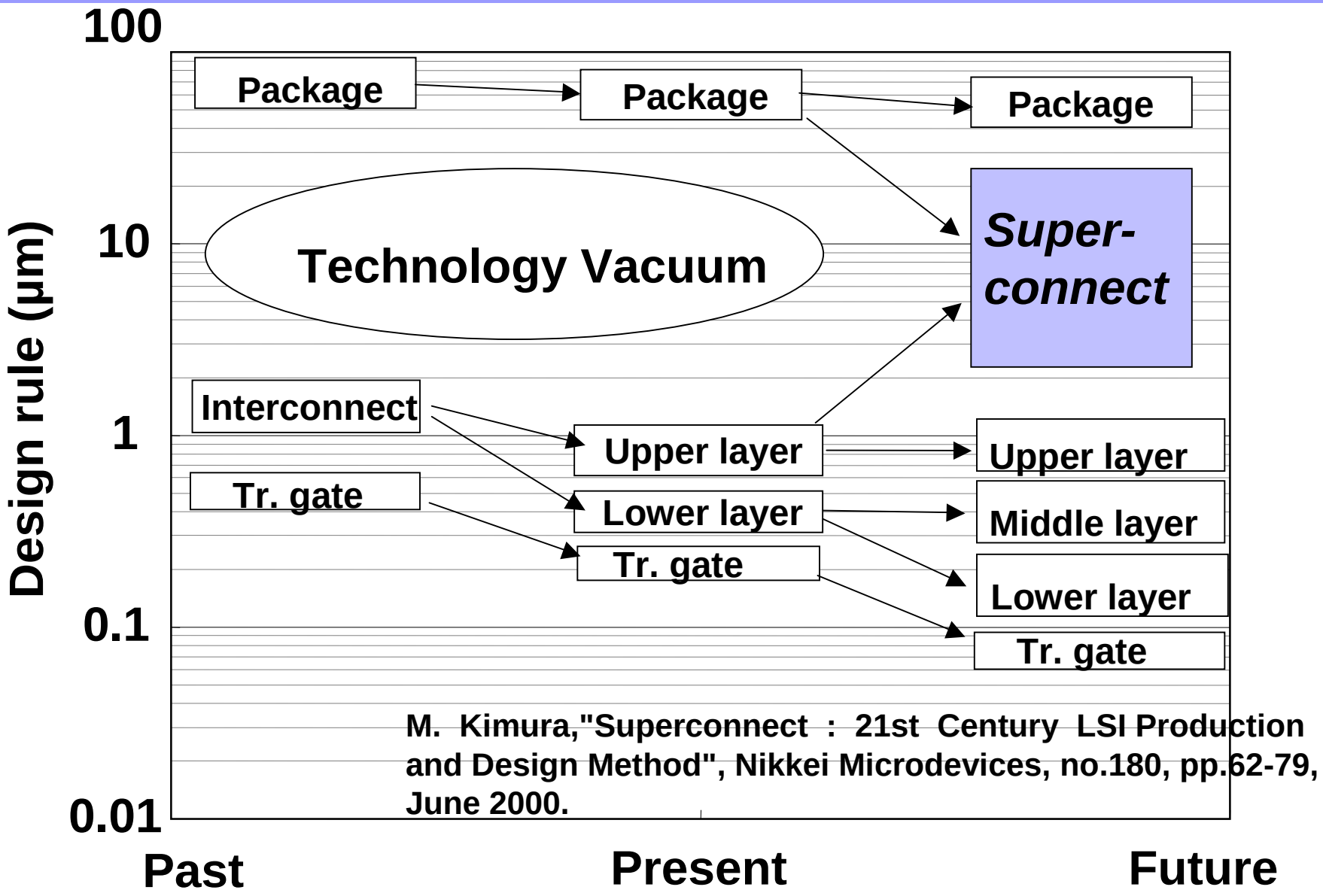
Outline

Low-power LSI - Through cooperation among levels -

- Introduction
- Technology - Circuit cooperation : Boosted Gate MOS (BGMOS)
- Software - LSI cooperation : VDD / VTH-hopping
- LSI – Assembly cooperation: Superconnect technology
- Summary



Super-connect technology



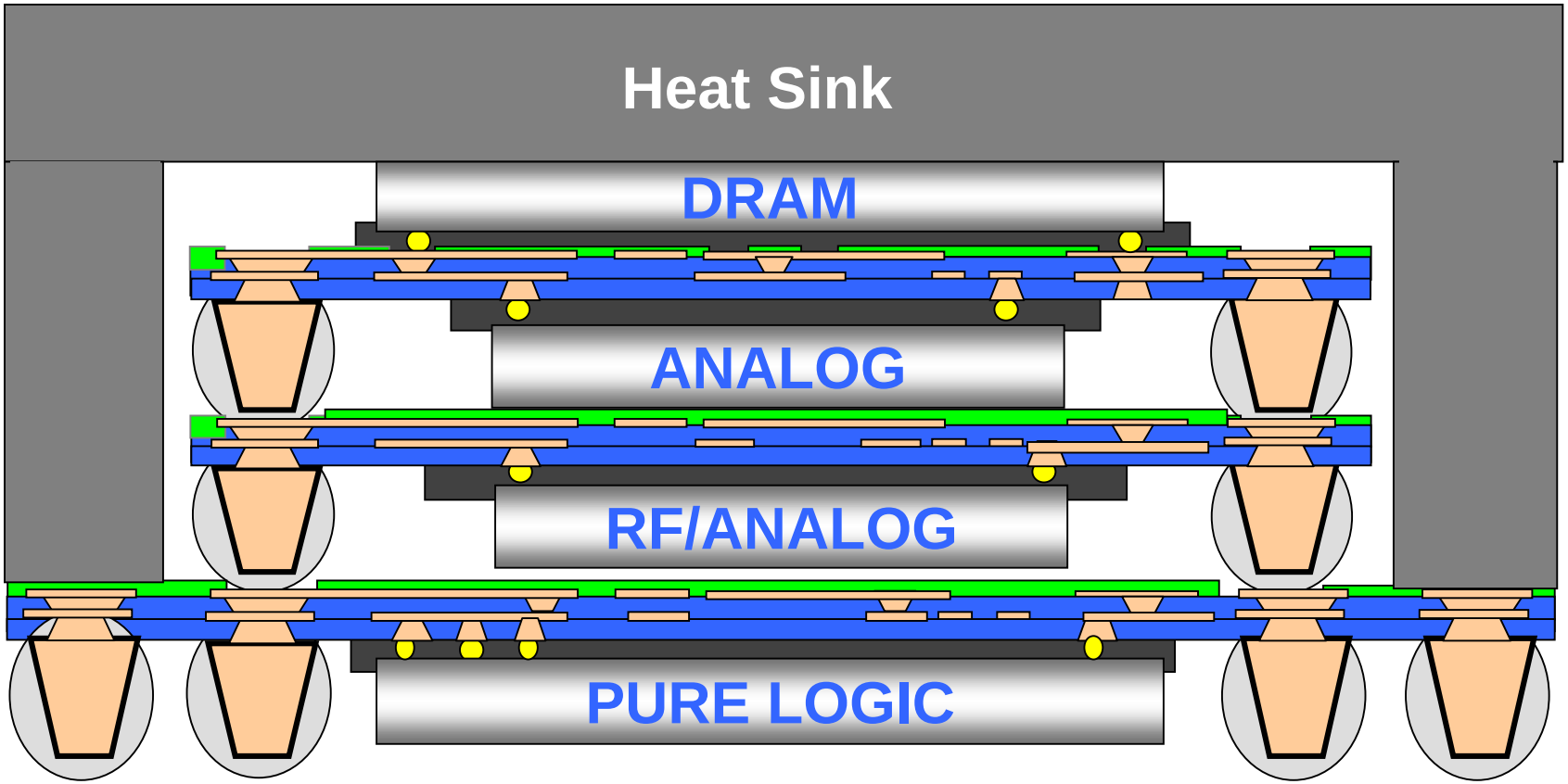
Super-connect

- Printed circuit board (PCB) : Low-perf., high-power
- SoC : High-performance but issues remain

- New system level integration : Super-connect

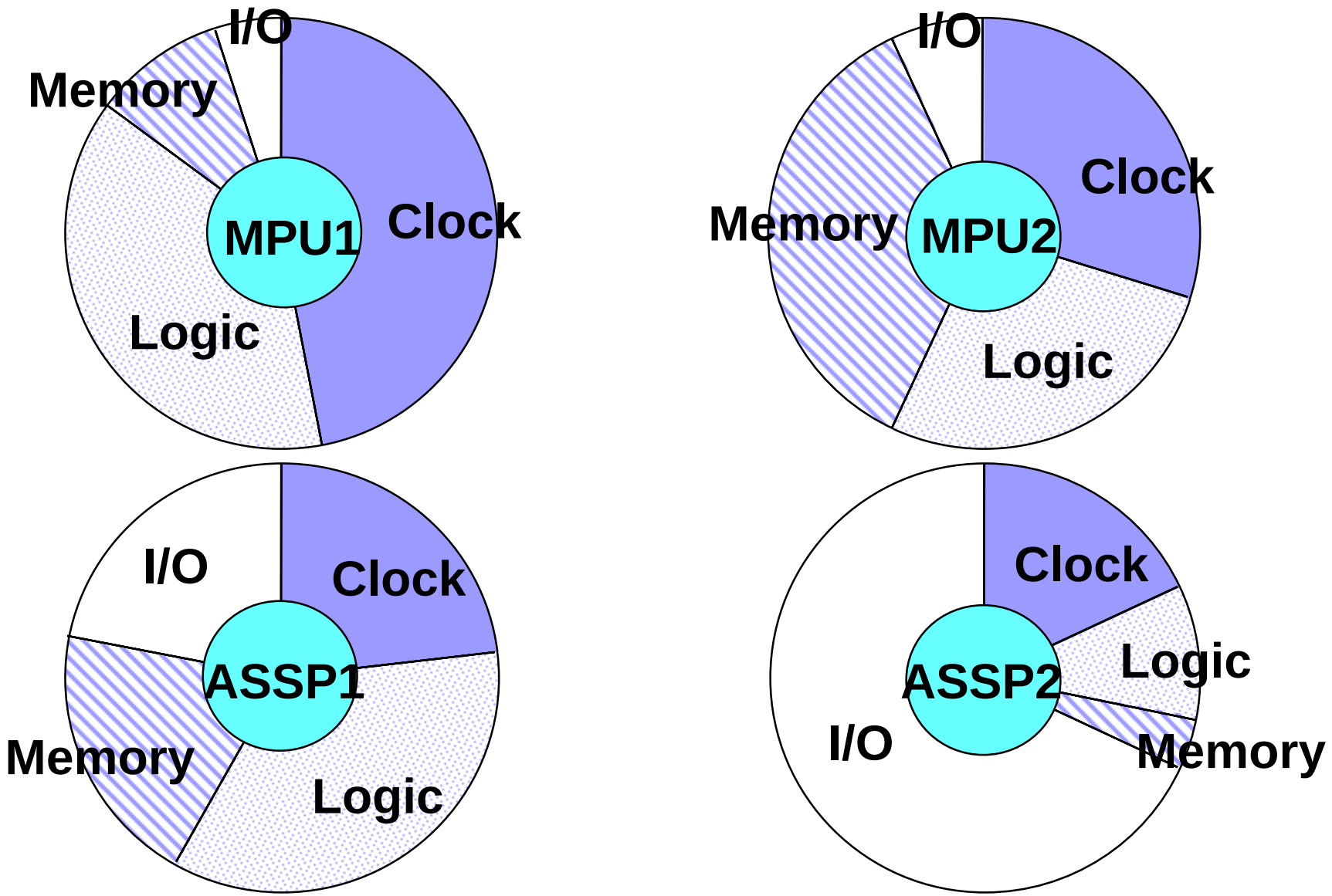
  - Connects separately built and tested chips not by the PCB but rather directly to construct high-performance yet low-cost electronic systems
  - May use around 10 micron level design rules

Super-connect example

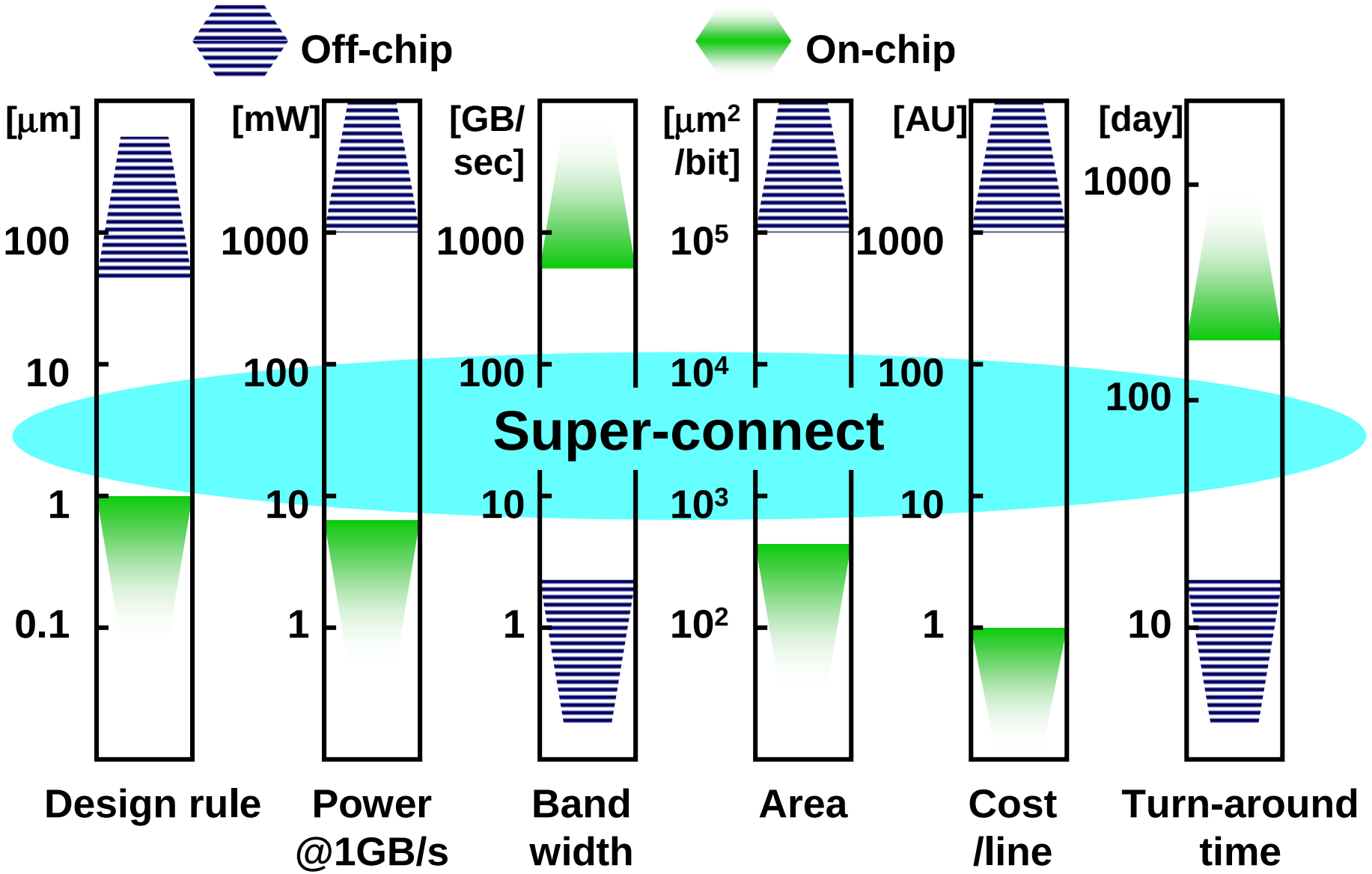


K.Ohsawa, H.Odaira, M.Ohsawa, S.Hirade, T.Iijima, S.G.Pierce, “3-D Assembly Interposer Technology for Next-Generation Integrated Systems,” ISSCC Digest of Tech. Papers, pp.272-273, Feb.2001.

Power distribution in CMOS LSI's

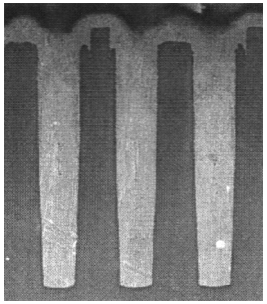


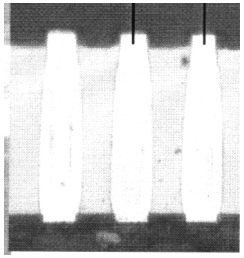
Super-connect

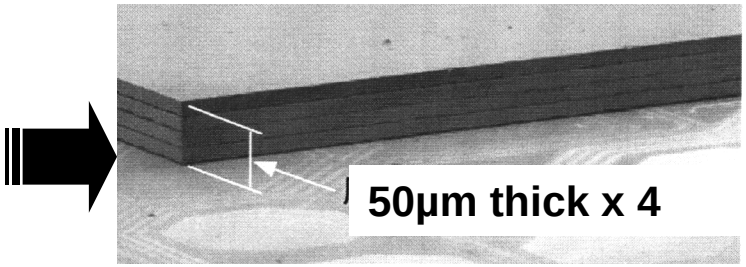


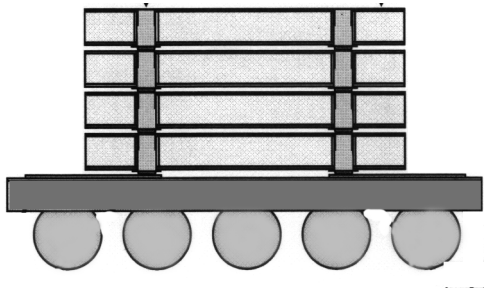
T.Sakurai

3D integration by super-connect









By ASET

Summary

- **Power consumption of LSI's tend to increase due to the scaling law and due to the leakage increase (sub-threshold, gate tunneling, and junction leakage).**

- **New trend for low-power LSI's is to pursue cooperative approaches among levels: BGMOS to cut-off standby leakage, V_{DD} / V_{TH} hopping to reduce operating power, and super-connect to reduce I/O power.**

- **One of the biggest barriers to the scaling is the leakage power increase and solutions are yet to be discovered.**