90% Write Power Saving SRAM Using Sense-Amplifying Memory Cell

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Abstract

A low power write scheme is proposed for an SRAM using seven-transistor sense-amplifying memory cells, which can save 90% of the power in write cycles when 4M SRAM is assumed. By reducing the bit line swing to 1/6 V_{DD} and amplifying the voltage swing by a sense-amplifier structure in a memory cell, charging and discharging component of the power of the bit lines is reduced. A 64Kbit test chip has been fabricated and operation has been verified.

Introduction

An SRAM is and is continued to be an important building block of System-on-a-Chip's. Low power feature for on-chip SRAM's is getting more important for mobile applications than just a small foot-print of the SRAM.

On-chip SRAM's tend to have large number of bit width such as 16 to 256 or even greater. In this type of SRAM's, the power of SRAM is dissipated mainly by charging and discharging of the bit line due to full swing nature of the bit lines in the write cycles. The power consumed in write cycles is much larger than that in read cycles. Reducing swing level is effective to reduce the power dissipation in write cycles and a half swing technique has been reported [1]. In the half swing scheme, 75% power reduction was achieved by restricting the bit line swing to a half of V_{DD}. It is, however, difficult to further reduce the power due to write-error problem in this scheme. One more issue associated with the half swing technique is that if the write and read cycles come alternately, there is additional power consumption due to the mismatch of the level of bit lines in read cycles and that in write cycles.

In this paper, a novel low-swing SRAM scheme using sense-amplifying cell is presented, with which further power saving in write cycles is possible. Since the write power is dominant in SRAM's with wide bit width, the peak and average operation current can be reduced.

Sense-Amplifying Cell (SAC) Scheme

Figure 1 (a) shows the circuit diagram and the associated timing chart of the proposed sense-amplifying cell (SAC) scheme. The salient feature of the scheme is an additional NMOS connected to the source of driver transistors in a memory cell, which enables low-swing of bit lines in a write operation. If the swing level of bit lines is denoted as ΔV_{BL}, the power consumed in bit lines is $fC_{BL}\Delta V_{BL}^2$. A bit line is precharged to V_{DD}-V_{TH} by an NMOS precharge transistor and is pulled down to V_{DD}-V_{TH}-ΔV_{BL} in a write '0' operation. The voltage level of V_{DD}-V_{TH}-ΔV_{BL} is prepared by a DC-DC converter with a help of voltage reference generator shown in Fig. 1 (b).

The precharge level must not be V_{DD} because access transistors of the cell cannot turn on in the write operation in this scheme. ΔV_{BL} must be independent of V_{TH} fluctuation in order to assure stable write operation. Figure 1 (b) shows write voltage generator which makes the voltage V_{WR} equal to V_{DD}-V_{TH}-ΔV_{BL} even in the presence of the V_{TH} fluctuation. Figure 2 shows ΔV_{BL} dependence on the V_{TH} fluctuation realized by the circuit. When V_{TH} is fluctuated by ±0.15V, ΔV_{BL} fluctuation can be kept as low as ±30mV. V_{WR} is used as a reference voltage in the DC-DC converter and the converter supplies V_{WR} to each bit lines through the write circuit.

Figure 1 (c) shows a sketch of waveforms in a write cycle. The NMOS switch connected to the source of driver transistor is turned off before a word line is accessed in a write cycle. Even if the voltage difference between a pair of bit lines is small, cell node can be inverted because the driver transistors do not draw current while the word line is activated thanks to the NMOS switch. Being different from the half swing technique, there is no additional power consumption even if the write and read cycles come alternately, because there is no mismatch between the level of bit lines in read cycles and that in write cycles.

Figure 3 and 4 show simulation results of power dissipation of 4M SRAM operated at 100MHz in 0.35μm technology. The more the bit width is, the more the total write power is saved because the power consumed by bit line charge and discharge becomes more dominant compared with the power of the other circuits when the bit width gets larger. When the bit width is 256, total write power is saved by 90% and 67 % compared with the conventional full swing scheme and half swing scheme, respectively.

Design Considerations

Figure 5 shows simulated delay and noise margin. Noise margin is defined as length of a diagonal line of the maximum square in the area bounded by the transfer curve of the memory cell and its 45-degrees mirror. Both read delay and noise margin may be degraded due to the additional NMOS switch in a memory cell. Area overhead also exists. In order to reduce area overhead, the NMOS switch can be shared by N cells. Parameter ß signifies a ratio of the channel width of the NMOS switch per cell to the channel width of a driver transistor. There is no read delay increase and no noise margin decrease even when the NMOS switch is shared among N memory cells.

If ß is large, it is good for delay and noise margin but area increases. Considering simulation results, ß=3 and N=4 are chosen, which corresponds to 5% delay increase, 25% noise margin decrease and 11% area increase. Here, a 4Mbit SRAM is assumed and cell area occupancy is assumed to be 60% of the total area of a SRAM macro. The read delay is defined the delay from address buffer input to output buffer output placed after a sense amplifier.

Measurement Results

Figure 6 shows a microphotograph of the chip fabricated with 0.35μm triple-metal CMOS process. Measurement results of power dissipation in write cycles are plotted in Figs. 3 and 4. Sense amplifying cell scheme enables to write data in a cell with low swing bit lines and reduces total write power by 90% when bit width is 256.

Conclusion

Sense amplifying cell (SAC) scheme is presented, which saves the power in the write cycle by 90% through the use of low-swing bit-lines. A test chip has been fabricated and a correct operation has been verified. Assuming 4M on-chip SRAM, the delay overhead and area overhead of the scheme are estimated to be 5% and 11%, respectively.

Acknowledgement

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References

[1] Kenneth W. Mai, Toshihiko Mori, Bharadwaj S. Amrutur, Ron Ho, Bennett Wilburn, Mark, A. Horowitz, Isao Fukushi, Tetsuo Izawa, and Shin Mitarai, "Low-Power SRAM Design Using Half-Swing Pulse-Mode Techniques", IEEE J. Solid-State Circuits, vol.33, No.11, pp.1659-1671, Nov., 1998

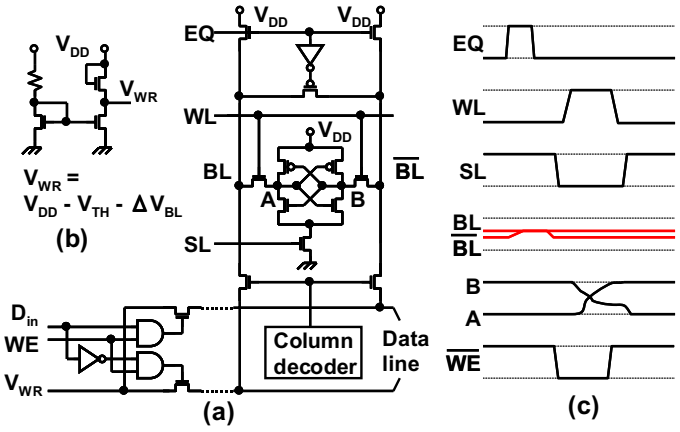


Fig.1 (a) Write voltage generator (b) Circuit schematic of SRAM using sense-amplifying cell (SAC) (c) Write cycle waveforms

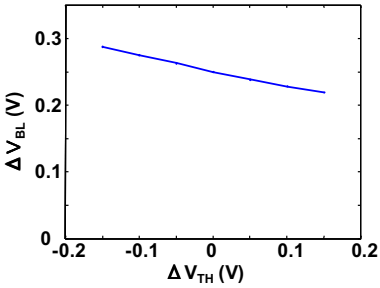


Fig.2 ΔV_{BL} dependence on ΔV_{TH}

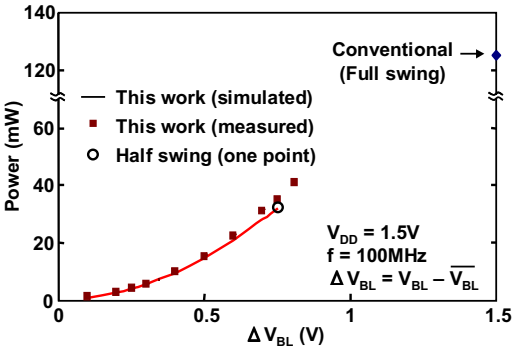
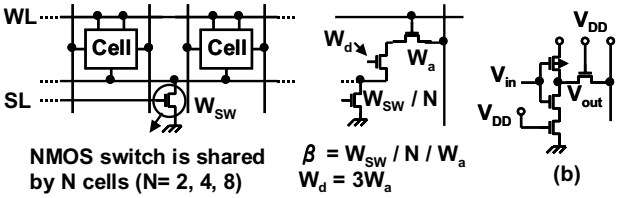


Fig.3 Write power consumption of bit lines versus bit line swing ΔV_{BL}



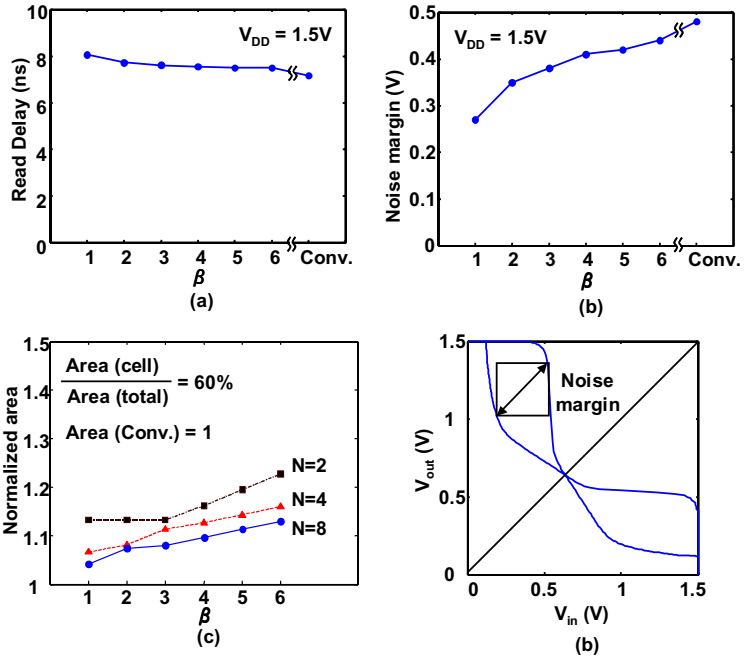


Fig.5 (a) Read delay, (b) noise margin, and (c) area. NMOS switch can be shared by N cells in order to reduce area overhead, but there is no delay increase and no noise margin decrease.

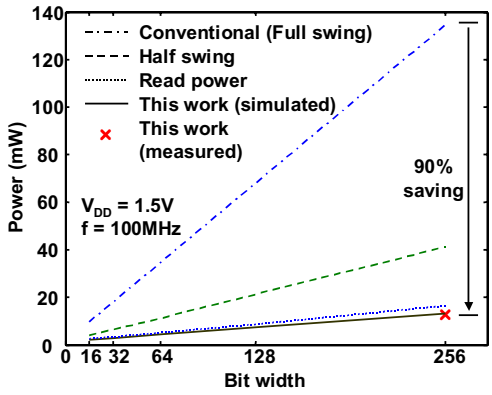


Fig.4 Write power consumption of SRAM versus bit width

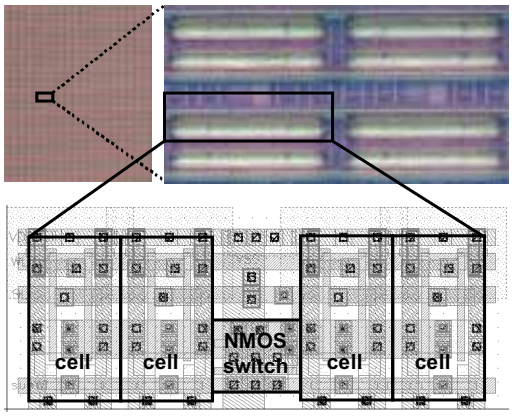


Fig. 6 Microphotograph and cell layout