POWER CONSUMPTION DISTRIBUTION IN DSM INTERCONNECTS WITH INDUCTIVE EFFECTS

Danardono Dwi Antono, and Takayasu Sakurai

Institute of Industrial Science, University of Tokyo

1. Inductive effects in DSM interconnects

As scaling of technology continues to the Deep Sub-Micron (DSM) regime, some papers claimed that on-chip interconnects inductive effects, such as propagation delay increase, overshoots, and inductive crosstalk, can no longer be ignored. Inductive effects in circuits could be analyzed by comparing the property when inductance is ignored and when it is considered. In previous works [1][2], we presented that propagation delay error, and overshoots of optimally buffered *RLC* interconnects could be suppressed by keep using interconnects with minimum width. In this paper, power consumption distribution in DSM interconnects with inductive effects is discussed.

2. Power consumption distribution

Traditionally, power consumption (or energy dissipation) of a particular resistor element can be calculated using formula (1). Where *j(t)* is current flowing in the resistor in time-domain function. Figure 1 shows a gate driving 1-step π-ladder *RLC* interconnects. Where *Rt*, *Ct*, and *len* are equivalent resistance of the driver, load capacitance, and interconnects length, and *R*, *L*, and *C* are interconnects resistance, inductance, and capacitance, respectively. If inductance is neglected (*RCRC*), energy dissipated in resistors *Rt* and *R* in Figure 1, can be calculated using formulas (2), and (3), which are derived with formula (1). Where *Ra=Rt*, *Rb=R*, *Ca=C/2*, and *Cb=C/2+Ct*. When inductance is considered (*RCRLC*), however, expressions for calculating power consumption cannot be derived in simple formulas. Instead, it is easy to calculate energy dissipated in resistors using a model order reduction method proposed in [3].

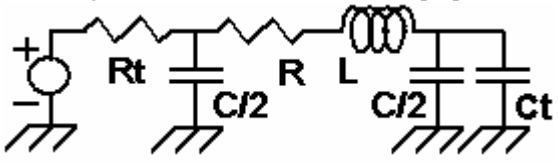

Figure 1: Driver-interconnects-load (*RCRLC*)

$$P_i = R_i \int_0^\infty j^2(t) \cdot dt \tag{1}$$

$$Pa = \frac{Vdd^2\left\{Ra(Ca+Cb)^2 + Rb \cdot Ca \cdot Cb\right\}}{2\left\{Ra \cdot Ca + Ra \cdot Cb + Rb \cdot Cb\right\}} \tag{2}$$

$$Pb = \frac{Vdd^2\left\{Rb \cdot Cb^2\right\}}{2\left\{Ra \cdot Ca + Ra \cdot Cb + Rb \cdot Cb\right\}} \tag{3}$$

3. Trends of power consumption in DSM VLSI

In this work, trends of power consumption distribution is studied with optimally buffered *RLC* interconnects as examples. Optimum buffer size and optimum interconnect length could be calculated using formula proposed in [4]. Then, interconnects data was developed from ITRS data as described in [1].

Tables 1 and 2 show calculation and comparison results of power consumption distribution of optimally buffered global interconnects for various technology nodes, and interconnects width *W* where inductance is neglected (*RC*), and considered (*RLC*). The results explain that (1) Power consumption distribution is constant in percentages as technology node continues where energy changed to heat in interconnects is about a half of energy dissipated in buffer resistance; (2) Comparing *RC* and *RLC* one, although it is not pretty significant, the power consumed in interconnects increases in *RLC*; (3) Error between *RC* and *RLC* also increases as wide interconnects width used.

As discussed in [1][2], instead of using n-step π-ladder *RLC* interconnects, distributed *RLC* interconnects should be used for analyzing high speed DSM interconnects behavior. Except for detail values, we believe that the three-conclusions described above will still be valid when we calculate power consumption distribution with distributed interconnects.

Table 1: Power consumption distribution of optimally buffered single global lines with various technology nodes (i.e. tech. node 90nm, *Wo*=310nm, *Rt*=98Ω, *Ct*=58fF, *len*=1.7mm, *r*=85kΩ/m, *l*=1280nH/m, *c*=132fF/m, *R*=r·len=146Ω, *Vdd*=1V)

W=Wo	Rt (1)	R (2)	(1)+(2)=(3)	(1)/(3)	(2)/(3)
RC,90	56.0 fJ	28.3 fJ	84.3 fJ	66%	34%
RC,60	30.0 fJ	15.4 fJ	45.4 fJ	66%	34%
RC,40	17.7 fJ	9.3 fJ	27.0 fJ	66%	34%
RLC,90	52.1 fJ	32.2 fJ	84.3 fJ	62%	38%
RLC,60	28.0 fJ	17.4 fJ	45.4 fJ	62%	38%
RLC,40	16.6 fJ	10.3 fJ	26.9 fJ	62%	38%

Table 2: Power consumption distribution of optimally buffered single global lines with various int. width *W* (in percentages)

	Rt, Wo	R, Wo	Rt,3Wo	R,3Wo	Rt,10Wo	R,10Wo
RC,90	66%	34%	69%	31%	72%	28%
RLC,90	62%	38%	63%	37%	65%	35%

4. References

[1] D. D. Antono, and T. Sakurai, “Inductance Effect on VLSI Interconnections,” Proceeding of Society Conference of IEICE A-3-7, September 2001.

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[3] Y. Shin, and T. Sakurai, “Power Distribution Analysis of VLSI Interconnects Using Model Order Reduction,” IEEE Trans. on CAD, vol. 21, no. 6, 739-745, June 2002.

[4] Y. I. Ismail, and E. G. Friedman, “Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits,” IEEE Trans. on VLSI, vol. 8, no. 2, pp. 195-206, April 2000.