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#### 1. Introduction

Signal integrity becomes serious topic in recent VLSI's, since it can restrict VLSI's performance. Previously, interconnect inductance is neglected and interconnect is modeled by Resistance-Capacitance (RC) model. Recently, with the parameter sizes entering deep submicron range, however, inductance has become an important consideration in the design and analysis of on-chip interconnects. Therefore, inductive interconnect and its responses need to model. In this work, modeling of inductive interconnects is employed, analytical expressions are shown, and numerical calculation as well as circuit simulation are figured. Thus, inductive effects in single line and adjacent interconnects can be concluded analytically.

To grasp the characteristics of interconnects and behavior of circuit accurately, kind of an internal on-chip digital oscilloscope is being developed. Using this measurement circuit, noise due to coupling effects in power line and waveforms of the signal can be reproduced. Thus, the problems of signal integrity are recognized and should be coped. This result will also make it obvious, whether when inductance should be considered.

- 2. Modeling of inductive interconnect responses and coupling effects
- 2.1. Transient response in single line

Figures 1 and 2 show gate driving inductive interconnects with load capacitance and two adjacent interconnects, respectively. Instead of using the real parameters, however, normalized parameters, which are normalized by R and C, are introduced to simplify the expressions for analyzing interconnects characterization. Those parameters are listed in Table 1.



Fig. 1. Single interconnect

Expression (1) shows output transient response expression  $V_o$  using normalized parameters. Note that this expression is derived from transfer function with telegrapher's equations for interconnect part and step function is given for input voltage  $V_i$ .

$$V_{o}(\sigma) = V_{DD} / (\sigma \cdot A(\sigma))$$
(1)

where  $A(\sigma) = (1+\sigma \cdot r_T \cdot c_T) \cdot \cosh(\sigma(1+l_T \cdot \sigma))^{\frac{1}{2}} + (\sigma/(1+l_T \cdot \sigma))^{\frac{1}{2}} \cdot (r_T+c_T(1+l_T \cdot \sigma)) \cdot \sinh(\sigma(1+l_T \cdot \sigma))^{\frac{1}{2}}$ . **r**, **l**, **c V**<sub>ag</sub> **r**, **l**, **c V**<sub>ag</sub> **r**, **l**, **c V**<sub>ag</sub>



Fig. 2. Two adjacent interconnects

Since output response can be figured only in time domain, Laplace function (1) should be transformed to time domain function. However, inversing (1) results in very difficult and complicated expressions [1]. Thus, instead of using exact function as (1), approximation function of (1) has been developed and shown as follows,

For  $0 \le \tau \le l_T^{\frac{1}{2}}$ ,  $v_0(\tau) = 0$ . (2) For  $l_T^{\frac{1}{2}} < \tau$ ,  $v_0(\tau) = 1 + k_1 \cdot \exp(-p_1 \cdot \tau) + k_2 \cdot \exp(-p_2 \cdot \tau)$ where  $v_0(\tau)$  is inversed Laplace transform of  $V_0(\sigma)$ in time domain and  $V_0(\sigma)$  is shown as follows,  $V_0(\sigma) = V_{DD}/\sigma \cdot \{l_T(c_T + l_2)\sigma^2 + (r_T \cdot c_T + r_T + c_T + l_2)\sigma +\}^{-1}$ . Note that  $l_T^{\frac{1}{2}}$  is known as time of flight parameter and this approximation function is able to be transformed in closed-form of time-domain function.

Table 1 Notations

Rt : input buffer resistance	$\sigma = s \cdot R \cdot C$ : normalized s
Ct : load capacitance	$T = t/(R \cdot C)$ : normalized t
len : interconnect length	$r_T = Rt/R$ : normalized Rt
$R = r \cdot len$ : int. resistance	$c_T = Ct/C$ : normalized Ct
$L = l \cdot len$ : int. self inductance	$l_T = L/(R^2 \cdot C)$ : normalized L
$C = c \cdot len$ : int. capacitance	$m_T = M/(R^2 \cdot C)$ :normalized M
$Cc = cc \cdot len : int. coupling cap.$	$\eta = Cc/C$ : normalized Cc
$M = m \cdot len$ : int. mut. inductance	$\zeta = 1+2\eta, \chi = x/\text{len}, \mu_{\pm} = l_{\text{T}} \pm$
$k = M_{12}/(L_1 \cdot L_2)^{\frac{1}{2}}$	$m_T$ , $\sigma' = \sigma \zeta$ , $\tau' = \sigma \zeta$ , $c_T' =$
	$c_{T}/\zeta, \mu_{2} = \mu_{2}/\zeta$

2.2. Coupling in two adjacent interconnects

Two adjacent interconnects with capacitive and inductive coupling are shown in Fig. 2.  $V_{ag}$  and  $V_{vi}$  are output responses of aggressor and victim lines, respectively. Crosstalk occurs in victim line due to inductive and capacitive coupling from aggressor line. To model adjacent interconnects analytically, two new parameters, fast (V<sub>+</sub>) and slow (V<sub>-</sub>) waves, are introduced as follows,

$$V_{+}=V_{ag}+V_{vi}, V_{-}=V_{ag}+V_{vi}.$$
 (3)  
Since  $V_{+}$  (V<sub>-</sub>) can be expressed with expression (1)  
by substituting  $V_{o}$  with  $V_{+}$  (V<sub>-</sub>), A with  $A_{+}$  (A<sub>-</sub>), =  
 $I_{T}$  with  $\mu_{+}$  ( $\mu_{-}$ ),  $c_{T}$  with  $c_{T}$  ( $c_{T}$ ), and  $\sigma$  with  $\sigma$  ( $\sigma$ ).

Thus, by using the two approximation functions, waveform of crosstalk in victim line can be calculated analytically.

## 2.3. Calculation results

The accuracy of numerical calculation method is determined by delay error. Delay error is defined as error between 50% propagation delay time from calculation results and delay time from circuit simulation result. Above approximation function and closed-form delay function from [2] are used for numerical calculation and compared to data from circuit simulation results using distributed lossy element, which is so-called W-element in Star-Hspice based on telegrapher's equation. Note that one should not use n-step  $\pi$ -ladder for RLC model that commonly used for RC one, since it resulted in spurious ringing.

While waveform of crosstalk in victim line of two adjacent interconnects can be generated using two approximation function, and example for two adjacent optimally buffered global interconnects is shown in Fig. 3. Although the details are not mentioned here, calculation results show that our model should become candidate for modeling inductive interconnects, since not only can it estimates the propagation delay time, but also model the output waveforms in both of single interconnect and two adjacent interconnects. Thus, the phenomenon of overshoots and undershoots in single line, crosstalk due to inductive coupling effects in two adjacent interconnects are able to predict.

Finally, rule of thumb for inductive effect in interconnects is proposed. Using this rule of thumb, it is easy for designers to determine whether they have to consider interconnect inductive effect or not, since considering interconnect inductance results in complicated calculation and consumes longer simulation time.



### 3. On-chip digital oscilloscope

To recognize signal integrity in VLSI circuits, on-chip signal waveforms must first be accurately measured to get an in-depth perspective of the complicated physical phenomenon of VLSI's. Since many parts of on-chip signal cannot be measured with external oscilloscope, making on-chip embedded measurement circuits is indispensable. One of the ideas for this measurement circuit is an easy-to-use on-chip 100 GHz-sampling oscilloscope which had been developed to maintain high sampling rate [3]. It Embedded small-area phasefeatured: 1) interpolated sampling clock generators to achieve 100GHz sampling rates, 2) Charge-sharing sampling heads that are able to capture waveform overshoots and undershoots, covering a wide area range of input-voltage levels. Sampling oscilloscope, however, need repetition of the signal waveforms, which made it difficult to measure. To cope this problem, on-chip digital oscilloscope using different method is being developed. Thus, noise due to inductive and capacitive coupling, overshoots and undershoots phenomenon, other characteristics of interconnects and also behavior of circuits are able to observe directly.

## 4. Summary

Approximation function is proposed for inductive on-chip single line and two adjacent interconnects. Thus, the behavior of interconnects due to inductive effects is estimated. Moreover, on-chip digital oscilloscope circuit is being developed to capture waveforms in interconnects directly to verify the phenomenon of signal integrity.

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