Power-Gating Switch Revisited:

A Fine-Grain Optimization for Leakage-Aware CMOS Circuits

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1. Introduction

Traditional approaches are far from the optimal solution for designing power switch [1] [2]. In this paper, the feasibility of the power-gating technique is explored by using spice-based simulation. The potential benefits of fine-grain optimization are demonstrated in terms of possible power savings, switching speed, and area overhead.

2. Experimental Results

We developed a simulation frame work with HSPICE (65 nm, BPTM MOSFET model, BSIM4.0), C/C++/STL, and Perl on Ultra-Unix machine. Also, we used off-the-shelf commercial tools (Synopsys and Cadence) for the functional verification and the layout (0.18um). A typical benchmark circuit (ISCAS 74283, 4-bit adder) is used for the experiment. Figure 1, 2 and 3 show the delay overhead (over no-switch case), the leakage power overhead (over no-switch case), and the wakeup time of a 4-bit adder with different sizes (Wsw: total widths of the power switches, Wtot: total widths of the logic circuits) and the number of clusters, respectively. Figure 4 shows that the impact (virtual ground voltages) of the discharge-balanced clustering. Figure 5 shows a layout example for 4-clustering case. The results show that more than two orders of magnitude of leakage power can be saved and the area overhead can be 3.7% with 10%-width switches (smaller than traditional approaches).

3. Conclusion

Trade-offs of power-switch optimization for power-gating circuits is explored in terms of speed, power, and area. Based on these experimental results, we are working on an efficient heuristic algorithm to demonstrate that fine-grain approaches are needed for future power gating circuits.

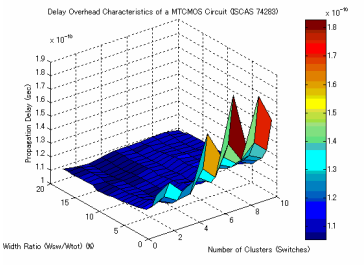

Fig.1. Delay overhead in terms of the size and the clustering of the power switch

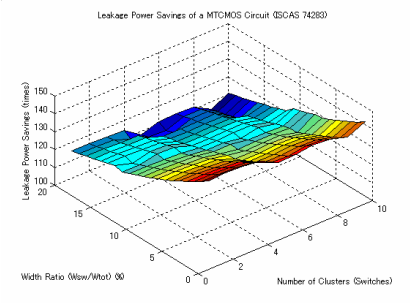

Fig.2. Leakage power savings in terms of the size and the clustering of the power switches

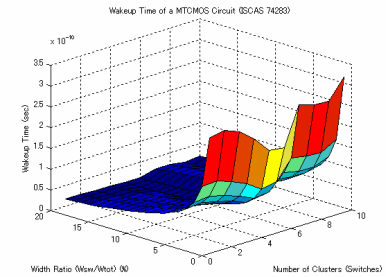

Fig.3.Wakeup time in terms of the size and the clustering of the power switch

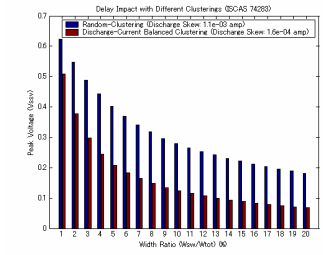

Fig.4. Impact of discharge-balanced clustering

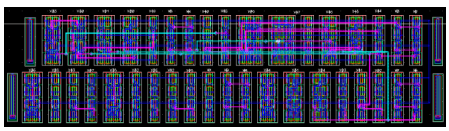

Fig.5. Area overhead with 4-switches

4. References

[1] Mutoh, et. al., IEEE JSSC, Aug. 1995 pp847 - 854
[2] J. Kao, et. al., DAC, June 1998 pp495 – 500